

## LDMOS Technology for RF Power Amplifiers

S. J. C. H. Theeuwes and J. H. Qureshi

Ampleon, Halfgeleiderweg 8, 6534 AV, Nijmegen, The Netherlands

Email: steven.theeuwes@ampleon.com

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**Abstract** - We show the status of laterally diffused metal-oxide-semiconductor (LDMOS) technology, which has been the device of choice for RF power applications for more than one decade. LDMOS fulfills the requirements for a wide range of class-AB and pulsed applications, such as base station, broadcast, and microwave. We present state-of-the-art RF performance of the LDMOS transistor measured with a load-pull test setup, achieving class-AB drain efficiencies of 70 % at 2 GHz for on-wafer and packaged devices. Furthermore, the results for several class-AB and Doherty amplifier implementations constructed with this technology are shown. As an illustration, a three-way Doherty application is demonstrated, which has a 7.5-dB back-off efficiency of 47 % at 1.8 GHz with a peak power of 700 W and linearity numbers better than -65 dBc.

**Index Terms** - Microwave amplifiers, MOSFET power amplifiers (PAs), power amplifiers, semiconductor device fabrication.

### I. INTRODUCTION

About 20 years ago, laterally diffused metal-oxide-semiconductor (LDMOS) transistors were first introduced into the RF power market as a replacement of bipolar transistors for base-station applications [1], [2]. The RF performance of LDMOS has spectacularly improved over the last decades [3], [4]. Today, LDMOS is the leading technology for a wide variety of RF power applications, to mention a few: base station, broadcast, FM, VHF, UHF, industrial, scientific, medical (ISM), and radar [5], while many new opportunities are being considered, e.g., as RF lighting [6] and microwave cooking. The LDMOS frequency range of operation has expanded in the last decades, now covering a range from 1 MHz up to 4 GHz, including WiMAX [7] and -band radar frequencies [8]. The power range of LDMOS spans more than three decades ranging from a few watts for driver devices up to a few

thousands of watts for pulsed applications.

The main driver for LDMOS has been the high volume base-station application, which requires continuous improvement, especially in efficiency, of the LDMOS technology. In the early days, LDMOS was operated in class-AB in feed-forward systems, while today, two- or three-way Doherty amplifiers in combination with digital pre-distortion (DPD) systems are the state-of-art for efficient base stations. The DPD enables good pre-distortibility at minimum power back-off (PBO), while the Doherty amplifier concept brings high back-off efficiency at the cost of linearity and gain reduction. LDMOS technology is very suitable for DPD and Doherty amplifiers [9]: due to its high gain (> 20 dB at 2 GHz), good efficiency, pre-distortibility, excellent reliability, and low cost.

The supply voltage of the mainstream LDMOS applications, in particular base station, is around 30 V, which gives a good tradeoff between power and efficiency. From low-frequency (500 MHz) and digital terrestrial television amplifiers applications, there has been a demand for high power levels. This has fueled the development of a 50-V supply voltage LDMOS [10], [11]. At the moment, the 30- and 50-V LDMOS technologies coexist on the market, each serving their own application segment.

In this paper, we show today's 30- and 50-V LDMOS technology giving device cross sections and showing RF results of on-wafer and packaged devices measured with load-pull setups. The evolution of the performance is discussed, including the key improvement parameters and the reliability [12], [13]. In the second half of this paper, we give an overview of the performance of power LDMOS devices and the performance in several Doherty amplifiers over the various frequency bands. A few of the illustrations are a 700-W 30-V LDMOS Doherty implementation at 1.8 GHz, giving 47 % efficiency at 7.5-dB back-off while meeting the tough linearity specs of multicarrier

global system for mobile communications (MC-GSM) signals. Moreover, in order to demonstrate the benefits of 50-V LDMOS technology, a 400-W 50-V LDMOS Doherty amplifier is presented that has a bandwidth of 160 MHz around 890-MHz carrier frequency. In addition to that, high-frequency applications of the LDMOS technology are demonstrated by a 40-W-band PA device for weather radar applications for 2.7–3.3 GHz.

## II. LDMOS DEVICE TECHNOLOGY

A schematic cross section of LDMOS is shown in **Figure 1**. A difference with standard CMOS is that an LDMOS transistor has a drain extension region to support the breakdown voltage. The 30- [1]-[4] and 50-V [10], [11] technology have a typical breakdown voltage of 70 and 120 V, respectively, which requires a drain extension length of 3 and 6  $\mu\text{m}$ . The epi thickness is about equal to the drain extension length. The LDMOS n+ source region is connected to the backside via a metal bridge, a p+ sinker, and a highly conducting p+ substrate. Electrons flow from the source to drain if the gate is positively biased inverting the laterally diffused p-well channel. The drain is shielded from the gate by a field plate realizing an extremely low feedback capacitance and good hot carrier reliability properties. Many fingers are placed in parallel to form a power die, resulting in a total finger length of 10–1000 mm.

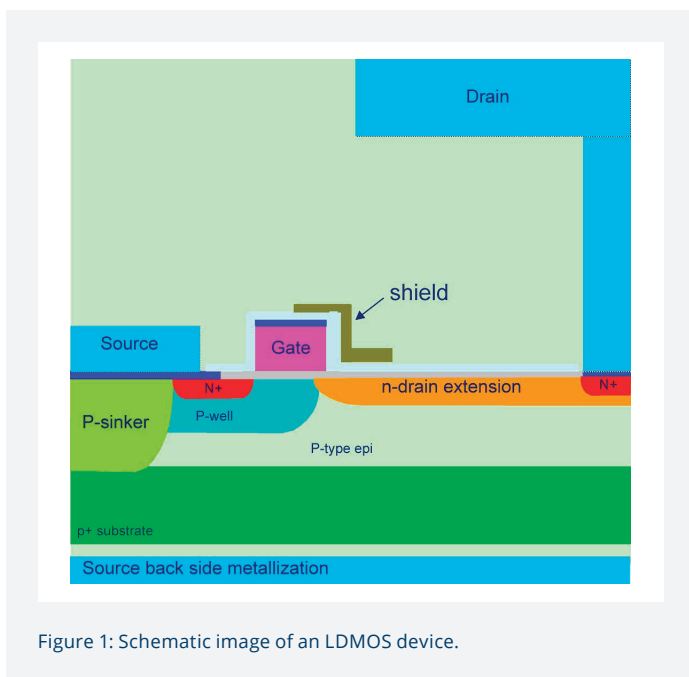


Figure 1: Schematic image of an LDMOS device.

Modern LDMOS technology is processed in a CMOS-fab, exploiting 8-in wafer manufacturing and lithography tools with capabilities down to 0.14  $\mu\text{m}$ . Additions to the CMOS process are a source sinker to the substrate, backside metallization, and tungsten shields between the drain and gate. The back-end metallization consists of multiple metal layers with thick top metals. In **Figure 2**, we show a five-metal AlCu LDMOS back-end. The top metal layers metal 4 and metal 5 are 2-

and 3- $\mu\text{m}$  thick, respectively. The drain metallization has a mushroom shape with a wide top for an optimum trade-off between electromigration reliability and performance parameters, such as (on)-resistance and output capacitance.

Two polysilicon gates, partly covered with a tungsten shield, are visible at the bottom part of the photograph. A close-up of the gate area is shown in **Figure 3**. The gate is covered with a thick  $\text{CoSi}_2$  layer to reduce the gate resistance. The thermal oxide of the gate is thin at the source side and is tapered toward a thicker oxide at the drain side, resulting in a first field plate formed by the gate. This construction gives a high gain and good reliability of the transistor. In the inset, the evolution of the gate length shows a reduction from 800 nm in the beginning of the LDMOS development down to 250 nm in 2012. The gate length reduction has spectacularly increased the LDMOS gain [7], [8]. The tungsten shield plate is in close proximity to the gate and is connected to the source metal with a repetitive metal connection (not shown). This shield not only reduces the feedback capacitance between gate and drain, but also reduces the electric fields at the end of the gate. This improved reliability makes it possible to increase the doping levels of the drain extension leading to an increase in efficiency and power density. Multiple field plates are used in the 50-V technology. The gate area for 50-V LDMOS with three

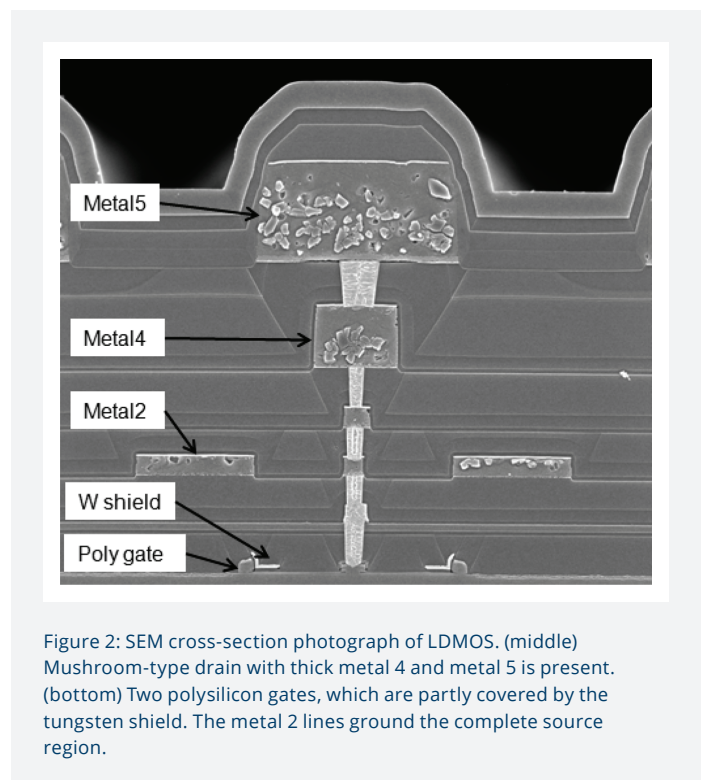


Figure 2: SEM cross-section photograph of LDMOS. (middle) Mushroom-type drain with thick metal 4 and metal 5 is present. (bottom) Two polysilicon gates, which are partly covered by the tungsten shield. The metal 2 lines ground the complete source region.

tungsten shields is depicted in **Figure 4**. The shields are laid out in a staircase design above the drain extension region. This staircase shield construction reduces the electric field peaks at the gate side of the drain extension, resulting in an almost ideal constant lateral field distribution [10].

In **Section III**, we give an overview of the RF performance of

the intrinsic LDMOS technology (both 30 and 50 V). The RF measurements are done with load-pull setup for on-wafer and unmatched packaged devices. In the following paragraph, the evolution of performance is shown for both unmatched low power and matched power devices. Furthermore, the key parameters are given and the ruggedness reliability is discussed. In **Section IV**, we show the RF performance of power devices, and in **Section V**, the results of devices in various Doherty implementations are discussed. In **Section VI**, we show an S-band radar device for weather radar applications.

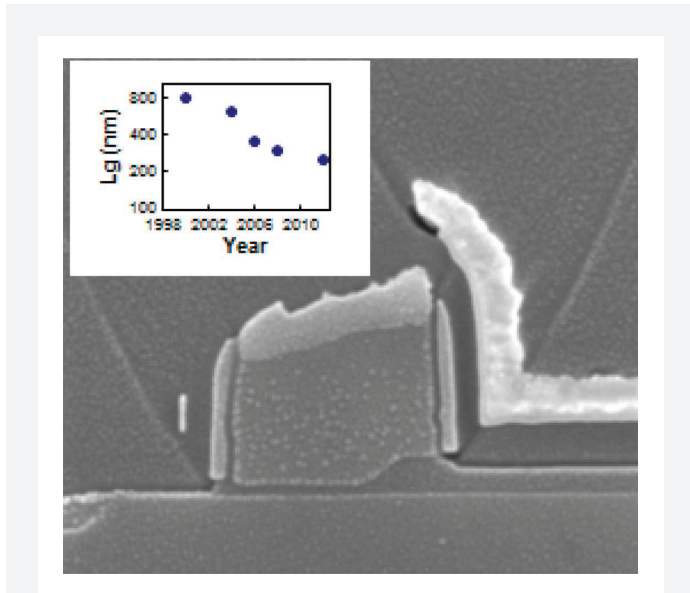


Figure 3: SEM cross-section photograph of the gate region. LDMOS has got a polysilicon gate with cobalt silicide on top. The gate oxide becomes thicker toward the drain side of the gate forming a first field plate. The source connected shield is visible at the right-hand side of the gate. The inset shows the evolution of the gate length.

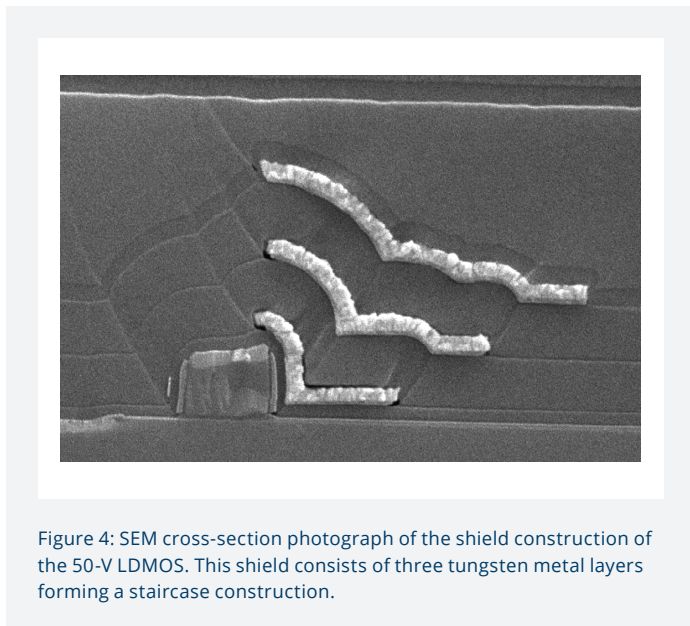


Figure 4: SEM cross-section photograph of the shield construction of the 50-V LDMOS. This shield consists of three tungsten metal layers forming a staircase construction.

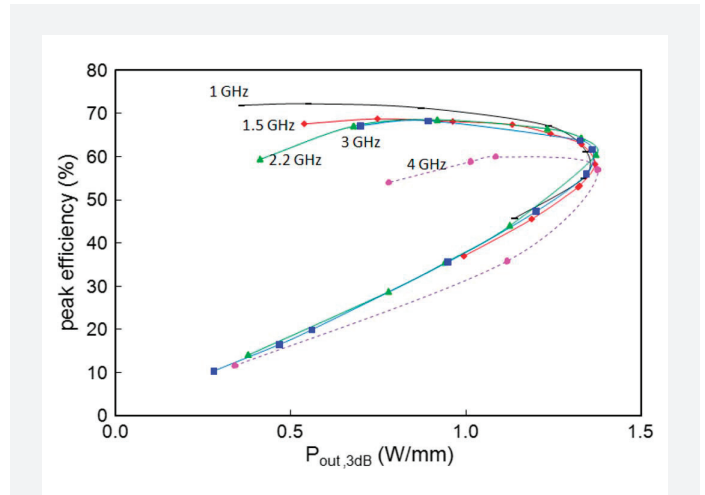


Figure 5: Maximum efficiency versus output power ( $P_{3dB}$ ) contour boundaries for 30-V LDMOS technology. Measurements are done for Ampleon latest 30-V generation with an on-wafer load-pull setup. A pulsed signal with 10 % duty cycle and pulsewidth of 1 ms is used.

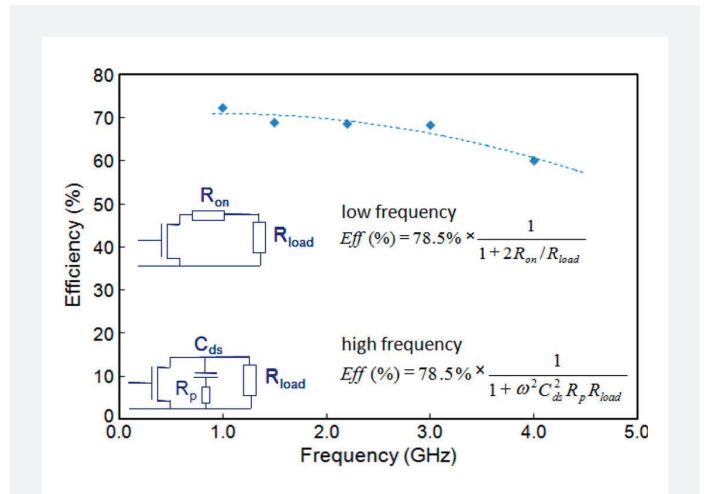


Figure 6: Frequency roll-off of the drain efficiency for 30-V LDMOS. The dotted line represents a loss model [4], which description and equations are depicted in the bottom part of the figure.

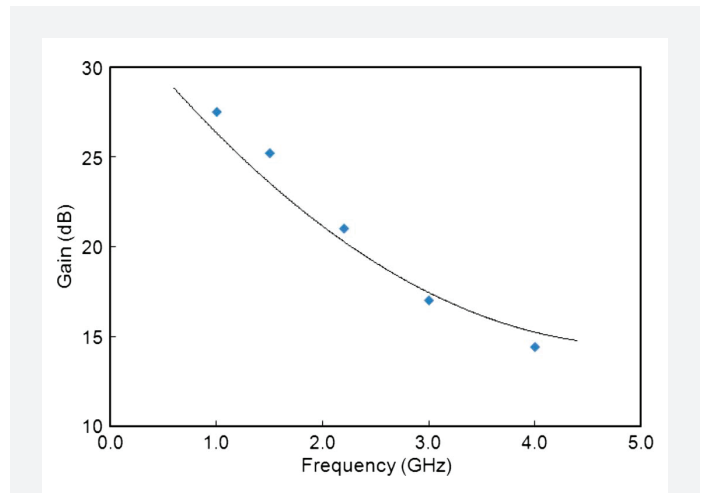


Figure 7: Frequency roll-off of the transducer gain of 30-V LDMOS [8]. The solid line is the -6-dB/octave behavior.

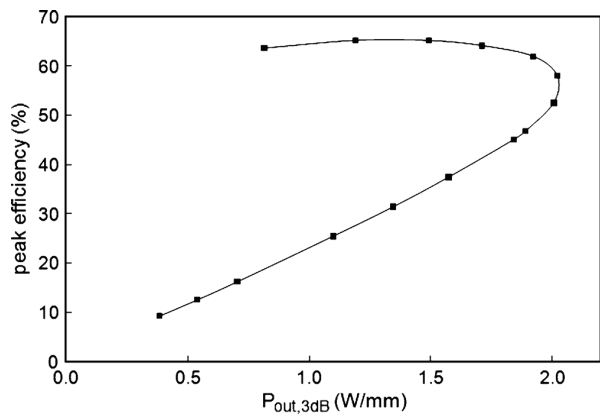


Figure 8: Efficiency-power contour boundaries for 50-V LDMOS technology [10]. Measurements are done at 1 GHz in a load-pull setup with a pulsed signal with 10% duty cycle and pulsewidth of 1 ms.

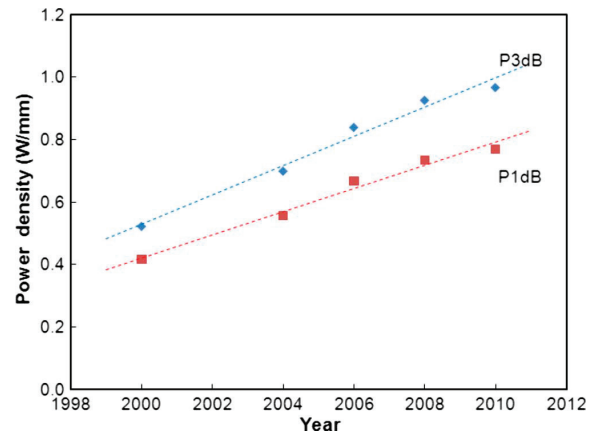


Figure 9: Evolution of power density for 30-V LDMOS. The power at 3-dB gain compression ( $P_{3dB}$ ) and 1-dB gain compression ( $P_{1dB}$ ) are given for a 150-W power device at 2.14 GHz. The devices are biased in class-AB with 5 mA/mm and a 28-V supply voltage. Lines guide the eye. The data up to 2006 was published in [4], while the other data is taken from [19].

### III. INTRINSIC LDMOS PERFORMANCE

#### A. 30-V LDMOS RF Performance

We show pulsed RF measurements from an on wafer load-pull setup for a state of the art 30-V LDMOS technology in **Figure 5** for a frequency range from 1 to 4 GHz. The device measured has a total gate finger length of 4.2 mm and is biased with a supply voltage of 28 V and a drain current of 5 mA per mm gate periphery to achieve class-AB performance. The efficiency versus power trade-off can be made visible by plotting the boundary contours of all measurements obtained by load-pulling the device over all possible load impedance states. From **Figure 5**, we see that the power density of 30-V LDMOS is 1.4 W/mm for the measured frequency range. We show in the next paragraph that this power density can be increased to 2 W/mm for the 50-V technology. The maximum drain efficiency of the same LDMOS is 72 % and shows hardly any roll-off versus frequency up to 3 GHz, where a drain efficiency of 68 % is measured. This efficiency is very close to the theoretical class-B maximum efficiency of 78.5 %. In the frequency range from 3 to 4 GHz, the efficiency falls off to 62 % at 4 GHz. The frequency roll-off is plotted in **Figure 6**, where a loss model fit of the indicated model [4] is included. In this model, the efficiency is limited at low frequency by the series resistance  $R_{on}$  of the LDMOS. The resistance of the drain extension is the dominant contribution to this series resistance. The efficiency roll-off at high frequencies is caused by losses due to the output capacitance.

The gain versus frequency of LDMOS is plotted in **Figure 7**. It follows a 6-dB/octave roll-off as represented by the solid line. The gain at 2 GHz is 21 dB, while the gain at 4 GHz is 15 dB.

#### B. 50-V LDMOS RF Performance

The 50-V LDMOS was developed in 2007, to increase the power density and impedance levels, for broadcast and ISM applications [10], [11]. The efficiency power boundary contours for the 50-V LDMOS are plotted in **Figure 8** as measured by load-pulling at 1 GHz.

The maximum power density is more than 2 W/mm for this 50-V LDMOS. This increase in power density from 1.4 W/mm for 30-V LDMOS to 2 W/mm is predominantly caused by the increase of supply voltage from 28 to 50 V, while the current capability of these technologies is similar. The maximum drain efficiency is also very similar, yielding a value of 67 % at 1 GHz. However, the drain extension needed to accommodate the 120-V break down is roughly two times longer and introduces a larger voltage dependent part of the output capacitance giving rise to more losses at higher frequencies. Therefore, this 50-V LDMOS technology has thus far found its introduction in applications below 1.5 GHz, although a further evolution of reduction in losses can be expected opening the possibilities for 2-GHz (Doherty) applications.

#### C. Evolution of RF Performance

In power applications, LDMOS devices with multiple fingers in parallel are mounted in a ceramic or plastic package. The flange is eutectically soldered to the source backside of the device while the drain and gate are connected via bond wires to the leads. The input and output impedance of a high-power device can be below a few ohm. High-Q input and output matching inside the package is applied to up-transform this impedance level. In **Figure 9**, we show the evolution of the power density at 2.14 GHz for a 150-W packaged LDMOS.

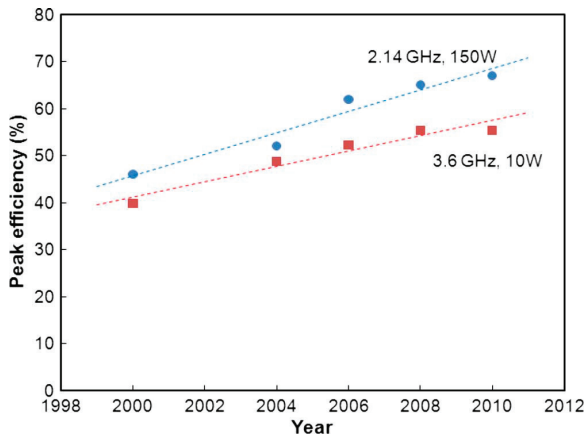


Figure 10: Evolution of the drain efficiency for 30-V LDMOS. The efficiency has increased to 67% at 2.14 GHz for a 150-W device and to 55% at 3.6 GHz for a 10-W device. Lines guide the eye. Data from [4], [8], and [19].

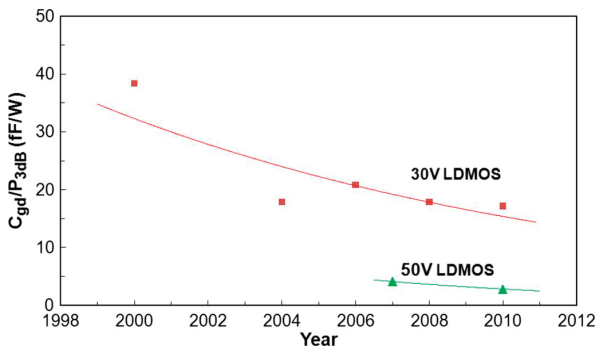


Figure 12: Feedback capacitance ( $C_{gd}$ ) evolution for 30- and 50-V LDMOS at condition  $V_g = 0$  V and  $V_d$  equal to the supply voltage, measured at 1 MHz. The capacitance has been normalized by the 3-dB compression power. Lines guide the eye. Data taken from internal evaluation devices [7], [8], [10], [19].

Over the last decade, the power density has about doubled, achieving more than 1 W/mm for the latest LDMOS generation. This is mainly achieved by increasing the current capability of the LDMOS. The power density is significantly lower than the on-wafer power density of 1.4 W/mm. The evolution of the maximum drain efficiency over the last decade is plotted in **Figure 10**. Both the results for an internally matched 150-W device at 2.14 GHz (corresponding to **Figure 9**) and a 10-W unmatched device at 3.6 GHz are shown.

The peak efficiency in class-AB of the latest generation LDMOS is almost 70 % at 2.14 GHz, close to the on-wafer load-pull result shown in the **Section III-A**. At 3.6 GHz, the drain efficiency is 55 %, a lower value than the on-wafer measurement, indicating that extra losses due to the packaged configuration are present. The evolution of peak efficiency has mainly been achieved by a reduction of the output capacitance losses, which is discussed in **Section III-D**.

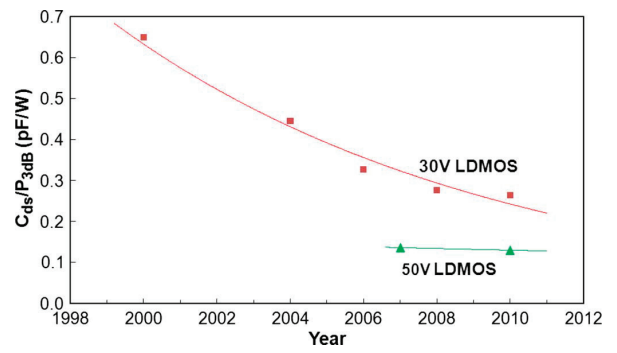


Figure 11: Output capacitance ( $C_{ds}$ ) evolution for 30- and 50-V LDMOS for  $V_g = 0$  V and  $V_d$  equal to the supply voltage, measured at 1 MHz. The output capacitance has been normalized by the 3-dB compression power. Lines guide the eye. Data taken from evaluation devices [7], [8], [10], [19].

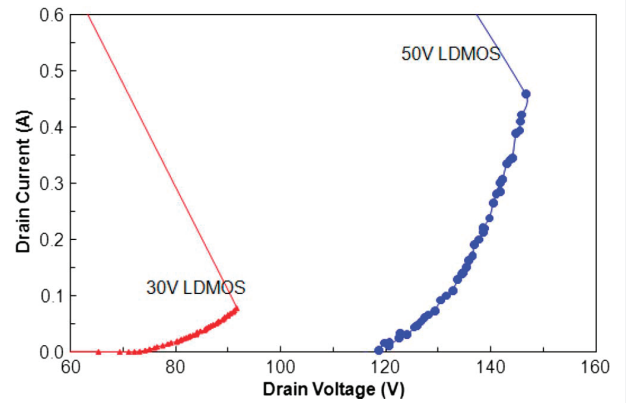
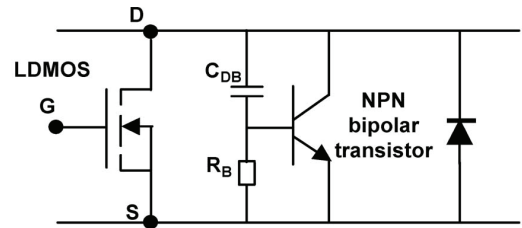


Figure 13: (top) Equivalent circuit of the LDMOS with parasitic NPN bipolar transistor. (bottom) TLP curves for the 30- and 50-V LDMOS [12].

#### D. Evolution of Key Parameters

Key parameters for LDMOS are not only dc parameters, such as on-resistance and the maximum current capability, but also the output, input, and feedback capacitances. These capacitances are especially important because they lead to a frequency-dependent behavior of the RF parameters; the output capacitance is important for the frequency-dependent losses (see **Figure 6**), but also for the bandwidth of the power amplifier (PA). The reduction of the output capacitance is plotted in **Figure 11** for both 30- and 50-V LDMOS.

The output capacitance has been reduced by a factor of 2 in the last decade. This reduction was achieved by scaling down the physical size of the drain contact width and by increasing the power density of the technology. The 50-V LDMOS has a much lower output capacitance for the same power level due to the higher power density of the 50-V device. The input capacitance has been kept constant during the LDMOS evolution by scaling the gate-oxide thickness proportionally to the gate length. The feedback capacitance evolution of 30- and 50-V LDMOS is given in **Figure 12**. A similar large reduction trend is found as for the output capacitance evolution. The feedback capacitance in LDMOS is small compared to the output capacitance: the  $C_{gd}$  value is typically 7 % of the  $C_{ds}$  value. Along with the evolution in output and feedback capacitance the on-resistance has also been improved. The on-resistance of the latest 30-V LDMOS and 50-V LDMOS devices is typically 14 and 29  $\mu\text{m} \cdot \text{mm}$ , respectively.

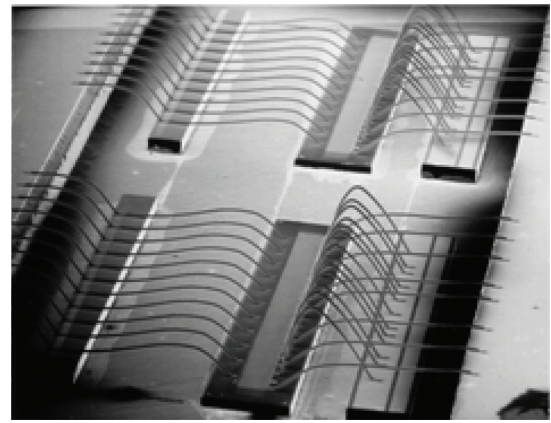
### E. Ruggedness Reliability

Ruggedness is the most important reliability parameter for RF power devices apart from the traditional quiescent current degradation and electromigration robustness. Ruggedness in LDMOS can be correlated to the inherently present parasitic bipolar NPN transistor [12], [13]. Important transistor parameters for triggering are the base resistance ( $R_b$ ) and the drain-to-base capacitance ( $C_{DB}$ ). The corresponding electrical scheme is given in **Figure 13** (top). The drain-source diode clamps the voltage across the LDMOS and the parasitic bipolar and sinks the excess current to the substrate. For large sink currents, however, the drain-source voltage exceeds the diode breakdown voltage and the parasitic bipolar transistor can be triggered.

As a characterization tool for triggering of this bipolar, transmission line pulse (TLP) measurements of the current-voltage characteristics are used [12]. The current and voltage characteristics for the 30- and 50-V LDMOS are given in **Figure 13** (bottom). From this figure, we see that the 30-V LDMOS has a breakdown of 70 V and a snapback voltage of 90 V. The 50-V LDMOS has a breakdown voltage of 120 V and a snapback voltage of 150 V. This snapback behavior has been realized by tailoring the electric fields in the LDMOS. The introduction of the triple stair case shield (see **Figure 4**) plays an essential part in improving the snap-back behavior of the 50-V technology. The extra voltage margin between the breakdown and snapback voltage allows the device to handle large drain voltage swings, as can occur in mismatch conditions, making the device very rugged.

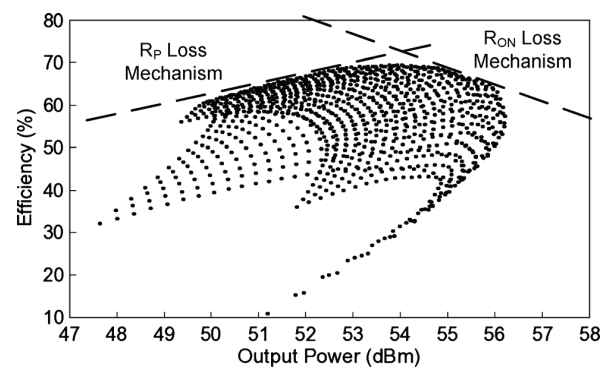
## IV. RF PERFORMANCE OF LDMOS POWER DEVICES

In this section, we describe the performance of LDMOS power devices, i.e., internally matched devices with peak power levels above 300 W. A photograph of typical internal matching structure of LDMOS is shown in **Figure 14**.



**Figure 14:** Photograph of an LDMOS power device with high-Q input and output matching inside the package.

Based on the efficiency power contours, we will show the key parameters for Doherty power amplifiers (DPAs). The load-pull data of a 400-W LDMOS power device is shown in **Figure 15**.

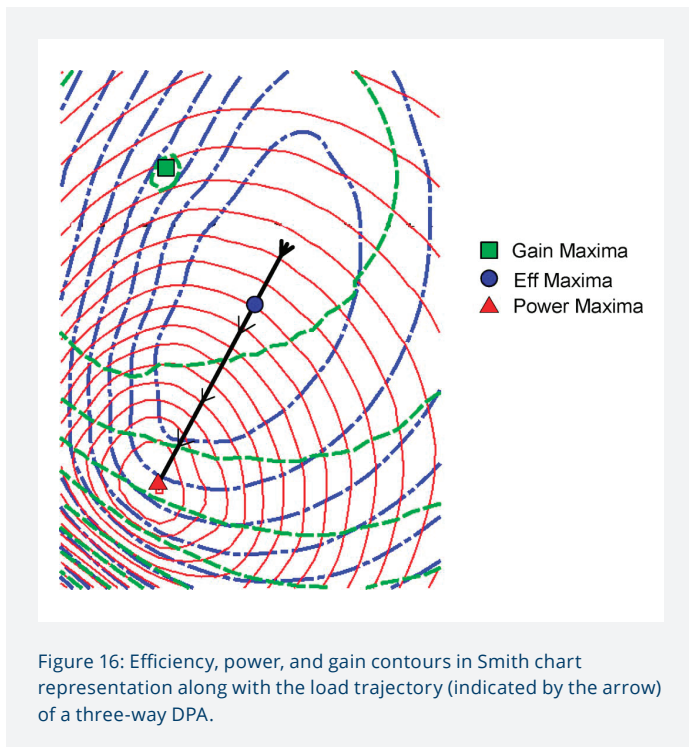


**Figure 15:** Efficiency versus output power ( $P_{3dB}$ ) for a 400-W peak power 30-V LDMOS device at 960 MHz.

The efficiency power data presented in **Figure 15** is obtained by sweeping the output load and input power of the PA device. The higher power levels usually correspond to low output loading conditions, whereas lower power levels are the result of higher output loading conditions [14]. Moreover, the data presented in **Figure 15** indicate that the PA device has maximum efficiency of 70 % at an output power of 200 W, which is around 3 dB lower than the maximum power of the device. Moreover, at power levels less than 200 W, the device shows continuous decrease in efficiency. The reason for such behavior lies in the loss mechanisms shown in **Figure 6**. At higher power levels, the dominant loss mechanism is  $R_{ON}$ , whereas at lower power levels, the loss is dominated by  $R_p$  mechanism.

Apart from the efficiency and power level of the LDMOS power device, the location of the power, efficiency, and gain contour

maximum is also very important for high-efficiency concepts like the DPA. In **Figure 16**, we show the efficiency, power, and gain contours of the 400-W LDMOS device in the Smith chart representation. The input of the device is conjugately matched and class-AB conditions are enforced (by shorting the harmonics) while obtaining the data presented in **Figure 16**.



In an ideal PA device, the points (loads) for maximum power, efficiency, and gain are located along a straight line; however, in real PA devices, these points make a triangle (see **Figure 16**). The main reason for the separation of these contours in LDMOS devices (under class-AB bias) is the feedback mechanism, e.g., due to the feedback capacitance  $C_{gd}$  and source inductance  $L_s$  [14].

## V. LDMOS DOHERTY IMPLEMENTATIONS

### A. DPAs Operation

The DPA is a very old concept to increase the average efficiency of the microwave transmitter. It was initially proposed in 1936 [15] to improve the efficiency of AM broadcast transmitters. It works on the principle of active load modulation of a PA device (main device) by injecting current from a second PA device (peaking device) into a common load. In the recent years, there is significant advancement in Doherty design techniques, e.g., multipath DPAs [9], [14], [16], [18], which have led to an increase of average efficiency of W-CDMA base stations. The details of the DPA operation are given in [9], [14], and [16]; therefore, in this paper, we focus more on the impact of the device parameters on the performance of the DPA.

A DPA is normally used to amplify the modulated signals having high peak-to-average ratios (PARs), which means that most of the time the DPA operates at the power levels that correspond to the average power of the output signal. At those power levels, the main PA device in the DPA configuration operates alone at high loading conditions (in order to increase the terminal voltages, and therefore, the efficiency). Hence, the efficiency of the main device at back-off power levels with increased loading conditions (e.g.,  $2 \times R_{opt}$  for a two-way and  $3 \times R_{op}$  for a three-way DPA) is very important for the average efficiency of the DPA.

From **Figure 15**, we see that the LDMOS peak efficiency of close to 70 % is situated around a power level of 200 W, which is at 3-dB back-off. This makes this device favorable for being used as the main device in the two-way DPA, as in the two-way DPA, the main device is subjected to 3-dB back-off once the power of the full PA is backed off by 6 dB.

Similarly, if the device is used as a main device in three-way DPA configuration, the load-pull data of **Figure 15** shows 65 % efficiency at 4.7-dB back-off power levels (134 W), which corresponds to the 9.6-dB back-off of the total PA.

In addition to the efficiency, the gain of an RF PA is also very important for DPA. The gain of a DPA is less than the intrinsic gain of the PA transistor and depends on following three parameters:

1. Gain of the intrinsic device;
2. Configuration of the DPA (e.g., two- or three-way);
3. Change of gain along the load trajectory of the DPA.

The last parameter depends on the location of the contour maxima of power, gain, and efficiency of the device, which should lie along the load-line trajectory of the main device in the DPA configuration, as shown in **Figure 16**.

In view of above considerations, efforts have been made to reduce the losses of the LDMOS transistors in order to improve its efficiency, especially in three-way DPA [16], [18] configurations. In addition to that, considerable effort has also been put to reduce the feedback mechanisms in the device, as well as in the package to improve the gain performance of the device in the DPA configuration. The result is an optimized high-efficiency high-power PA device technology suitable for two- and three-way DPAs [9].

### B. 30-V LDMOS DPAs Results

In **Figure 17**, we show a photograph of a three-way DPA board designed at 1.8 GHz. This amplifier is based on the three-way Doherty concept [18] and contains three 250-W LDMOS

devices. The top device is biased in class-AB and acts as a main device and the bottom two devices are biased in class-C mode and act as peaking devices. The power at the input is split with a passive power splitter. The gate biasing of the devices ensures that only the main PA device is active at deep PBO levels ( $< 10$  dB), while peaking 1 (middle device) and peaking 2 (bottom device) turn on at medium ( $6 \text{ dB} < \text{PBO} < 10$  dB) and high power levels, respectively. The output power of the devices is combined with a three-way power combiner.

The instantaneous efficiency of this three-way LDMOS DPA is shown in **Figure 18**.

The DPA has a peak power of  $> 700$  W and an instantaneous efficiency of 50 % at 7.5-dB PBO. This results in an average efficiency of 47 % for modulated signals having high PARs, e.g., MC-GSM and third-generation (3G) WCDMA. The spectrum of an MC-GSM signal after DPD is shown in **Figure 19**. These are obtained using Opticron DPD setup. The wide RF and video bandwidth of the DPA allows to correct the linearity better than -65 dBc for an average output power of 120 W, with a signal PAR of 6.2 dB and 20-MHz signal bandwidth.

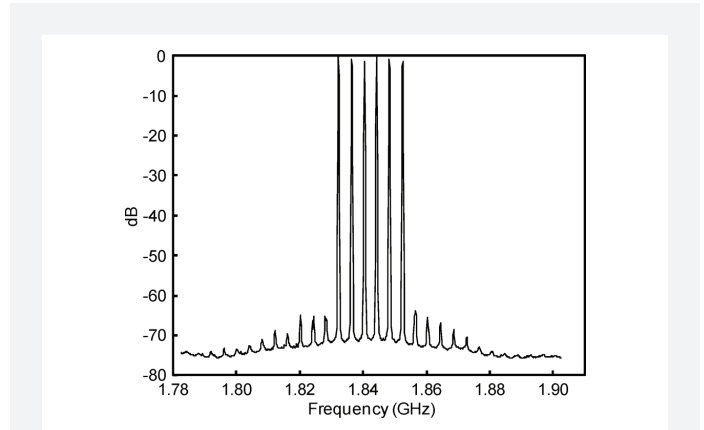


Figure 19: Output spectrum of three-way LDMOS DPA with 6C-GSM signal after applying pre-distortion.

An overview of the performance of various three-way DPAs is given in **Table I**. The efficiency of the DPAs decreases with operating frequency, but it is still possible to achieve average efficiencies close to 50 % up to 2 GHz and 40 % at 2.7 GHz. A DPA based on 50-V LDMOS is also given in **Table I**, showing comparative performance at 1 GHz.

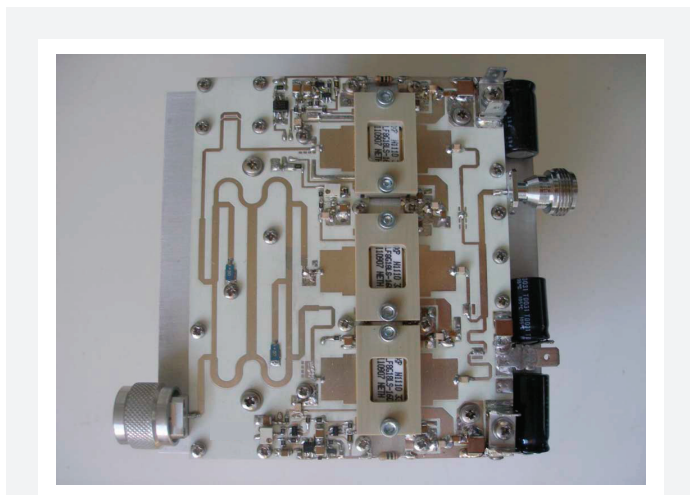


Figure 17: Photograph of a 700-W peak power three-way DPA, designed for 1.8 GHz.

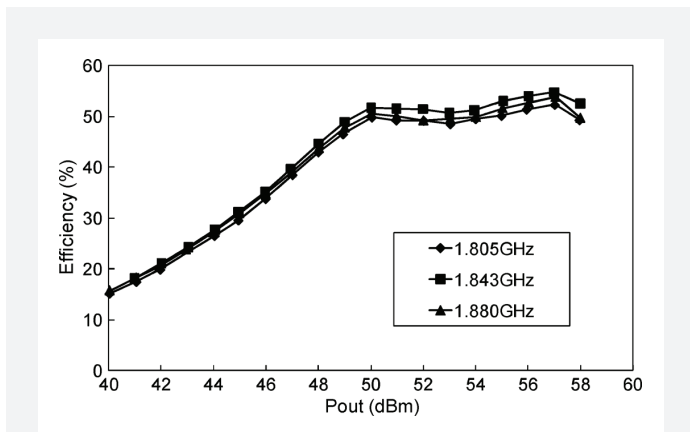


Figure 18: Measured efficiency versus output power of the three-way DPA designed for 1.8 GHz [18].

Description Peak Power, $V_{\text{supply}}$	$f$ (GHz)	Gain (dB)	Eff, ( $P_{\text{avg}}$ ) (%), (W)	ACPR (dBc)
800 W, 32 V [18]	0.94	16	51 (125 W)	$< -63$
550 W, 50 V [18]	0.94	17	49 (80 W)	$< -60$
630 W, 28 V [20]	0.925	17.6	45 (112 W)	$< -50$
700 W, 32 V [18]	1.80	16.5	47 (120 W)	$< -65$
630 W, 32 V [18]	2.14	15	47 (100 W)	$< -60$
446 W, 28 V [20]	2.14	14.3	48 (70 W)	$< -55$
630 W, 32 V [18]	2.65	13.5	40 (80 W)	$< -58$
100 W, 28 V [20]	2.60	14.35	40.9 (20 W)	$< -54$

Table I: Performance of several 3-way Doherty Power Amplifiers designed for different frequencies. Seven DPAs are based on 30 V LDMOS and one DPA is based on 50 V LDMOS. Peak power, gain, efficiency at average power and ACPR values after applying pre-distortion are given.

### C. 50-V LDMOS Doherty Results

The 50-V LDMOS technology allows higher RF voltage swings at the drain of the PA devices resulting in increased power density and higher values of required output loads. This high load impedance results in lower quality (Q) factor output matching network, thereby decreasing the losses and increasing the fractional bandwidth of the output match significantly [17]. Furthermore, 50-V LDMOS technology allows a compact output matching network, and therefore a more dense packing of the power, resulting in a smaller packaged device. In **Figure 20**, we show the frequency response from a broadband 800-960-MHz 400-W LDMOS DPA.



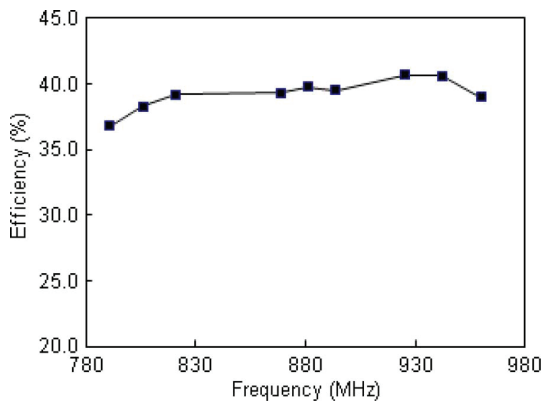


Figure 20: Measured efficiency at 8-dB back-off of a broadband 50-V LDMOS two-way DPA.

The gain is typically 20 dB and the efficiency at 8-dB back-off, as required for DVB and MC-GSM signals, is 37 % - 42 % over the band, which is a 10 % improvement compared to class-AB operation.

## VI. LDMOS AT S-BAND APPLICATIONS

The evolution of LDMOS has not only resulted in the extension of LDMOS to higher power levels, but has also opened the possibilities for LDMOS in 3-4-GHz frequency range. Typical applications for these frequencies are S-band radar and WiMAX and LTE bands for base station. As an example, we show a 40-W S-band radar device for weather radar applications for 2.7-3.3 GHz in **Figure 21**. The high intrinsic gain and low output capacitance of the current LDMOS technology allows to design with a gain of 13 dB over the full band (2.7-3.3 GHz) with an efficiency more than 50 %.

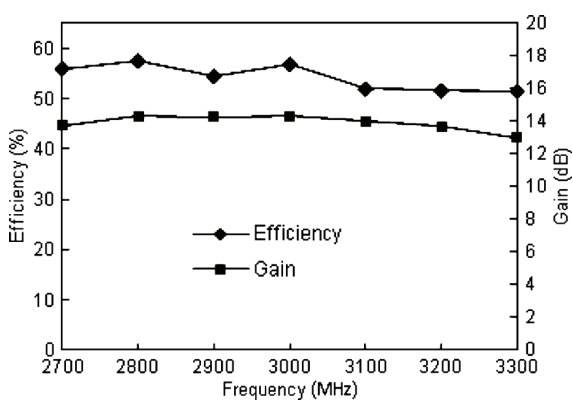


Figure 21: The efficiency and gain performance of an S-band PA at output power of 40 W made with 30-V LDMOS technology.

## VII. CONCLUSION

We have given SEM device cross sections of state-of-the-art 30- and 50-V LDMOS technology showing the special gate construction and the staircase shield construction. The intrinsic device performance has been presented for a frequency range of 1-4 GHz and the key device parameters were discussed. Furthermore, the performance of power devices and of several three-way Doherty amplifiers has been shown. Average efficiencies close to 50 % can be achieved with three-way Doherty LDMOS amplifiers at 2 GHz in combination with high gain and low adjacent channel power ratio (ACPR) after pre-distortion. LDMOS is also suitable for broadband high-efficiency Doherty amplifiers, as shown for a 50-V LDMOS DPA. Finally, an S-band weather radar LDMOS amplifier was presented having 13 dB of gain and more than 50 % efficiency. New ideas related to device technology and electromagnetics are being applied to the LDMOS technology to open up even more advanced concepts, like N-way DPAs and switching mode amplifiers.

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## DR. IR. S. J. C. H. THEEUWEN

Steven Theeuwen was born in Nuth, The Netherlands, in 1970. Steven holds a M.Sc. degree in physics from Eindhoven University of Technology, The Netherlands, and a Ph.D. degree in physics from Delft University of Technology, The Netherlands. Steven joined the Marketing, Strategy & Innovation group of Philips Semiconductors Nijmegen, The Netherlands, in 2000 as a device physicist to develop high-frequency transistors in Si and III-V materials. Currently he is working for Ampleon Netherlands B.V. (spun-out of NXP in 2015, spun-out of Philips in 2006), The Netherlands, in the RF innovation group developing highly efficient LDMOS devices for base station, broadcast and microwave applications. Among his device physics research subjects are the hot carrier injection degradation, ruggedness, power density and loss mechanisms for RF power LDMOS devices. Steven has published more than thirty scientific papers and (co-) authored more than a dozen patent applications.

