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Efficiency Improvement of LDMOS Transistors for Base Stations: Towards the Theoretical Limit

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ABSTRACT

We present the evolution in LDMOST technology of the last decade, leading to a present 32 percent efficiency value for a two carrier W-CDMA signal with -37 dBc IM3 and discuss future prospects to increase the performance even further. The achieved reduction of parasitic elements currently opens the way for system concepts such as high efficiency classes and Doherty type concepts.

INTRODUCTION

In base stations for personal communication systems (GSM, EDGE, W-CDMA), RF power amplifiers are key components. For these power amplifiers, RF Laterally Diffused MOS (LDMOS) transistors are the standard choice of technology because of their excellent power capabilities, gain, linearity and reliability. To meet the demands imposed by new communication standards, the performance of LDMOS is subject to continuous improvements **[1,2,3]**. Wideband CDMA (W-CDMA) requires linear operation of the PA, which means operating the amplifier sufficiently far in back off reducing at the same time the efficiency of the PA. Nowadays much attention is paid to improve this trade-off between linearity and efficiency on device and system level.

In this paper, we present the evolution obtained in LDMOST technology over the last 6 years; the continuous improvements made in LDMOS technology which led to a present 32 percent W-CDMA efficiency world-record value, and the future prospects to increase the performance even further. Attention will be paid to the maximum achievable theoretical limit.

ACHIEVED PERFORMANCE TRENDS

In **Figure 1** the realized increase in drain efficiency with a 2 carrier W-CDMA signal at -37 dBc IM3 is shown for the LDMOST technology generations with the feature size (gate-length) in brackets. The improvement rate is almost 2 percent point per year. The increase in efficiency has been accompanied by an improvement in other relevant parameters, as shown in **Table 1** with the higher power gain as most important one. **Figure 2** shows the W-CDMA performance at 2 GHz of the latest devices. The hot carrier degradation as characterized by Idq-degradation extrapolated to 20 years has been decreased significantly from year 2000 on and kept well under control after that **[4]** (**Figure 3**). The power density has been increased with 60 % to a value of 0.66 W/mm. For smaller devices the value approaches 1.0 W/mm.

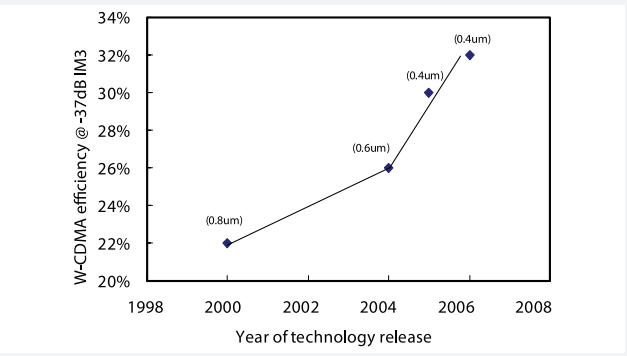


Figure 1: Realized W-CDMA efficiency at 2.14 GHz versus time for 100 W LDMOS-transistors. The used gate-length is shown in brackets.

	2000	2004	2005	2006
Pout (W) @P-1dB	90 W	100 W	100 W	100 W
Wg (mm)	3 x 72 mm	2 x 90 mm	3 x 50 mm	3 x 50 mm
Power density (W/mm)	0.416	0.55	0.66	0.66
Gain @ 2GHz (dB)	12.5 dB	13.5 dB	18 dB	18.5 dB
Peak PAE (%)	45 %	50 %	60 %	60 %
Eff (-37dBc 2c-WCDMA)	22 %	26 %	30 %	32 %
Idq degr (%)	25 %	5 %	3 %	2 %
Rth (K/W)		0.75	0.5	0.5

Table 1: Achieved improvement of relevant device parameters.

LDMOS PROCESS AND EFFICIENCY ANALYSIS

The performance boost has been primarily accomplished by a rigorous reduction of output losses of the LDMOST attaining the device architecture of **Figures 4** and **5**. **Figure 6** shows a TEM cross-section of the LDMOST showing the gate and shield in more detail. The last generations are processed in a 8-inch CMOS-fab capable of lithography down to 0.14 um where the LDMOST process is derived from C075 CMOS (0.35um gate) process with LOCOS isolation.

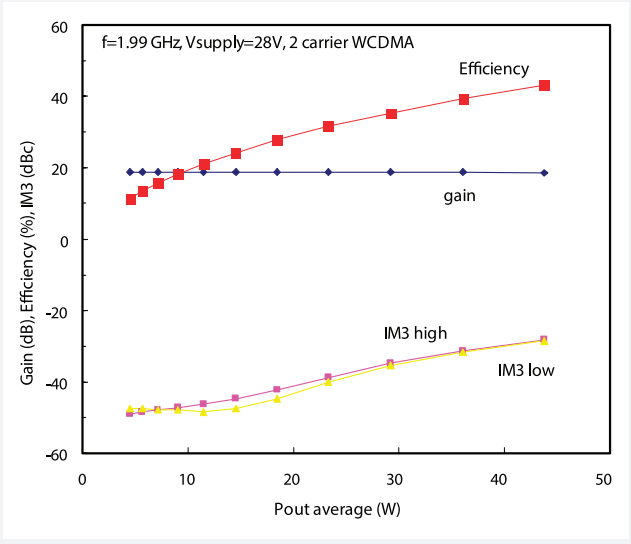


Figure 2: Latest 2c-WCDMA performance.

Additions to this process are the source plug to the substrate, CoSi2 gate silicidation, tungsten shield, thick 2.8 µm fourth AlCu metallization layer and p-well and drain-extension implantation optimization.

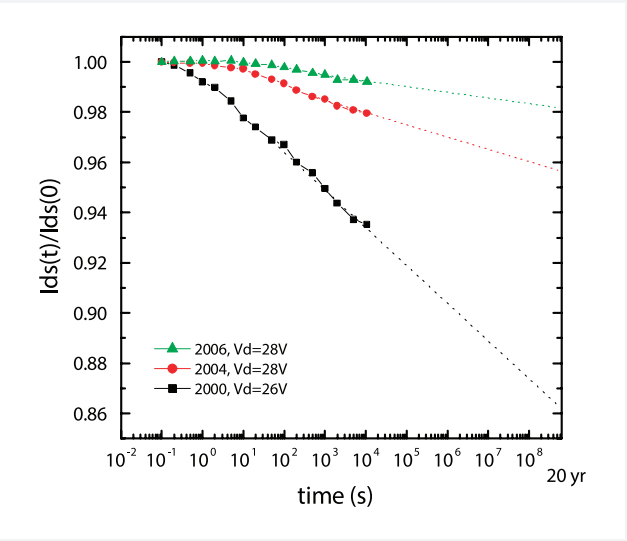


Figure 3: Idq degradation versus time showing that the reliability is well under control.

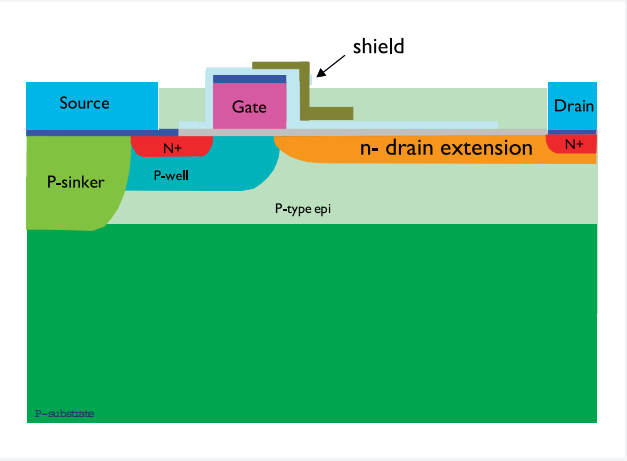


Figure 4: Schematic cross-section of state of the art LDMOST.

Figure 7 shows the two dominant loss mechanisms for the LDMOST. The first one is due to the on-resistance, which is determined by the drain-extension and is frequency independent. The second one, which is frequency dependent, is due to loss in the output capacitance where the resistive part is a combination of resistance of the drain-extension and substrate resistance. Analysis of large signal performance at various frequencies and devices optimized at several supply voltages shows, see **Figure 8**, that above 10 V the peak efficiency becomes frequency dependent. Hence, parallel output losses are the dominant mechanism for the base station transistors with a supply voltage of 28 V. At 1 GHz almost the theoretical class-AB efficiency of 78.5 % is reached.

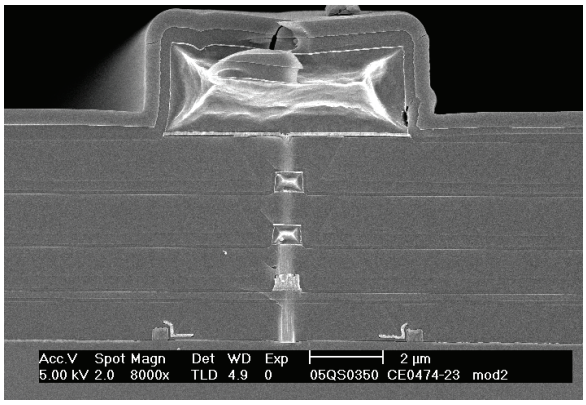


Figure 5: SEM cross-section of state of the art LDMOST.

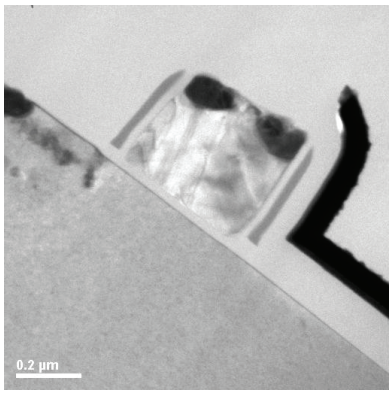
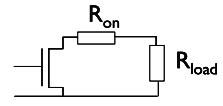
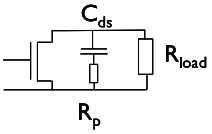


Figure 6: TEM cross-section of the gate region.

For low voltage the efficiency is dominated by series losses due to the on-resistance only. The gain as function of supply voltage and frequency is shown in **Figure 9**. The performance at 28 V and 3.5 GHz has been improved to such an extent that LDMOS is nowadays the common choice for WiMAX applications.



$$Eff\ (\%) = 78.5\% \cdot \frac{1}{1 + 2R_{on}/R_{load}}$$



$$Eff\ (\%) = 78.5\% \cdot \frac{1}{1 + \omega^2 C_{ds}^2 R_p R_{load}}$$

Figure 7: Two loss mechanisms in LDMOST denoted by series losses (top picture) and parallel losses (bottom picture).

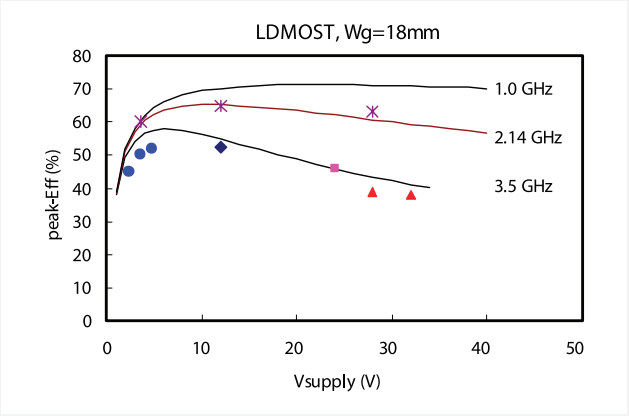


Figure 8: Peak efficiency versus supply voltage at three frequencies showing the dominance of parallel losses above 10 V supply voltage. Markers are experimental results and solid lines are theoretical curves. The LVLDMOST data with a supply voltage of 2.4, 3.0 and 4.8 V where taken from reference [5].

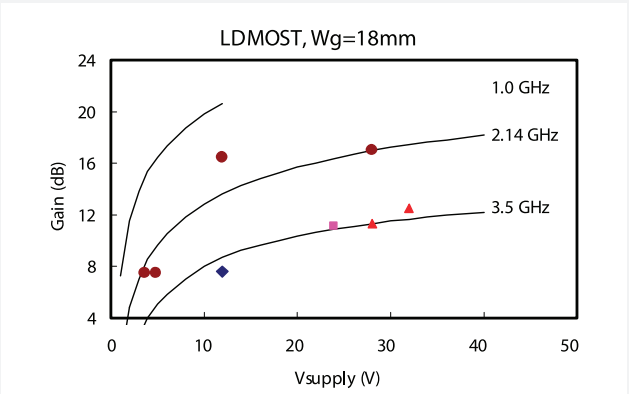


Figure 9: Gain versus supply voltage at three frequencies. Markers are experimental results and solid lines are theoretical curves.

Despite the fact that the cut-off frequency increases with decreasing supply voltage the gain rapidly diminishes. This has to do with the reduction of the load resistance for lower supply voltages.

TOWARDS HIGH EFFICIENCY

Having identified the main loss-mechanisms, a continuous effort has been undertaken to reduce the capacitance and onresistance significantly. **Figure 10** shows the output capacitance and on-resistance per unit of gate periphery (mmWg) as function of technology generation. The on-resistance has been reduced by optimizing the drain extension, where the introduction of the shield (in 2004) made it possible to improve the trade-off between hot-carrier degradation and on-resistance. The lower output-capacitance was made possible, among other measures, by a rigorous reduction of the drain-junction area without sacrificing electromigration performance **[4]** using the back-end process depicted in **Figure 4** and **5**.

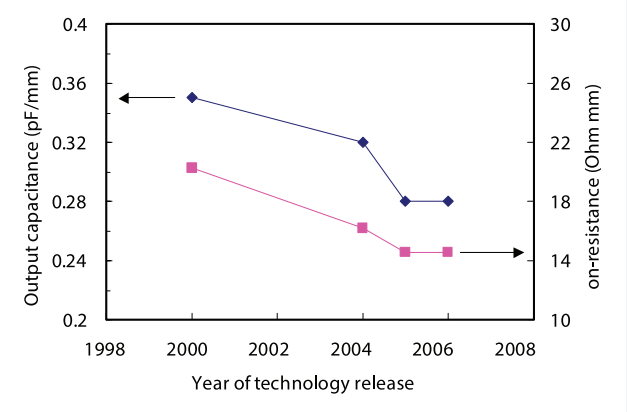


Figure 10: Improvement in output capacitance and on-resistance.

Table 2 shows the values for a given output power. Due to the increased power-density the total on-resistance for a 100 Watt transistor did not change but the output capacitance has been reduced with more than 40 % leading to the achieved improved efficiency.

	2000	2004	2005	2006
Pout (W) @P-1dB	90 W	100 W	100 W	100 W
Wg (mm)	3 x 72 mm	2 x 90 mm	3 x 50 mm	3 x 50 mm
Power density (W/mm)	0.416	0.55	0.66	0.66
gm (S)	6.66	8.65	10.83	10.8
Ron (Ohm)	0.094	0.090	0.097	0.097
Cout (pF)	75.0	57.0	42.5	42.5

Table 2: On-resistance and output capacitance for devices with similar output power.

Increasing the efficiency via reduction of the losses is not the only way. In **Figure 11**, the W-CDMA efficiency is plotted against the back-off power necessary to achieve the desired linearity (markers). Lines are 1-tone efficiency curves for several degrees of losses and the ideal class-AB curve without losses (dashed line). The higher efficiency of the 2006 generation has been reached by lowering the back-off level instead of by going to a different efficiency line with fewer losses. Making the LDMOS more linear has made this possible. Optimizing the harmonic impedances has also great influence on the linearity **[6,7]**. **Figure 11** also shows a point at 39 % that is considered to be the highest efficiency possible for a conventional class-AB power amplifier. Here the device has such a linearity that the distortion is due to hard clipping only. A back-off level of -6dB is than required to meet the EVM specification.

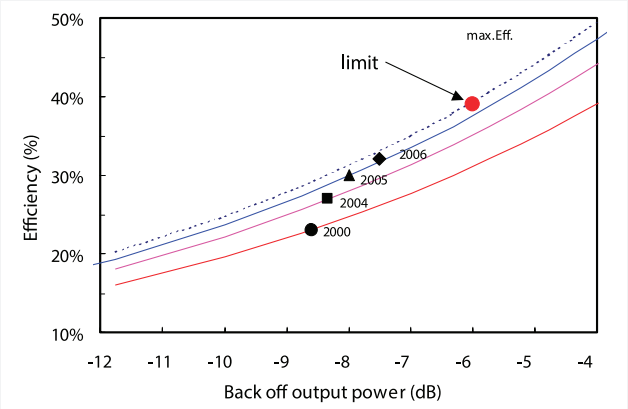


Figure 11: Efficiency curves (solid lines) for various output losses and ideal class-AB efficiency without losses (dashed line) versus back-off level. Markers are the results of the technology generations showing the path taken towards higher efficiency.

CONCLUSIONS

To conclude, the efficiency improvement as shown in the last years can still be continued until the theoretical limit of 39 % has been reached. Although the improvement via loss reduction has almost come to an end, the improvement via linearity has just been started. Moreover, because the LDMOST becomes more and more an ideal transistor not hampered by its parasitics, system concepts such as high efficiency class operation, Doherty type concepts and DPD start to work better. So, higher and faster efficiency improvements are expected and already obtained (see **Figure 12**) using these concepts.

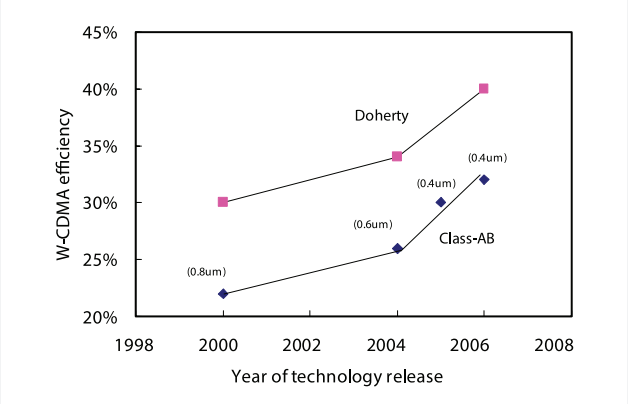


Figure 12: As figure 1 but complemented with efficiency results of Doherty PA's using the same technology.

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