AMPLEON

LDMOS Ruggedness Reliability

S.J.C.H. Theeuwen, J.A.M. de Boet, V.J. Bloem, W.J.A.M. Sneijers
Ampleon, Halfgeleiderweg 8, 6534 AV, Nijmegen, The Netherlands
Email: steven.theeuwen@ampleon.com

Original publication: Microwave Journal, technical feature, April 2009, pp. 96-104 (2009)

Abstract - We give an overview of 28-42-50 V LDMOS technologies and discuss the ruggedness reliability in addition to the RF performance. Various ruggedness tests are presented like pulsed snapback measurements, VSWR and video bandwidth tests.

I. INTRODUCTION

RF power amplifiers are key components in base stations, broadcast transmitters, ISM applications and microwave applications. They can handle a wide range of signal types like GSM, EDGE, W-CDMA, Wimax, and DVB-T. RF Laterally Diffused MOS (LDMOS) transistors have been the choice of technology for these power amplifiers since more than a decade, because of their excellent power capabilities, gain, efficiency, cost and reliability.

Ruggedness is one of the most important reliability parameters for RF power transistors. Ruggedness is the ability to withstand a stress condition without degradation or failure. One way to characterize ruggedness is by measuring the voltage standing wave ratio (VSWR) in a RF test fixture with a defined mismatch at the output. The design of the test fixture and the matching of the transistor are critical for the result of the VSWR test. LDMOS transistors are optimized to withstand a certain power and voltage, and the process is engineered for the best trade-off between RF performance and ruggedness.

In this paper we show RF LDMOS devices, which combine very good ruggedness with state of the art RF performance. We will elaborate about the ruggedness tests we have developed to meet today's product ruggedness criteria.

II. RF LDMOS Technologies (28-42-50 V)

Ampleon has developed a base station RF LDMOS technology **[1,2]** and high voltage RF LDMOS technologies **[3]**. The base station technology operates at supply voltages around 28 V, while the high voltage technology can be used at 42 and 50V. Both LDMOS are processed in an 8-inch CMOS-fab capable of lithography down to 0.14 um, where the LDMOST process is derived from C075 CMOS (0.35 um gate) process with LOCOS isolation. Additions to this C075 process are the source sinker to the substrate, CoSi2 gate silicidation, tungsten shield, and mushroom-type drain structure with thick multi-layer AlCu metallization. A schematic picture of LDMOS is shown in **Fig. 1**.

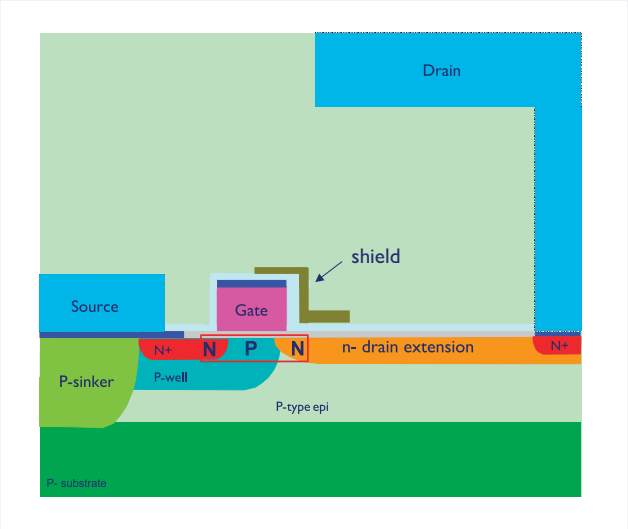

Figure 1: Schematic picture of LDMOS technology. The inherently present NPN parasitic bipolar transistor is indicated in the red square

The RF performance of the base station LDMOS is state of the art, and used in a wide range of applications like GSM, W-CDMA and Wimax, as presented in **[1]**. Recently we have developed high voltage (42-50 V) LDMOS technologies **[3]** for high power devices at frequencies below 1 GHz. Typical RF performance of the high voltage technology at 470-860 MHz (UHF) and 225 MHz (VHF) is shown in **Fig. 2** and **3**, respectively. The UHF device delivers 75-110Wavg at 42 and 50 V, respectively. The broadband gain is 19 dB and the efficiency is 30-32 % with a CCDF of 8 dB.

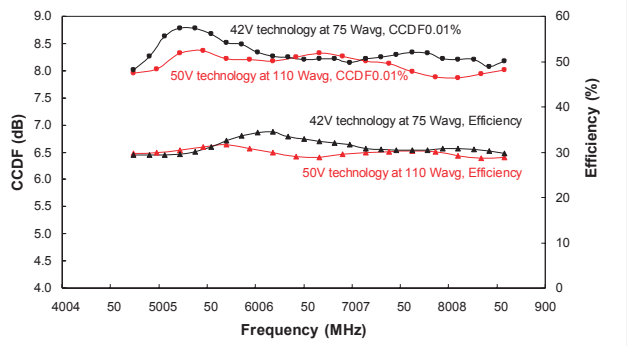

Figure 2: RF performance of the 42V and 50V LDMOS technology devices at 470-860 MHz for an 8k DVB-T signal

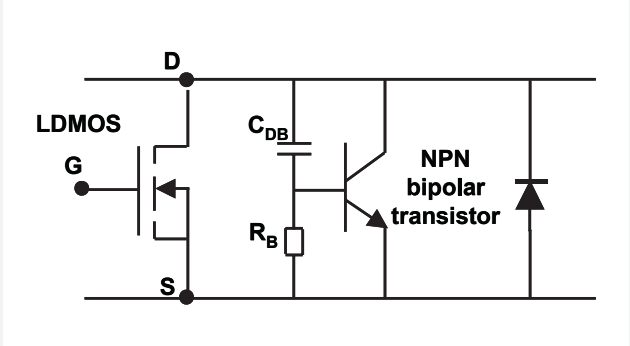

Figure 4: Electric representation of the LDMOS and the inherently present parasitic bipolar transistor and drain-substrate diode

The VHF device (**Fig. 3**) delivers 1300 W power (P1dB) at 50 V with a peak efficiency of over 70 % and a gain of 24 dB.

Both devices have been tested to be very rugged and capable of handling high voltage and high power over a wide band of extreme mismatch conditions. In general, at low frequencies more ruggedness is required of devices. This is partly due to the higher harmonic content at frequencies much lower than the cut-off frequency. Also the signal type is important for ruggedness, sharply varying pulse signals with a steep rise time being more severe for ruggedness. For this reason, LDMOS technologies have been hardened under the most stringent ruggedness tests during development, and in particular the 50 V high voltage technology.

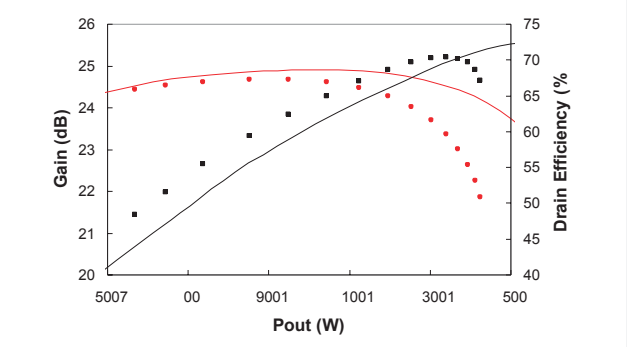

Figure 3: RF performance of a 50V LDMOS technology device at 225 MHz

III. PARASITIC BIPOLAR TRANSISTOR

Inherent to the LDMOS device is the presence of a parasitic bipolar transistor. This NPN bipolar transistor is indicated in **Fig. 1**. The corresponding electrical scheme is given in **Fig. 4**, showing besides the LDMOS the presence of the parasitic NPN bipolar transistor and the drain-substrate diode. The drain-source diode clamps the voltage across the LDMOS and the parasitic bipolar and sinks the excess current to the substrate. For large sink currents, however, the drain-source voltage exceeds the diode breakdown voltage and the parasitic bipolar transistor can be triggered.

This triggering of the parasitic bipolar transistor is essential for the occurrence of a ruggedness failure. To make the bipolar transistor robust for a triggering event, the bipolar of the LDMOS has been characterized and optimized. Important transistor parameters for triggering are the base resistance (RB), the gain of the bipolar, and the amplitude of the base current. As a characterization tool for triggering of this bipolar, we use short pulse (50 ns to 200 ns) measurement of the current-voltage characteristics. An impedance transmission line is used as a pulse source to create a rectangular pulse. The desired voltage is applied via a DC power supply and then quickly discharged with a low inductance switch. The current and voltage are measured with a memory scope during the discharge. The snapback in the I-V curve is measured, which gives insight in the device properties of the DUT. The characterization is done on wafer with small (test) devices in a 50 Ω commercial available set-up. Power RF devices cannot be used since the setup is not able to generate enough current. This is a fast and adequate evaluation of device and process changes on ruggedness without influence of test circuits and matching conditions.

IV. RUGGEDNESS CHARACTERIZATION

During the development of RF-LDMOS processes, we have continuously improved the intrinsic ruggedness of the parasitic bipolar transistor of the RF power LDMOS devices.
The base resistance is important for ruggedness as can be seen from the electrical representation in **Fig. 4**. In the processing we have varied the base resistance of the parasitic bipolar transistor to lower the voltage drop between base and emitter. In **Fig. 5** we see the pulsed current voltage characteristic of base station RF LDMOS devices with different base resistances. Around the (diode) breakdown voltage of the transistor (in this example around 73 V) the drain current starts to increase, and at 82 V snapback occurs. This snapback voltage and snap back current are the two parameters, which are a measure for the intrinsic RF-ruggedness. By process optimising the base resistance we have succeeded in doubling the snapback current resulting in a better VSWR of the corresponding power devices.

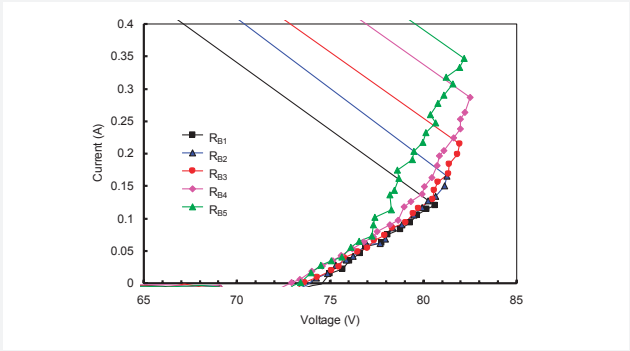

Figure 5: Pulsed current voltage characterization of several devices with different base resistance

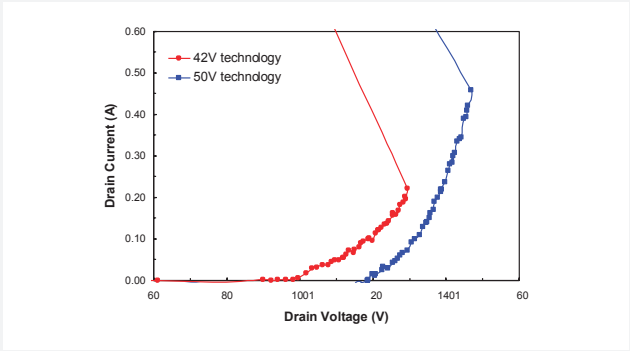

Figure 7: Pulsed current voltage measurements of the high voltage broadcast LDMOS for different epi thickness

Furthermore we have optimised the capacitance between the base of the bipolar and the drain (C_{DB}) by engineering the drain extension of the LDMOS. In **Fig. 6** we show measurements for different drain engineering (DE) variants. At 83-98 V the parasitic bipolar of the device is triggered, causing a snapback in the curve. We see that this snapback improves by DE variation, resulting in a more rugged device. This is confirmed by VSWR measurements done at power devices. The best devices can tolerate a 10 V higher supply voltage for the same power level and VSWR of 10:1.

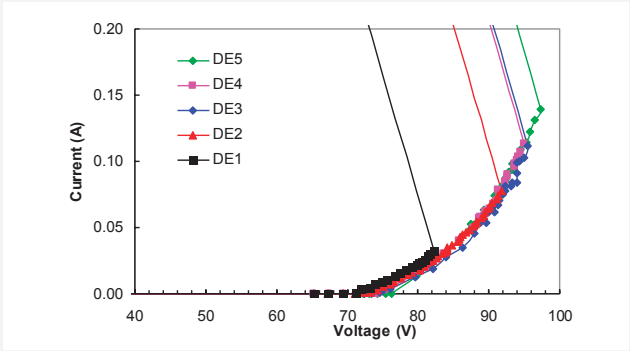

Figure 6: Characterization of devices with different drain engineering variants at Vgs=0V

From this rugged base station LDMOS technology we have derived super-rugged high voltage (42-50 V) RF LDMOS technologies for broadcast applications up to 1 GHz and for VHF and ISM applications, where most stringent reliability criteria are demanded.

Fig. 7 shows that the breakdown voltage of these high voltage technologies is increased compared to the 28 V base station technology. More importantly also the snapback voltage is significantly larger, resulting in values of 130 and 150 V. Simultaneously, the snapback current is more than doubled compared to the base station technology, shown in **Fig. 6**. High voltage power devices have been measured for VSWR 10:1 at the nominal supply voltage of 42-50 V, but can even withstand values up to 60-70 V, as is expected from **Fig. 7**. This ruggedness has been achieved by engineering of the drain extension, epi layer thickness, and shield construction. From the snapback current and voltage we calculate the maximum dissipated power before failure. This power is an indication for the quality of the ruggedness of a power device as is shown in **Fig. 8** for 42 V development devices. We have plotted the power at which a power device fails (applying a VSWR of 10:1 with a DVB-T signal) versus the power at which an on-wafer test device fails (pulsed current voltage sweep). We find a linear relation between the power and on-wafer test device, which indicates this on-wafer test is a good predictor for the ruggedness of a power device. For large powers there is a deviation from the linear trend. We speculate that this is due to thermal aspects and circuitry matching.

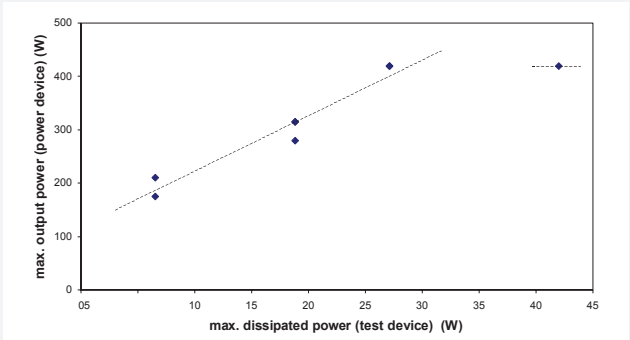

Figure 8: Correlation between the peak power at which a power device fails (VSWR of 10:1, 8k DVB-T, 9.5dB PAR) and the power dissipated at snapback of a corresponding test device.

V. RUGGEDNESS SAFE OPERATION AREA

In the application not only a drain voltage is applied but also a gate voltage. If the applied gate voltage is above the threshold voltage, current will flow in the transistor and in the base. This base current in combination with a high drain voltage will more easily trigger the parasitic bipolar transistor. We have measured the failures of devices for a wide range of current-voltage settings to construct a parasitic bipolar safe operation area (PB-SOA). The constructed PB-SOA curve is shown in **Fig. 9.**

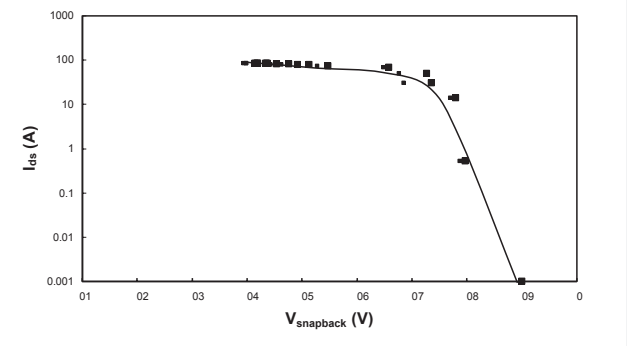

Figure 9: Constructed Safe Operation Area of the parasitic bipolar transistor as derived from on-wafer pulsed I-V measurements for Ampleon base station RF LDMOS

This PB-SOA curve resembles the theoretical safe operation area curve (**Fig. 10**), as is known for e.g. CMOS devices. We have added a few I-V characteristics and the class AB load line.

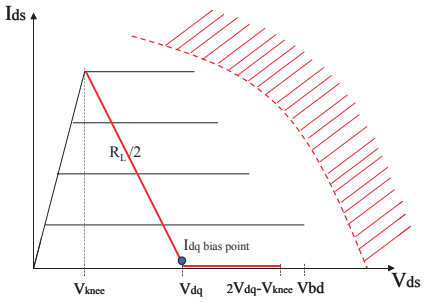

Figure 10: Schematic picture of the Safe Operation Area

The load line approached the edge of the SOA at its two extremes: at high drain current and at high drain voltage. For high current we have thermally induced triggering of the bipolar while at high drain voltage we have electrically induced triggering. By engineering the snap back characteristic we optimize our LDMOS devices to prevent the occurrence of the electrically induced triggering, since this mechanism is the most frequent cause for ruggedness failures as determined from the occurrence of a random damage pattern. Also the thermal behavior of LDMOS is part of the continuous improvement.

VI. RUGGEDNESS IN APPLICATIONS

After the on-wafer pulsed current voltage ruggedness measurements, several ruggedness tests are performed in the application circuitry, the most common one being a measurement of the VSWR. In data sheets typically a VSWR of 10:1 is specified under nominal power conditions. A wider bandwidth operation is required for more complex signals like W-CDMA. This puts heavier constraints to the broadband decoupling of circuits. The LDMOS device has to withstand signal deformations due to a non-ideal decoupling.

To test the wideband ruggedness a Video Band Width (VBW) measurement is performed. In a VBW test a signal with 2 tones in compression is applied, with a tone spacing of Δf. The tone spacing is increased until the device fails. Such a VBW test is shown in Table I for the base station LDMOS technology with a Δf of 80 MHz. This is a typical bandwidth for multi-slots W-CDMA amplifiers. Usually the LDMOS is operated at 32 V, but we see that the devices pass up to 35V supply voltage with this 80 MHz tone spacing.

P_{out} (dBm)	Vd		
	32 V	33 V	35 V
41.5	Pass	Pass	Pass
42.0	Pass	Pass	Pass
42.5	Pass	Pass	Pass
43.0	Pass	Pass	Pass

Extremely rugged devices are the high voltage technology families. These devices operate at 42-50 V at UHF or VHF frequencies, low frequencies where the most ruggedness demands exist. In **Fig. 11** the VSWR versus output power is plotted for drain supplies of 50 and 55 V. As predicted by the on-wafer tests (discussed in **Paragraph IV**), we see that the device can easily tolerate 55V drain voltage in combination with a VSWR of 20 and a power of 1.4 kW, values far above the nominal operation settings. These ruggedness tests are standard tests in the Ampleon reliability program and lead to state-of-the-art reliability performance.

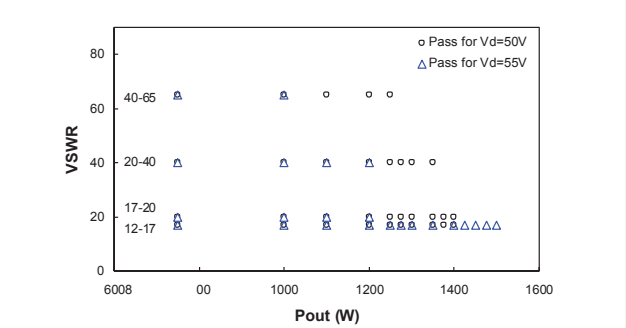

Figure 11: VSWR ruggedness measurement at various output power for a pulsed CW (with 20% duty cycle) signal at 225 MHz

VII. CONCLUSIONS

We have shown various ruggedness reliability tests for RF power transistors. Pulsed on-wafer snapback measurements during the development and VSWR and Video Bandwidth tests in the application circuitry are used to optimize the ruggedness of 28-42-50 V LDMOS technologies. Extremely rugged devices have been developed in combination with state-of-art RF performance.

ACKNOWLEDGEMENTS

The authors wish to acknowledge J. Gajadharsing, B. Merkus, H. Mollee, P. Hammes, T. Bakker, K. Vennema, J. Klappe, and M. Murphy for all discussions and support during the development.

REFERENCES

[1] F. van Rijs, S.J.C.H. Theeuwen, “Efficiency improvement of LDMOS transistors for base stations: towards the theoretical limit”, International Electron Devices Meeting, IEDM2006, pp. 205-208 (2006).

[2] S.J.C.H. Theeuwen, H. Mollee, “LDMOS Transistors in Power Microwave Applications”, December white paper at Micr. Journ. web (2008).

[3] S.J.C.H. Theeuwen, W.J.A.M. Sneijers, J.G.E. Klappe, J.A.M. de Boet, “High Voltage RF LDMOS Technology for Broadcast Applications”, Proceedings of the 3rd european Microwave Integrated Circuits Conference, EuMIC02-2, pp. 24-27 (2008).

www.ampleon.com

Date of release: March 2017
Document identifier: AMP PP 2017 0328
Printed in the Netherlands