CLP24H4S30P

RF power GaN-SiC HEMT

Rev. 1 — 23 July 2024

AMPLEON

Product data sheet

1. Product profile

1.1 General description

30 W GaN-SiC HEMT power transistor optimized with best Continuous Wave (CW) power and efficiency for applications in cooking, industrial, scientific and medical at frequencies from 2400 MHz to 2500 MHz.

The CLP24H4S30P is designed for driving high-power CW transistors and is assembled in a high performance DFN package.

Table 1. Application performance

Typical RF performance in a class-AB application circuit, unless otherwise specified.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(mA)	(V)	(W)	(dB)	(%)
CW	2400 to 2500	20	50	25	17	75

1.2 Features and benefits

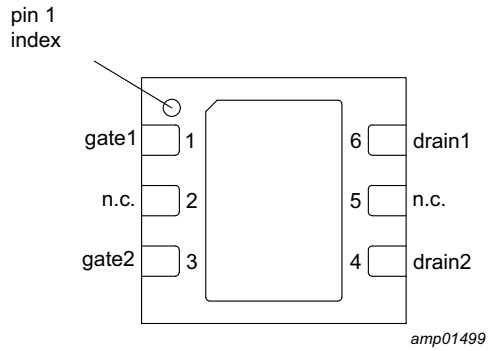
- High efficiency
- Ultra-small external matching circuit
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally input matched
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifier for CW applications in the 2400 MHz to 2500 MHz frequency range such as commercial and consumer cooking; industrial, scientific and medical applications

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
gate1	1	gate 1
n.c.	2	not connected
gate2	3	gate 2
drain2	4	drain 2
n.c.	5	not connected
drain1	6	drain 1

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
DFN-7x6.5-6-1	CLP24H4S30PZ	934960709515	TR7, 1000-fold, 16mm, Dry Pack	1000
DFN-7x6.5-6-1	CLP24H4S30PXY	934960709538	TR7, 100-fold, 16mm, Dry Pack	100

4. Limiting values

Table 4. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	operating	-	52	V
V_{DS}	drain-source voltage	V_{GS} = –8 V	-	150	V
$V_{GS(amp)}$	amplifier gate-source voltage		–15	+2	V
$I_{GF(amp)}$	amplifier forward gate current		-	3.2	mA
T_{stg}	storage temperature		–65	+150	°C
T_{ch}	active die channel temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(ch-top)(FEA)}$ [1]	thermal resistance from active die channel to top of package by Finite Element Analysis	P_{dis} = 8 W; T_{case} = 65 °C	6.12	K/W
$R_{th(ch-c)(FEA)}$ [1]	thermal resistance from active die channel to case by Finite Element Analysis	P_{dis} = 8 W; T_{case} = 65 °C	5.7	K/W

[1] The device is mounted on a PCB with copper filled vias underneath the grounding pad of the device, with the PCB mounted on a cooling surface. The ambient temperature is 25 °C.

[2] Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

6. Characteristics

Table 6. DC characteristics

Single section DC characteristics; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 3.2 mA	–3.5	–2.8	–2.2	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 64 mA	–3.05	–2.6	–2.05	V
$I_{D(leak)}$	drain leakage current	V_{GS} = –10 V; V_{DS} = 50 V	-	-	0.774	mA
I_{GSS}	gate leakage current	V_{GS} = –8 V; V_{DS} = 0 V	-	-	0.155	mA
I_{DSX}	drain cut-off current	V_{DS} = 20 V; V_{GS} = 2 V	-	2.68	-	A

Table 7. RF characteristics

Test signal: pulsed at f = 2450 MHz; RF performance at V_{DS} = 50 V; t_p = 50 μs; δ = 2 %; I_{Dq} = 5 mA; T_{amb} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 30 W	-	18.4	-	dB
RL_{in}	input return loss	P_L = 30 W	-	–8	-	dB
η_D	drain efficiency	P_L = 30 W	-	61	-	%

Table 8. Ruggedness performance

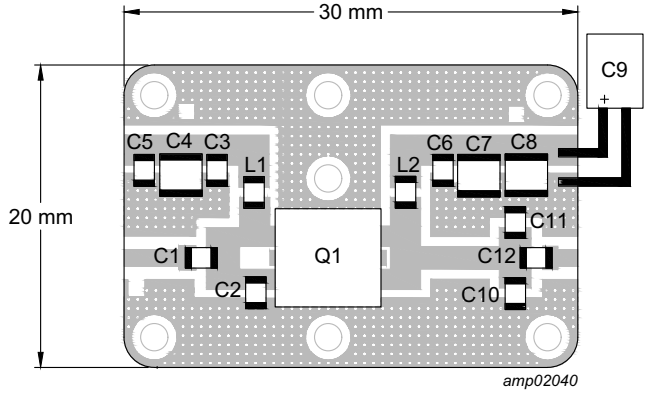
RF performance at T_{amb} = 25 °C; V_{GS} = −4 V; in a class-C demo.

Test signal	f (MHz)	P_L (W)	VSWR	V_{DS} (V)	Result
CW	2450	30	10 : 1 at all phase angles	70	no device degradation
pulsed CW [1]	2450	30	10 : 1 at all phase angles	70	no device degradation

[1] t_p = 100 µs; δ = 20 %.

7. Application information

7.1 Test circuit



Printed-Circuit Board (PCB): TC350; thickness = 0.508 mm with Type II vias. See Table 9 for a list of components.

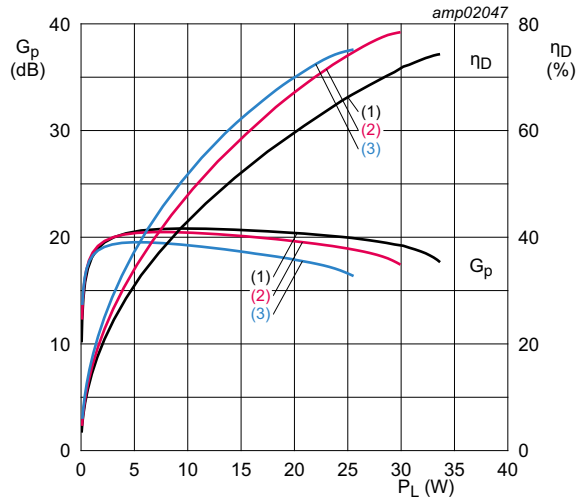
Fig 2. Component layout for test circuit

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C3, C6, C12	multilayer ceramic chip capacitor	100 pF	ATC600F101JW250XT
C4, C7	multilayer ceramic chip capacitor	1000 pF	ATC800B102KW50XT
C5, C8	multilayer ceramic chip capacitor	4.7 µF, 100 V	TDK: C2012X7R1H475K
C2	multilayer ceramic chip capacitor	1.2 pF	ATC600F1R2BW250XT
C10, C11	multilayer ceramic chip capacitor	1.4 pF	ATC600F1R4BW250XT
C9	electrolytic capacitor	1000 µF, 63 V	
L1	inductor	12 nH	Coilcraft: 0805HP-12NXGRC
L2	inductor	6.8 nH	Coilcraft: 0805HP-6N8XGRC
Q1	GaN transistor		CLP24H4S30P

7.2 Graphical data



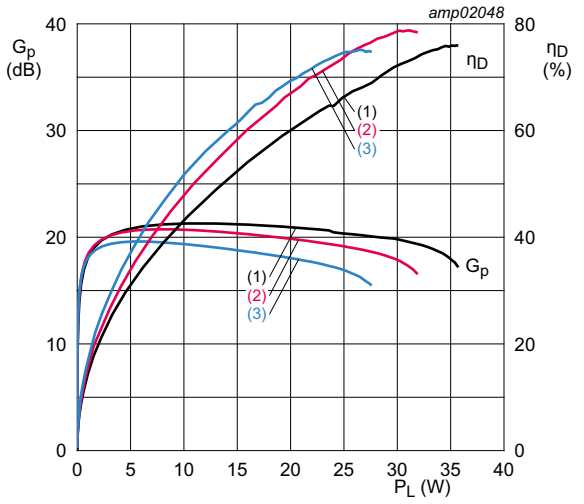
Test signal: CW; V_{DS} = 50 V; I_{Dq} = 1 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



Test signal: CW pulsed; V_{DS} = 50 V; I_{Dq} = 1 mA; t_p = 100 µs; δ = 10 %.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values

7.3 Impedance information

Table 10. Typical impedance

Simulated Z_S and Z_L matching circuit Impedances.

f	Z_S [1]	Z_L [1]	$Z_{L(2H)}$ [1]
(MHz)	(Ω)	(Ω)	(Ω)
2400	18.99 – 31.23j	11.92 + 34.05j	2.46 – 87.88j
2450	18.06 – 30.33j	11.90 + 36.92j	2.16 – 79.62j
2500	17.19 – 29.44j	11.92 + 39.93j	2.46 – 72.61j

[1] Z_S, Z_L and $Z_{L(2H)}$ defined in Figure 5.

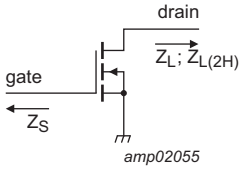


Fig 5. Definition of transistor impedance

8. Package outline

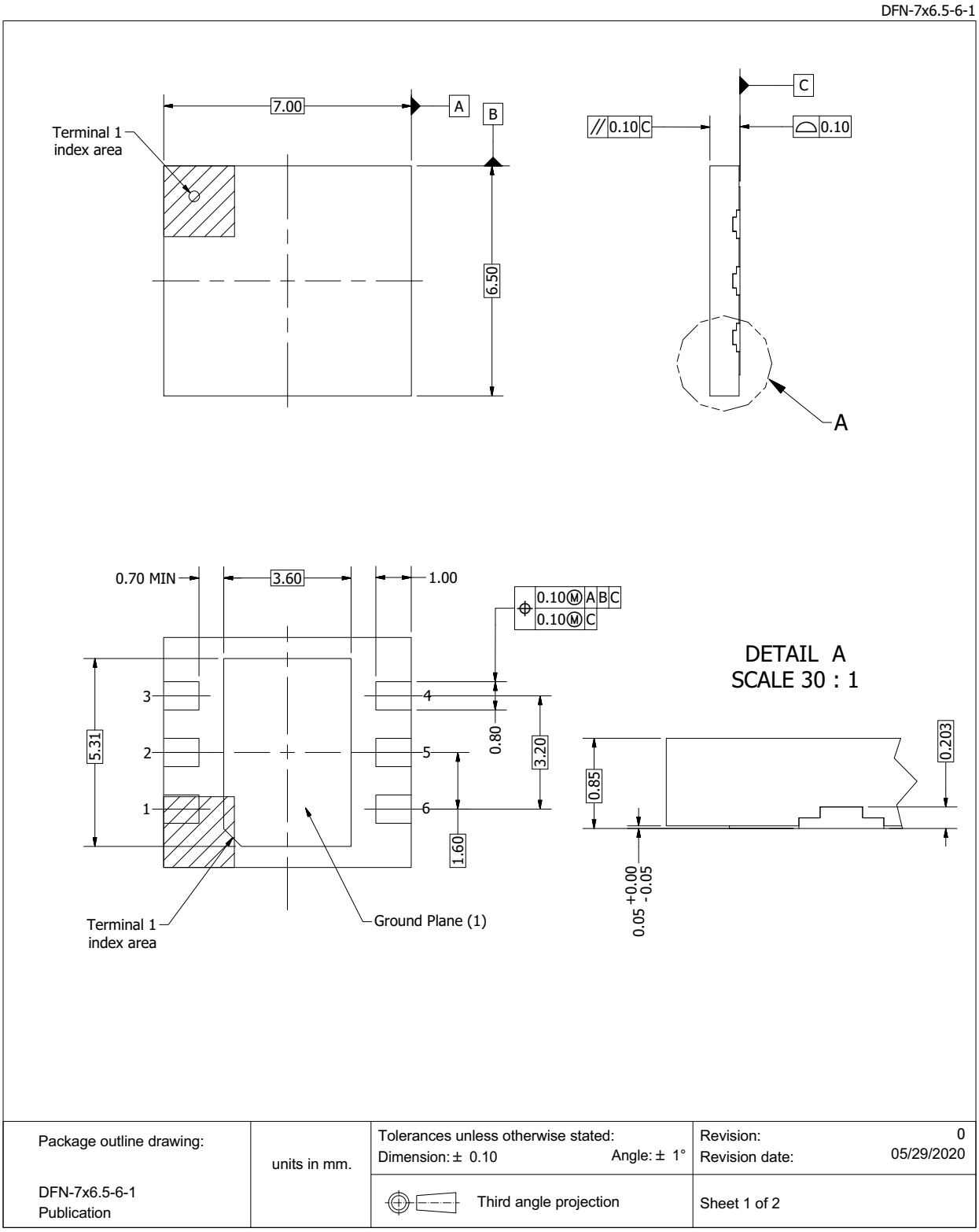


Fig 6. Package outline DFN-7x6.5-6-1 (sheet 1 of 2)

DFN-7x6.5-6-1

Drawing Notes	
Items	Description
(1)	Terminals (bottom View) and ground-plane (bottom View) are plated with matte Sn.
(2)	Plastic or metal protrusions of 0.075 mm max. per side are not included.

Package outline drawing: DFN-7x6.5-6-1 Publication	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.10 Angle: ± 1° Third angle projection	Revision: 0 Revision date: 05/29/2020 Sheet 2 of 2

Fig 7. Package outline DFN-7x6.5-6-1 (sheet 2 of 2)

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1A

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SiC	Silicon Carbide
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CLP24H4S30P v.1	20240723	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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