CLF3H0060-30; CLF3H0060S-30

Broadband RF power GaN HEMT

AMPLEON

Rev. 1 — 20 December 2021 **Product data sheet**

1. Product profile

1.1 General description

The CLF3H0060-30 and CLF3H0060S-30 are 30 W general purpose, unmatched broadband GaN-SiC HEMT transistors that are usable in the frequency range from DC to 6.0 GHz. The device utilizes a thermally enhanced package which supports both CW and pulsed applications.

Table 1. Typical performance

RF performance at T_{case} = 25 °C; V_{DS} = 50 V; I_{Dq} = 60 mA; in a class-AB broadband demo.

Test signal	f	P_L	G_p	η_D
	(MHz)	(W)	(dB)	(%)
CW [1]	960	30	20.18	60.61
	1050	30	20.33	60.34
	1150	30	20.51	62.17
	1250	30	20.46	66.10
	1350	30	19.97	66.40
	1400	30	19.32	65.10
pulsed CW [1][2]	960	30	20.24	61.62
	1050	30	20.40	61.58
	1150	30	20.56	62.87
	1250	30	20.57	67.10
	1350	30	20.10	67.80
	1400	30	19.44	66.48

[1] Measured on a 960 MHz to 1400 MHz broadband circuit.

[2] t_p = 100 μs; δ = 10 %.

Table 2. Typical performance

RF performance at T_{case} = 25 °C; V_{DS} = 50 V; I_{Dq} = 100 mA; in a class-AB broadband demo.

Test signal	f	P_L	G_p	η_D
	(MHz)	(W)	(dB)	(%)
CW [1]	500	30	15.52	62.67
	700	30	15.37	53.75
	1000	30	15.17	49.14
	1400	30	14.87	47.38
	2000	30	15.20	47.86
	2500	30	15.36	47.37

[1] Measured on a 500 MHz to 2500 MHz broadband circuit.

Table 3. Typical performance

RF performance at T_{case} = 25 °C; V_{DS} = 50 V; I_{Dq} = 60 mA; in a class-AB broadband demo.

Test signal	f	P_L	VSWR	Test voltage	Result
	(MHz)	(W)		(V)	
CW [1]	1300	30	15 : 1 at all phase angles	50	no device degradation
pulsed CW [2][3]	2500	30	15 : 1 at all phase angles	50	no device degradation

[1] Measured on a 1300 MHz narrowband circuit.

[2] Measured on a 2500 MHz narrowband circuit.

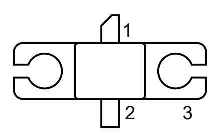
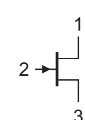
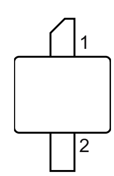
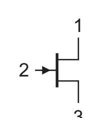
[3] t_p = 100 μs; δ = 10 %.

1.2 Features and benefits

- 30 W general purpose broadband RF power GaN HEMT
- High efficiency
- Low thermal resistance
- Excellent ruggedness
- Designed for broadband operation in the frequency range from DC to 6.0 GHz
- For RoHS compliance see the product details on the Ampleon website
- Large signal models in ADS and MWO are available on the Ampleon website

2. Pinning information

Table 4. Pinning

Pin	Description		Simplified outline	Graphic symbol
CLF3H0060-30 (SOT1227A)				
1	drain			 amp01464
2	gate			
3	source	[1]		
CLF3H0060S-30 (SOT1227B)				
1	drain			 amp01464
2	gate			
3	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 5. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1227A	CLF3H0060-30U	9349 603 36112	Tray; 20-fold; non-dry pack	20
SOT1227B	CLF3H0060S-30U	9349 603 37112	Tray; 20-fold; non-dry pack	20

4. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	150	V
V_{GS}	gate-source voltage		–8	+2	V
I_{GF}	forward gate current	external R_G= 5 Ω	-	11	mA
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(s-c)(IR)}$ [1]	thermal resistance from active die surface to case by Infrared measurement	T_{case} = 85 °C; V_{DS} = 50 V; I_{Dq} = 70 mA; P_{dis} = 24 W	3.2	K/W
$R_{th(ch-c)(FEA)}$ [2]	thermal resistance from active die channel to case by Finite Element Analysis	T_{case} = 85 °C; V_{DS} = 50 V; I_{Dq} = 70 mA; P_{dis} = 24 W	5.6	K/W

[1] Infrared (IR) thermal values are for reference only and cannot be used to determine performance or reliability.

[2] Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

6. Characteristics

Table 8. DC characteristics

T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = –8 V; I_D = 5 mA	150	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 6 V; I_D = 50 mA	-	–2.9	-	V
I_{DSX}	drain cut-off current	V_{GS} = 2 V; V_{DS} = 6 V	-	3.9	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 6 V	-	-	43.75	nA
g_{fs}	forward transconductance	V_{GS} = 0 V; V_{DS} = 6 V	-	1.22	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = 0 V; V_{DS} = 100 mV	-	75	-	mΩ

Table 9. AC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = −8 V; V_{DS} = 50 V; f = 1 MHz [1]	-	6.06	-	pF
C_{oss}	output capacitance	V_{GS} = −8 V; V_{DS} = 50 V; f = 1 MHz [1]	-	3.17	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = −8 V; V_{DS} = 50 V; f = 1 MHz [1]	-	0.26	-	pF

[1] Include package.

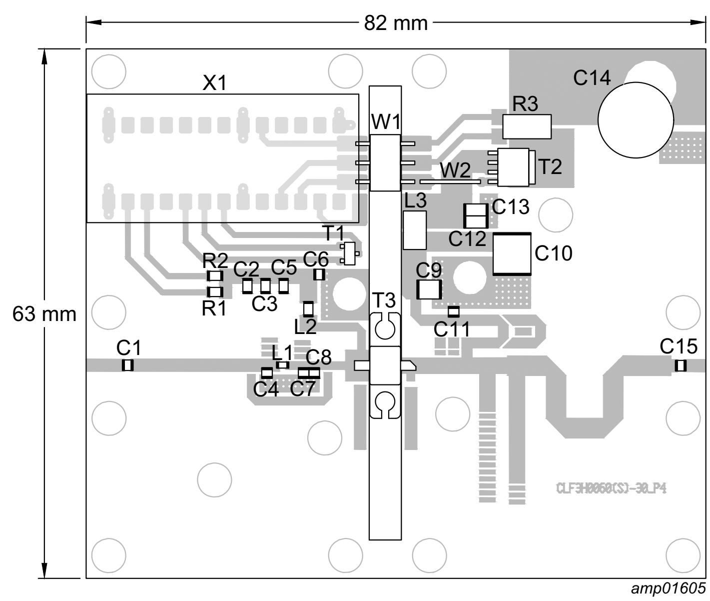
Table 10. RF characteristics

Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; V_{DS} = 50 V; I_{Dq} = 70 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production circuit measured at 2500 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 30 W	15.5	17	-	dB
RL_{in}	input return loss	P_L = 30 W	-	−15	-	dB
η_D	drain efficiency	P_L = 30 W	57	61.5	-	%

7. Application information

7.1 Demo circuit information (f = 960 MHz to 1400 MHz)



Printed-Circuit Board (PCB): Rogers RO4350; thickness = 0.762 mm.

See Table 11 for list of components.

Fig 1. Component layout for broadband demo circuit f = 960 MHz to 1400 MHz

Table 11. List of components

For test circuit see Figure 1.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	82 pF	ATC 100A
C2	multilayer ceramic chip capacitor	100 nF	B37941X5104K062
C3	multilayer ceramic chip capacitor	10 pF	GRM21BR72E103KW03L
C4	multilayer ceramic chip capacitor	2.7 pF	ATC 100A
C5	multilayer ceramic chip capacitor	1 nF	GRM21AR72E102KW01D
C6	multilayer ceramic chip capacitor	82 pF	ATC 100A
C7	multilayer ceramic chip capacitor	3.9 pF	ATC 100A
C8	multilayer ceramic chip capacitor	3.6 pF	ATC 100A
C9	multilayer ceramic chip capacitor	4.7 μF	CGA6M3X7S2A475M200AE
C10	multilayer ceramic chip capacitor	4.7 μF	GRM55ER72A475KA01L
C11	multilayer ceramic chip capacitor	11 pF	ATC 100A
C12	multilayer ceramic chip capacitor	10 nF	VJ1206Y103KXCT
C13	multilayer ceramic chip capacitor	1 μF	GRM31CR72A105KA01L
C14	electrolytic capacitor	220 μF, 63 V	EEUFR1J221LB
L1	surface mount inductor	3.3 nH	B82496C3339A
L2	surface mount inductor	100 nH	MLZ2012DR10DT
L3	ferrite bead	47 Ω at 100 MHz	2743019447
R1	SMD resistor	10 kΩ	0805
R2	SMD resistor	4.7 Ω	0805
R3	current sense resistor	10 mΩ	FC4L64R010FER
W1	connector		
W2	PTFE wire		
T1	PNP general purpose transistor		BC857A
T2	N-channel MOSFET		PSMN8R2-80YS
T3	DUT		CLF3H0060(S)-30
X1	GaN bias module		Ampleon

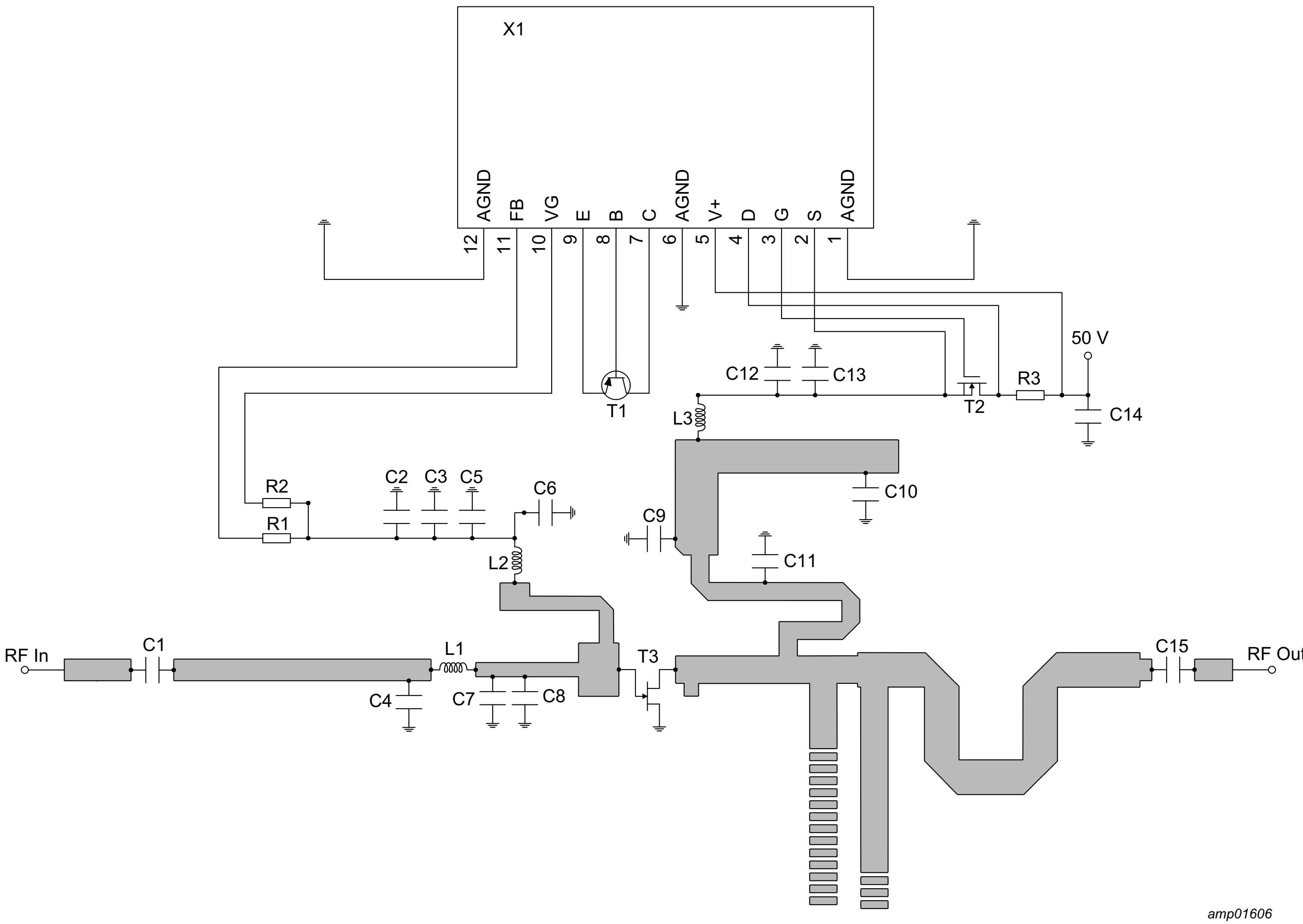
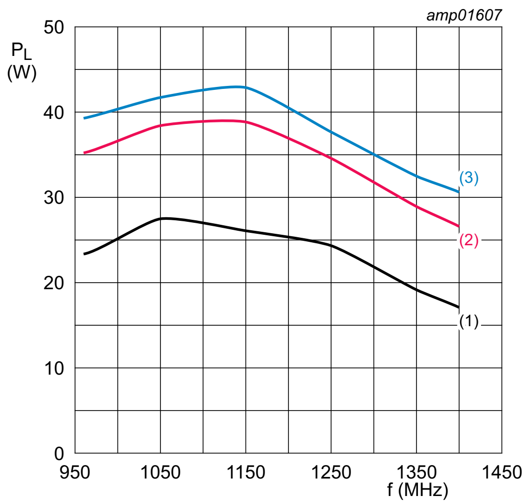


Fig 2. Schematic for broadband demo circuit f = 960 MHz to 1400 MHz

7.2 Graphical data (f = 960 MHz to 1400 MHz)

7.2.1 CW performance



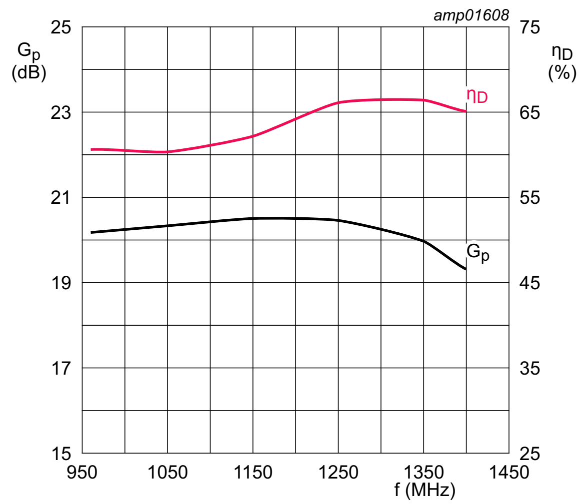
V_{DS} = 50 V; I_{Dq} = 60 mA.

(1) $P_{L(1dB)}$

(2) $P_{L(2dB)}$

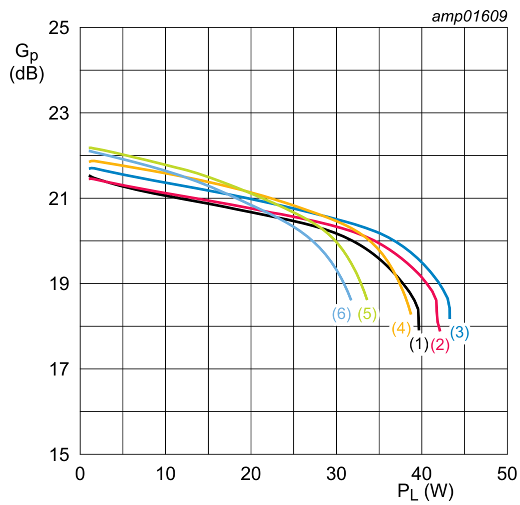
(3) $P_{L(3dB)}$

Fig 3. Output power at gain compression as a function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA; P_L = 30 W.

Fig 4. Power gain and drain efficiency as function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA.

(1) f = 960 MHz

(2) f = 1050 MHz

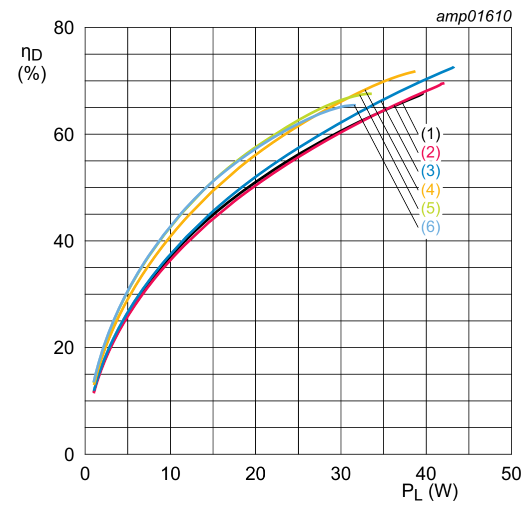
(3) f = 1150 MHz

(4) f = 1250 MHz

(5) f = 1350 MHz

(6) f = 1400 MHz

Fig 5. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA.

(1) f = 960 MHz

(2) f = 1050 MHz

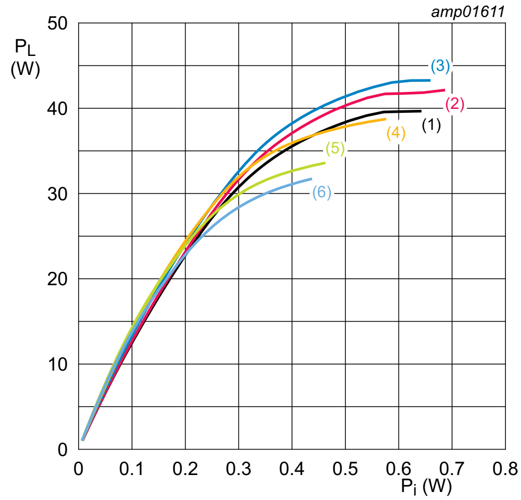
(3) f = 1150 MHz

(4) f = 1250 MHz

(5) f = 1350 MHz

(6) f = 1400 MHz

Fig 6. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA.

(1) f = 960 MHz

(2) f = 1050 MHz

(3) f = 1150 MHz

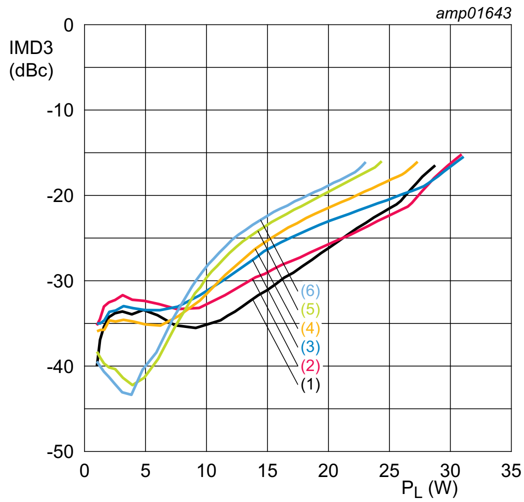
(4) f = 1250 MHz

(5) f = 1350 MHz

(6) f = 1400 MHz

Fig 7. Output power as a function of input power; typical values

7.2.2 2-Tone CW performance



V_{DS} = 50 V; I_{Dq} = 60 mA; 10 kHz spacing.

(1) f = 960 MHz

(2) f = 1050 MHz

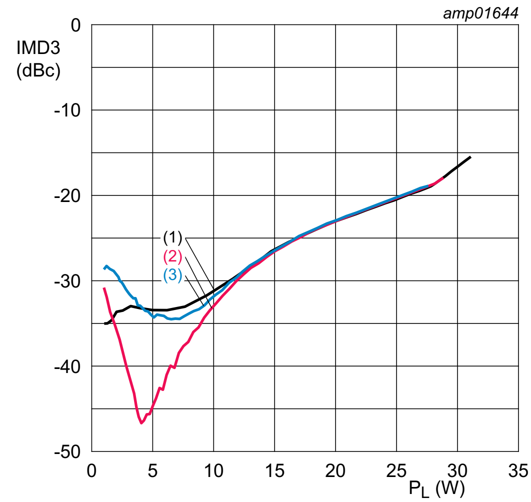
(3) f = 1150 MHz

(4) f = 1250 MHz

(5) f = 1350 MHz

(6) f = 1400 MHz

Fig 8. Third-order intermodulation distortion as a function of output power; typical values



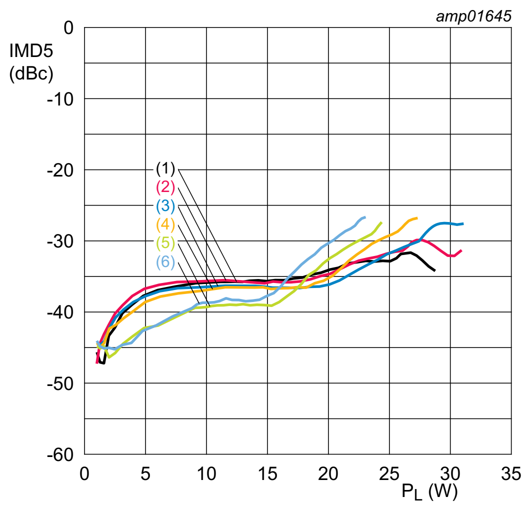
V_{DS} = 50 V; f = 1150 MHz; 10 kHz spacing.

(1) I_{Dq} = 60 mA

(2) I_{Dq} = 120 mA

(3) I_{Dq} = 180 mA

Fig 9. Third-order intermodulation distortion as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA; 10 kHz spacing.

(1) f = 960 MHz

(2) f = 1050 MHz

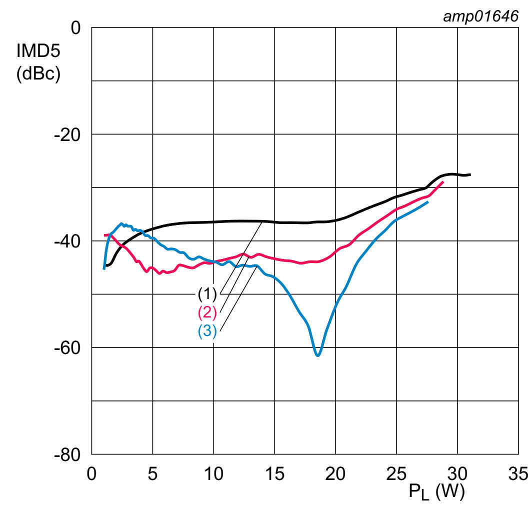
(3) f = 1150 MHz

(4) f = 1250 MHz

(5) f = 1350 MHz

(6) f = 1400 MHz

Fig 10. Fifth-order intermodulation distortion as a function of output power; typical values



V_{DS} = 50 V; f = 1150 MHz; 10 kHz spacing.

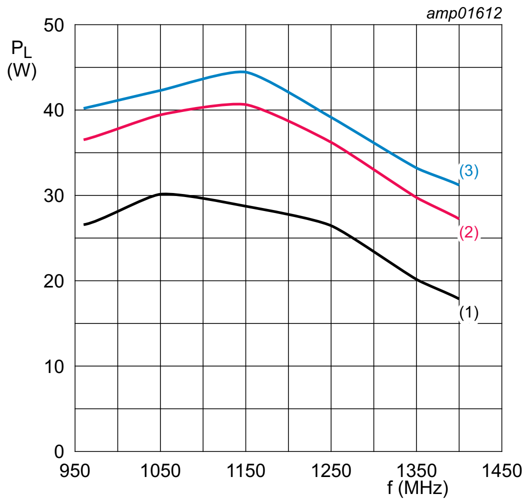
(1) I_{Dq} = 60 mA

(2) I_{Dq} = 120 mA

(3) I_{Dq} = 180 mA

Fig 11. Fifth-order intermodulation distortion as a function of output power; typical values

7.2.3 Pulsed CW performance



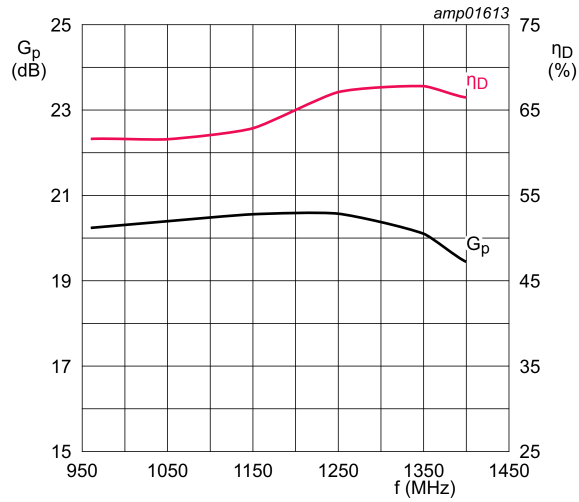
V_{DS} = 50 V; I_{Dq} = 60 mA; t_p = 100 µs; δ = 10 %.

(1) $P_{L(1dB)}$

(2) $P_{L(2dB)}$

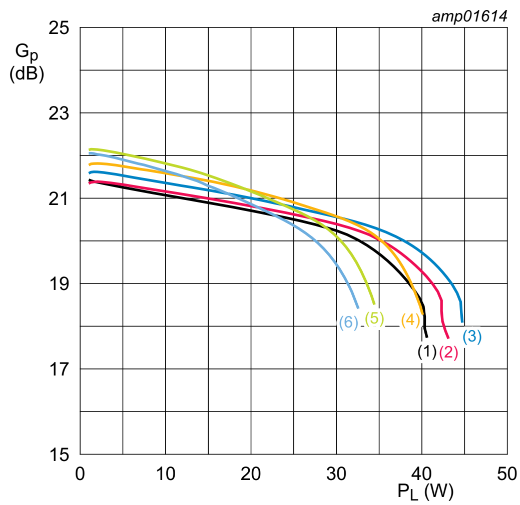
(3) $P_{L(3dB)}$

Fig 12. Output power at gain compression as a function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA; P_L = 30 W; t_p = 100 µs; δ = 10 %.

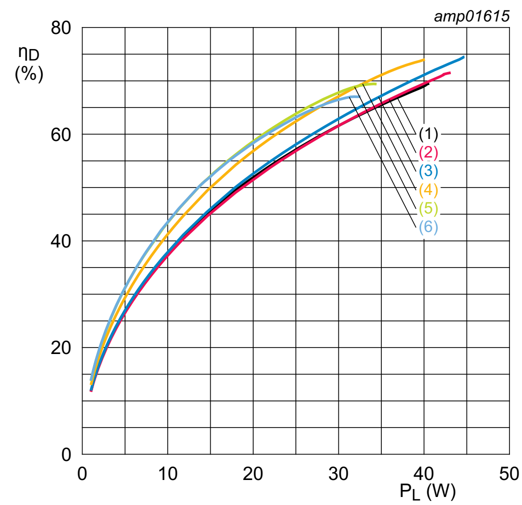
Fig 13. Power gain and drain efficiency as function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA; t_p = 100 μs; δ = 10 %.

(1) f = 960 MHz
(2) f = 1050 MHz
(3) f = 1150 MHz
(4) f = 1250 MHz
(5) f = 1350 MHz
(6) f = 1400 MHz

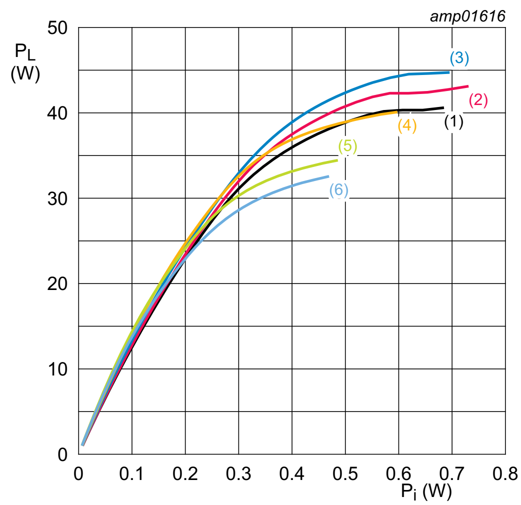
Fig 14. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA; t_p = 100 μs; δ = 10 %.

(1) f = 960 MHz
(2) f = 1050 MHz
(3) f = 1150 MHz
(4) f = 1250 MHz
(5) f = 1350 MHz
(6) f = 1400 MHz

Fig 15. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 60 mA; t_p = 100 μs; δ = 10 %.

(1) f = 960 MHz

(2) f = 1050 MHz

(3) f = 1150 MHz

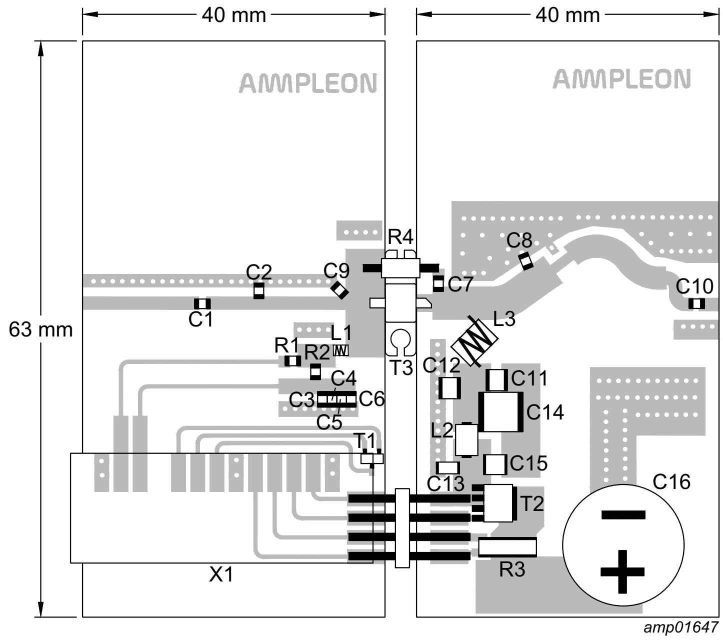
(4) f = 1250 MHz

(5) f = 1350 MHz

(6) f = 1400 MHz

Fig 16. Output power as a function of input power; typical values

7.3 Demo circuit information (f = 500 MHz to 2500 MHz)



Printed-Circuit Board (PCB): Taconic RF-35; thickness = 0.762 mm.

See Table 12 for list of components.

Fig 17. Component layout for broadband demo circuit f = 500 MHz to 2500 MHz

Table 12. List of components

For test circuit see Figure 17.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	8.2 pF	ATC 600F
C2	multilayer ceramic chip capacitor	0.8 pF	ATC 600F
C3	multilayer ceramic chip capacitor	100 nF, 50 V	0805 generic
C4	multilayer ceramic chip capacitor	10 nF, 50 V	0805 generic
C5	multilayer ceramic chip capacitor	22 pF, 100 V	0805 generic
C6	multilayer ceramic chip capacitor	1 nF, 100 V	0805 generic
C7	multilayer ceramic chip capacitor	10 pF	ATC 600F
C8	multilayer ceramic chip capacitor	1.1 pF	ATC 600F
C9	multilayer ceramic chip capacitor	0.5 pF	ATC 600F
C10	multilayer ceramic chip capacitor	22 pF	ATC 600F
C11	multilayer ceramic chip capacitor	100 pF	ATC 100B
C12	multilayer ceramic chip capacitor	1000 pF	ATC 100B
C13	multilayer ceramic chip capacitor	1 μF, 100 V	1206 generic
C14	multilayer ceramic chip capacitor	10 μF, 100 V	TDK C550X7S2A106M
C15	multilayer ceramic chip capacitor	1 nF, 200 V	1210 generic
C16	electrolytic capacitor	470 μF, 63 V	PCE3667CT-ND
L1	ceramic chip inductor	10 nH	Coilcraft: 1008CS-100X
L2	ferrite bead	47 Ω at 100 MHz	2743019447

Table 12. List of components *...continued*
For test circuit see Figure 17.

Component	Description	Value	Remarks
L3	air core inductor	12 nH	Coilcraft: GA3094
R1	SMD resistor	10 kΩ	0805
R2	SMD resistor	10 Ω	0805
R3	current sense resistor	5 mΩ	RL7520WT-R005-F
R4	resistor	200 Ω	LR12010T0200J
T1	PNP general purpose transistor		BC857A
T2	N-channel MOSFET		PSMN8R2-80YS
T3	DUT		CLF3H0060(S)-30
X1	GaN bias module		Ampleon

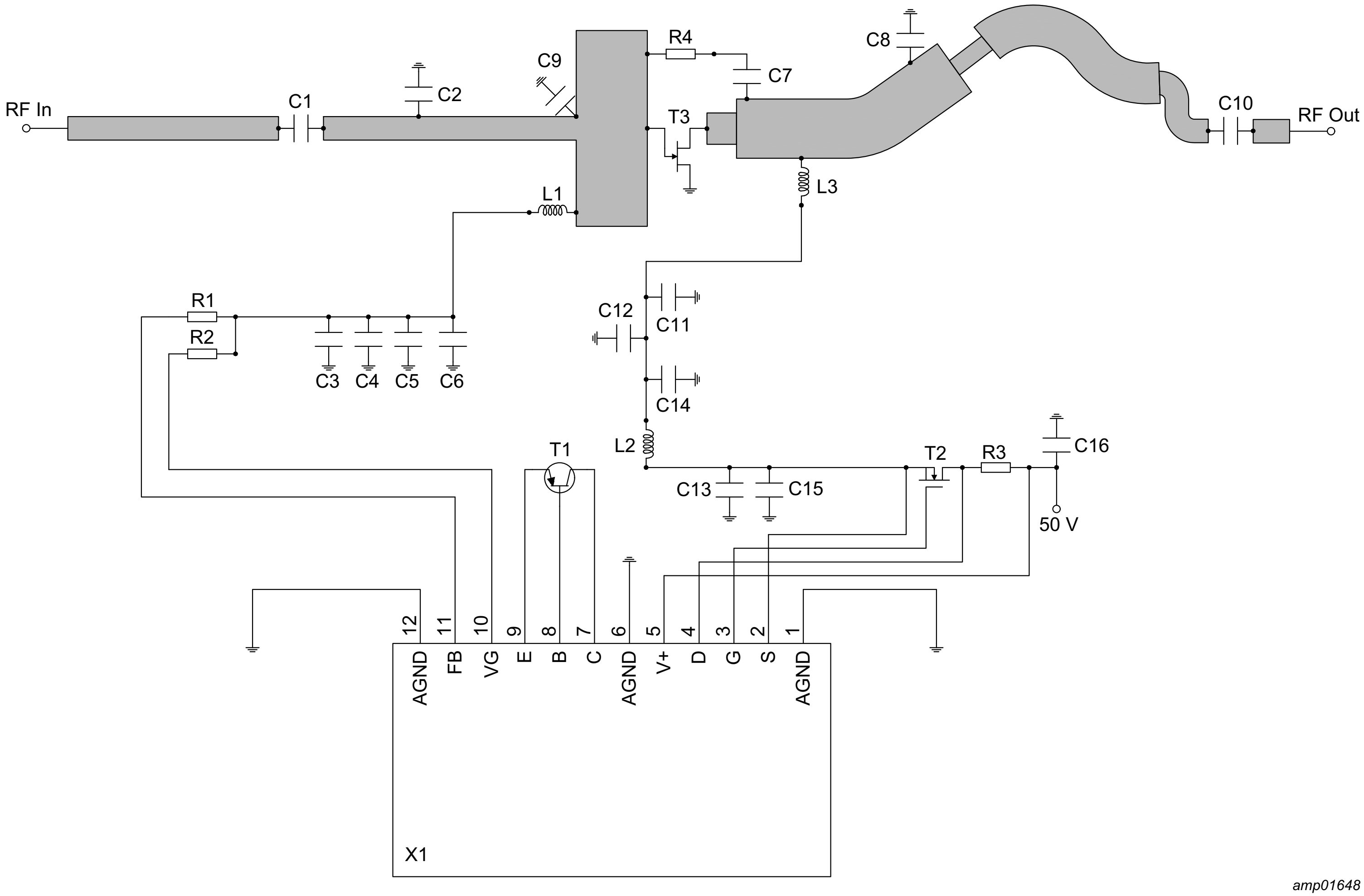
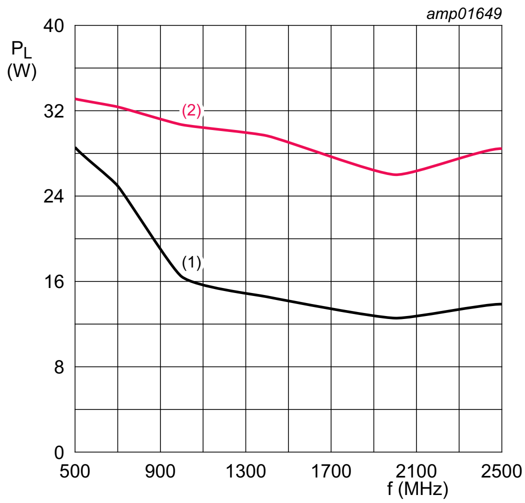


Fig 18. Schematic for broadband demo circuit f = 500 MHz to 2500 MHz

7.4 Graphical data (f = 500 MHz to 2500 MHz)

7.4.1 CW performance

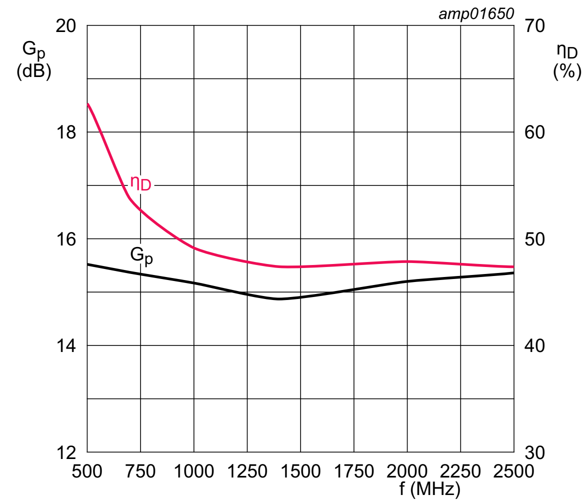


V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) $P_{L(1dB)}$

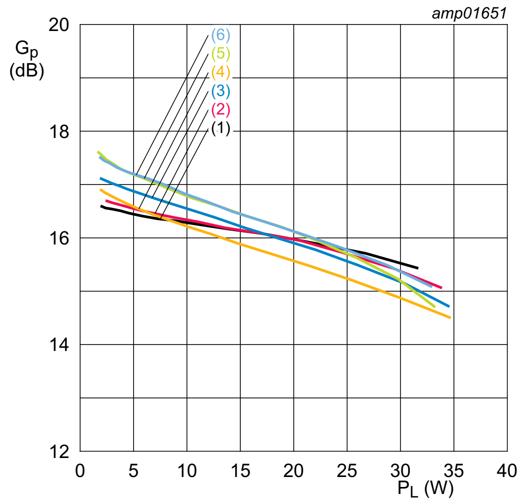
(2) $P_{L(2dB)}$

Fig 19. Output power at gain compression as a function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA.

Fig 20. Power gain and drain efficiency as function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) f = 500 MHz

(2) f = 700 MHz

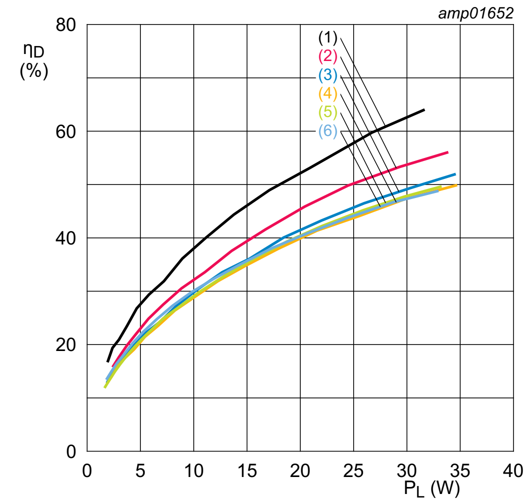
(3) f = 1000 MHz

(4) f = 1400 MHz

(5) f = 2000 MHz

(6) f = 2500 MHz

Fig 21. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) f = 500 MHz

(2) f = 700 MHz

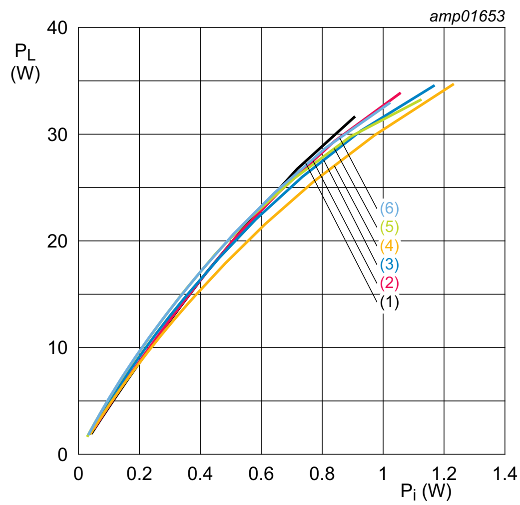
(3) f = 1000 MHz

(4) f = 1400 MHz

(5) f = 2000 MHz

(6) f = 2500 MHz

Fig 22. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA.

(1) f = 500 MHz

(2) f = 700 MHz

(3) f = 1000 MHz

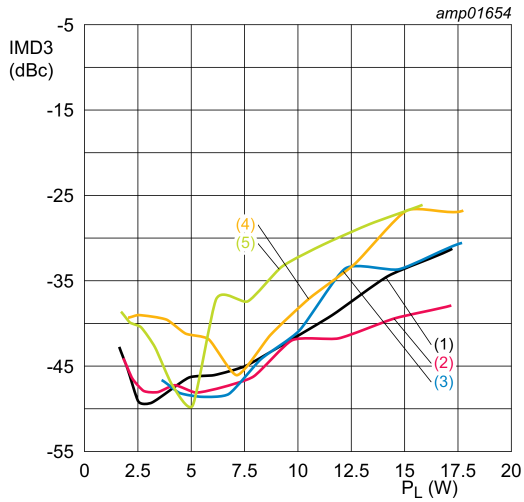
(4) f = 1400 MHz

(5) f = 2000 MHz

(6) f = 2500 MHz

Fig 23. Output power as a function of input power; typical values

7.4.2 2-Tone CW performance



V_{DS} = 50 V; I_{Dq} = 100 mA; 10 kHz spacing.

(1) f = 500 MHz

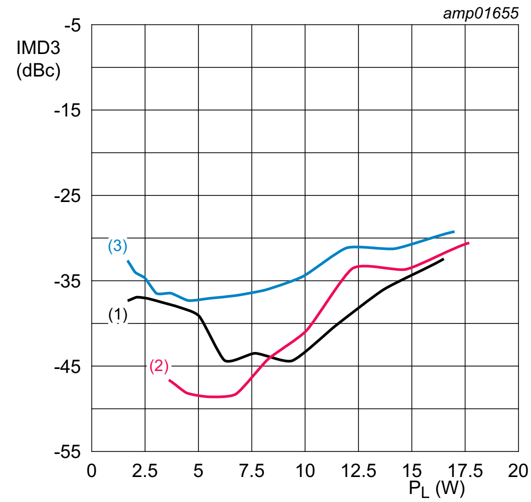
(2) f = 1000 MHz

(3) f = 1500 MHz

(4) f = 2000 MHz

(5) f = 2500 MHz

Fig 24. Third-order intermodulation distortion as a function of output power; typical values



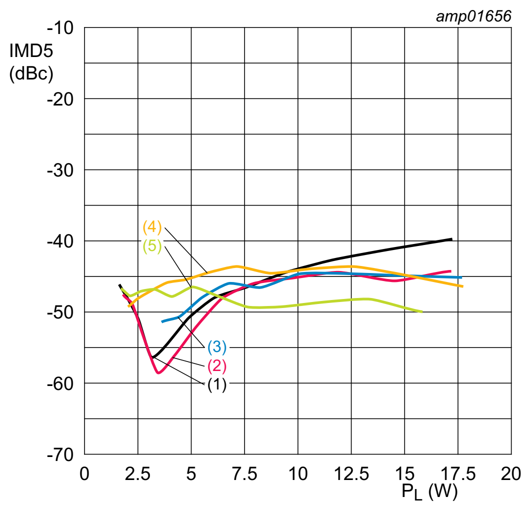
V_{DS} = 50 V; f = 1500 MHz; 10 kHz spacing.

(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

(3) I_{Dq} = 150 mA

Fig 25. Third-order intermodulation distortion as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA; 10 kHz spacing.

(1) f = 500 MHz

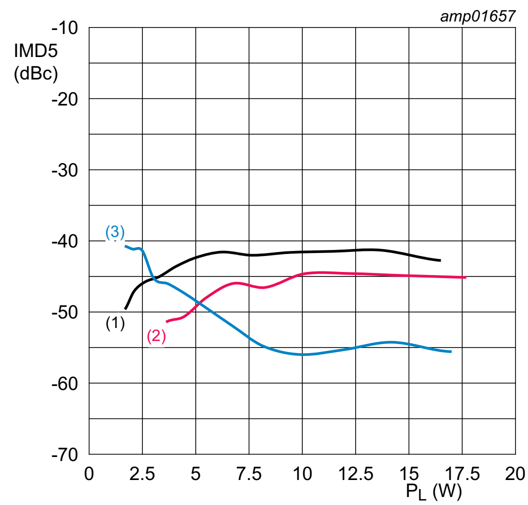
(2) f = 1000 MHz

(3) f = 1500 MHz

(4) f = 2000 MHz

(5) f = 2500 MHz

Fig 26. Fifth-order intermodulation distortion as a function of output power; typical values



V_{DS} = 50 V; f = 1500 MHz; 10 kHz spacing.

(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

(3) I_{Dq} = 150 mA

Fig 27. Fifth-order intermodulation distortion as a function of output power; typical values

8. Test information

8.1 Load-pull impedance information

The measured load-pull impedances are shown below. Impedance reference plane defined at device leads. Measurements performed with Ampleon test fixtures. Test temperature set at 25 °C with a pulsed CW signal; t_p = 100 μs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA.

Table 13. Typical impedance

Typical values unless otherwise specified.

f	Z_S	Z_L (maximum $P_{L(M)}$)	Z_L (maximum η_D)
(MHz)	(Ω)	(Ω)	(Ω)
1000	2.1 + j9.3	24.0 + j9.0	35.0 + j38.0
1400	2.0 + j4.7	21.0 + j10.0	20.0 + j22.0
1700	1.8 + j1.5	19.0 + j8.3	16.0 + j15.0
2000	2.0 – j1.2	16.0 + j6.2	16.0 + j12.0
2500	2.5 – j5.0	14.0 + j1.7	7.6 + j7.8
2700	2.3 – j6.4	12.0 + j1.3	5.1 + j6.7
3000	3.6 – j7.7	13.0 – j1.2	7.2 + j4.1
3500	4.7 – j12.6	11.8 – j3.7	8.0 + j0.9
4000	6.0 – j15.7	10.9 – j5.9	7.5 – j3.5
4500	6.8 – j17.0	9.7 – j9.5	6.1 – j6.6
5000	6.8 – j19.1	8.9 – j12.0	5.9 – j9.8

[1] Z_S and Z_L defined in Figure 28.

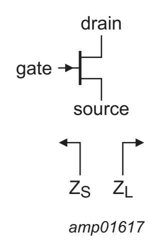
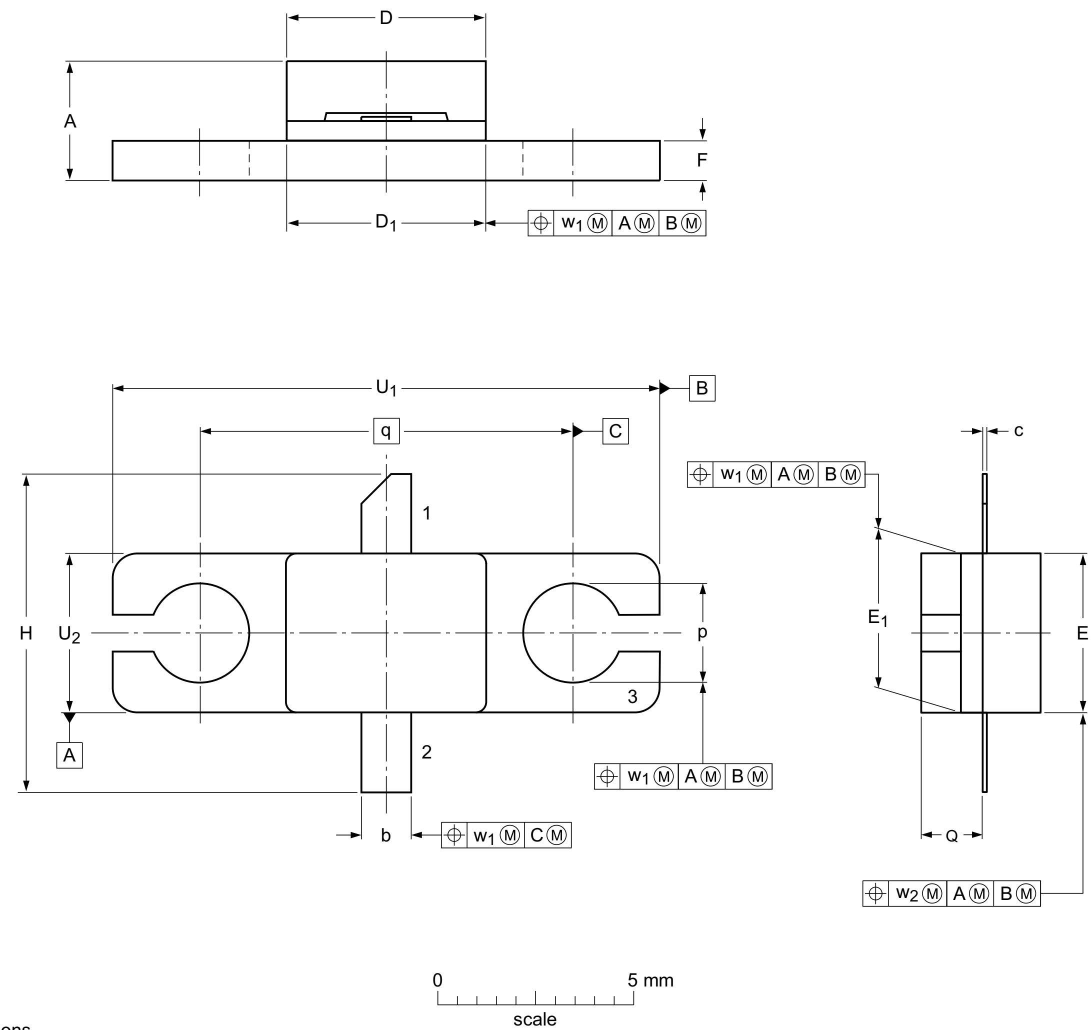


Fig 28. Definition of transistor impedance

Z_S is the measured source pull impedance presented to the device. Z_L is the measured load pull impedance presented to the device.

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT1227A**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	max	3.68	1.40	0.15	5.18	5.21	4.17	4.19	1.14	8.64	2.67	1.70		14.10	4.19		
	nom												9.53			0.25	0.380
	min	2.84	1.14	0.08	4.98	4.95	3.96	3.94	0.89	7.62	2.41	1.45		13.84	3.94		
inches	max	0.145	0.055	0.006	0.204	0.205	0.164	0.165	0.045	0.340	0.105	0.067		0.555	0.165		
	nom												0.375			0.01	0.015
	min	0.112	0.045	0.003	0.196	0.195	0.156	0.155	0.035	0.300	0.095	0.057		0.545	0.155		

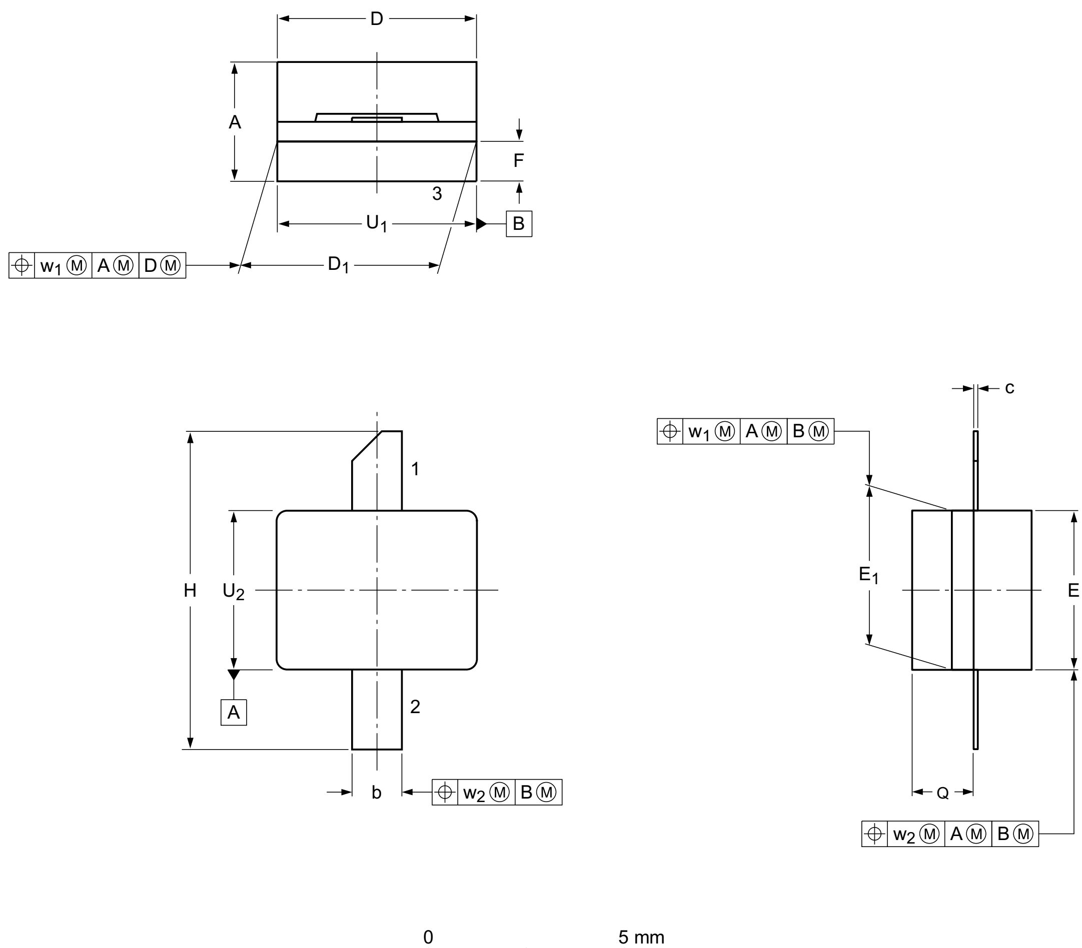
Note
1. Millimeter dimensions are derived from the original inch dimensions.

sot1227a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1227A						~~12-06-08~~ 13-10-14

Fig 29. Package outline SOT1227A

Earless Flanged ceramic package; 2 leads **SOT1227B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	F	H	Q	U_1	U_2	w_1	w_2
mm	max	3.68	1.40	0.15	5.18	5.21	4.17	4.19	1.07	8.64	1.70	5.21	4.19		
	nom													0.25	0.380
	min	2.84	1.14	0.08	4.98	4.95	3.96	3.94	0.97	7.62	1.45	4.95	3.94		
inches	max	0.145	0.055	0.006	0.204	0.205	0.164	0.165	0.042	0.340	0.067	0.205	0.165		
	nom													0.01	0.015
	min	0.112	0.045	0.003	0.196	0.195	0.156	0.155	0.038	0.300	0.057	0.195	0.155		

Note
1. Millimeter dimensions are derived from the original inch dimensions.

sot1227b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1227B						~~12-06-08~~ 13-10-15

Fig 30. Package outline SOT1227B

10. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 14. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1A [2]

[1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V.

[2] HBM classification 1A is granted to any part that passes after exposure to an ESD pulse of 250 V.

11. Abbreviations

Table 15. Abbreviations

Acronym	Description
ADS	Advanced Design System
CW	Continuous Wave
DUT	Device Under Test
ESD	ElectroStatic Discharge
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MTF	Median Time to Failure
MWO	Microwave Office
PTFE	Polytetrafluorethylene
SMD	Surface Mounted Device
RoHS	Restriction of Hazardous Substances
SiC	Silicon Carbide
VSWR	Voltage Standing Wave Ratio

12. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CLF3H0060-30_3H0060S-30 v.1	20211220	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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15. Contents

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