BLU9H0408L-800P

UHF power LDMOS transistor

Rev. 2 — 14 October 2024

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 800 W LDMOS power transistor for UHF radar applications in the frequency range from 400 MHz to 800 MHz.

Table 1. Typical performance

RF performance at T_{case} = 25 °C; t_p = 100 µs; δ = 10 %; I_{Dq} = 1300 mA; in a class-AB demo circuit.

Test signal	f	I_{Dq}	V_{DS}	P_L	G_p	η_D
	(MHz)	(mA)	(V)	(W)	(dB)	(%)
pulsed RF	410 to 460	1300	50	800	21.9	70.4
	700	1300	50	750	20.3	67.2

1.2 Features and benefits

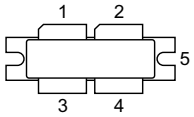
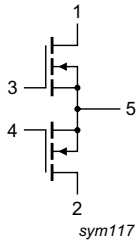
- Designed for broadband in UHF radar applications
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Excellent stability
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for UHF radar applications in the 400 MHz to 800 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLU9H0408L-800P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	108	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; V_{DS} = 50 V; P_L = 300 W	0.13	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.4 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 240 mA	1.5	2.2	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	41	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 8.5 A	-	90	-	mΩ

Table 7. AC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	368	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	69	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	0.86	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 10 % at V_{DS} = 50 V; I_{Dq} = 1300 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production circuit measured at frequency of 700 MHz.

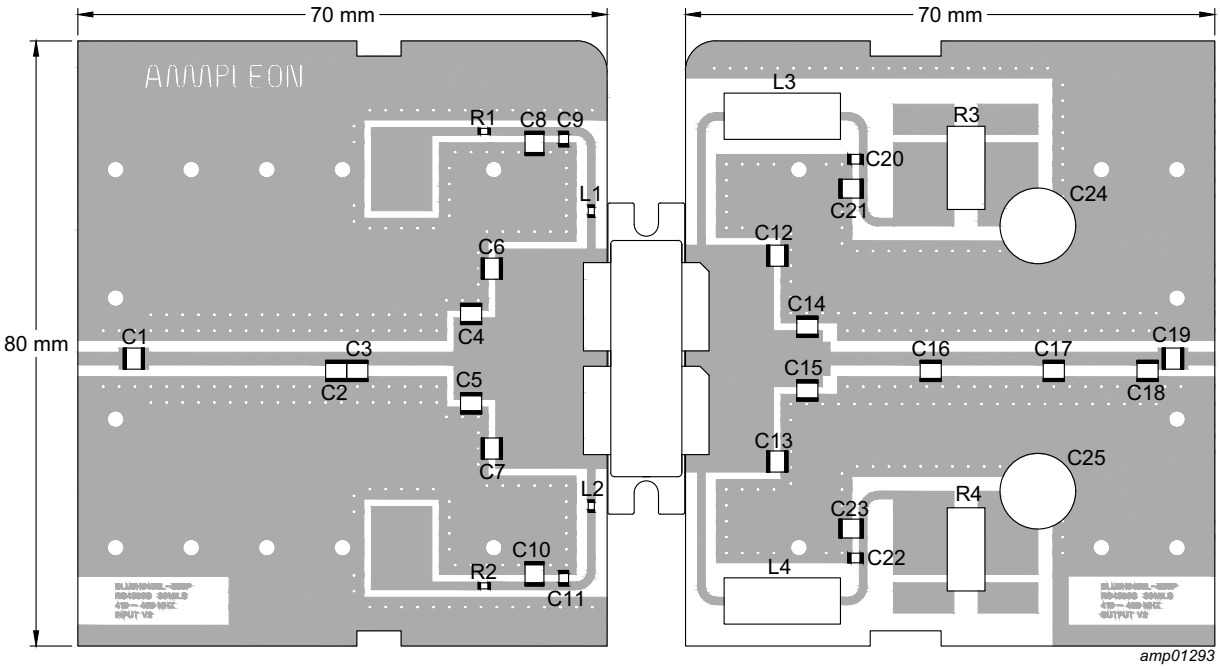
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 750 W	19.5	20.5	-	dB
RL_{in}	input return loss	P_L = 750 W	-	−7	-	dB
η_D	drain efficiency	P_L = 750 W	64	67.5	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLU9H0408L-800P is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 1300 mA; P_L = 750 W (pulsed CW); f = 700 MHz. Pulsed conditions: t_p = 100 μs; δ = 10 %.

7.2 Test circuit



Printed-Circuit Board (PCB): RO4350B: height = 0.762 mm. See Table 9 for a list of components.

Fig 1. Component layout for test circuit

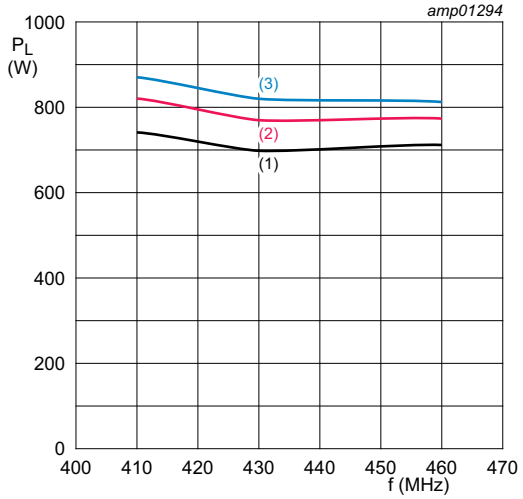
Table 9. List of components

See Figure 1 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	36 pF	
C2	multilayer ceramic chip capacitor	3.6 pF	
C3	multilayer ceramic chip capacitor	24 pF	
C4, C5	multilayer ceramic chip capacitor	33 pF	
C6, C7	multilayer ceramic chip capacitor	56 pF	
C8, C10, C21, C23	multilayer ceramic chip capacitor	4.7 μF	
C9, C11, C20, C22	multilayer ceramic chip capacitor	0.1 μF	
C12, C13	multilayer ceramic chip capacitor	13 pF	
C14, C15	multilayer ceramic chip capacitor	56 pF	
C16	multilayer ceramic chip capacitor	20 pF	
C17	multilayer ceramic chip capacitor	1.0 pF	
C18	multilayer ceramic chip capacitor	1.8 pF	
C19	multilayer ceramic chip capacitor	11 pF	
C24, C25	electrolytic capacitor	1000 μF	
L1, L2	wire wound surface mount inductor	56 nH	
L3, L4	6 turn air core inductor	150 nH	
R1, R2	surface mount resistor	5.6 Ω	
R3, R4	current sense resistor	5 mΩ	

7.3 Graphical data

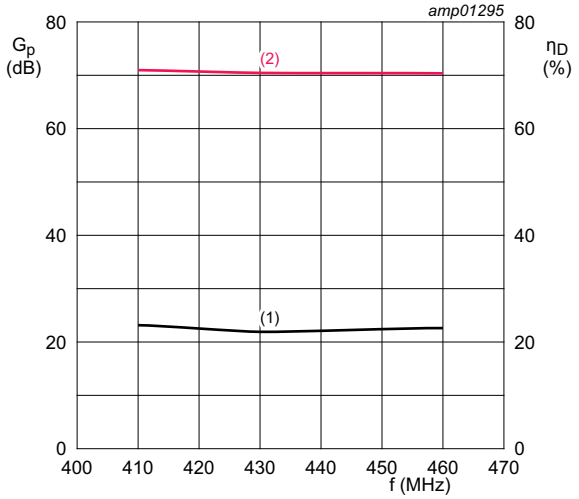
7.3.1 Pulsed CW performance (f = 410 MHz to 460 MHz)



V_{DS} = 50 V; I_{Dq} = 1300 mA; t_p = 100 µs; δ = 10 %.

(1) $P_{L(1dB)}$
(2) $P_{L(2dB)}$
(3) $P_{L(3dB)}$

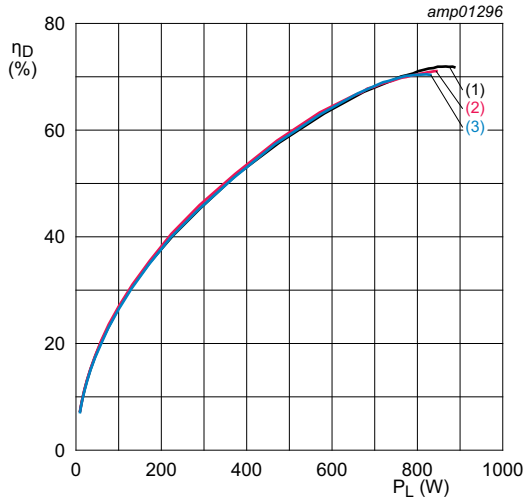
Fig 2. Output power at gain compression as a function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 1300 mA; P_L = 800 W; t_p = 100 µs; δ = 10 %.

(1) G_p
(2) η_D

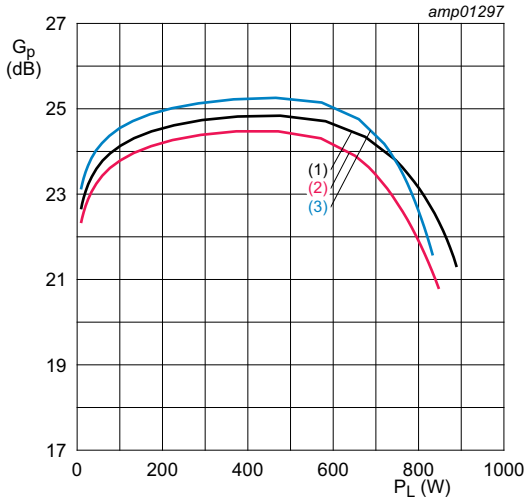
Fig 3. Power gain and drain efficiency as function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 1300 mA; t_p = 100 µs; δ = 10 %.

(1) f = 410 MHz
(2) f = 430 MHz
(3) f = 460 MHz

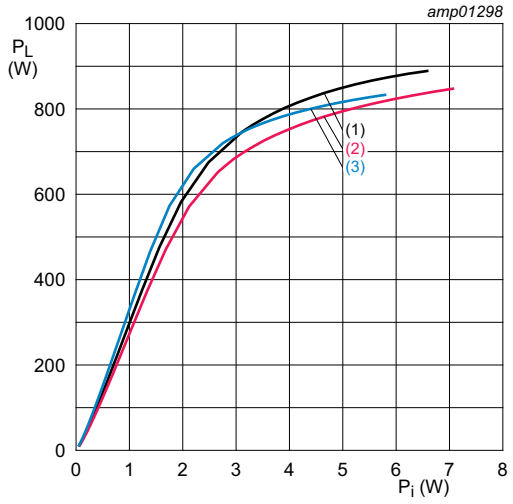
Fig 4. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 1300 mA; t_p = 100 µs; δ = 10 %.

(1) f = 410 MHz
(2) f = 430 MHz
(3) f = 460 MHz

Fig 5. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 1300 mA; t_p = 100 μs; δ = 10 %.

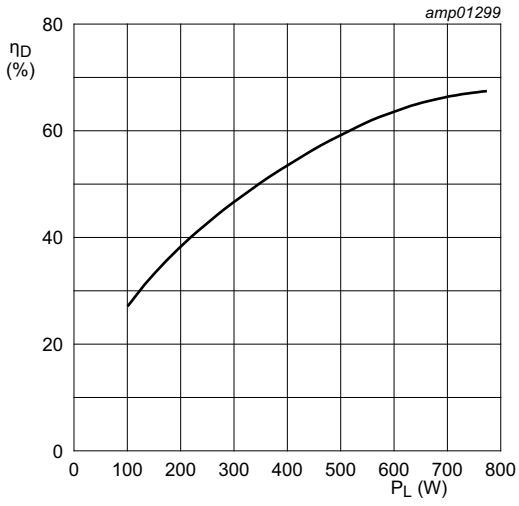
(1) f = 410 MHz

(2) f = 430 MHz

(3) f = 460 MHz

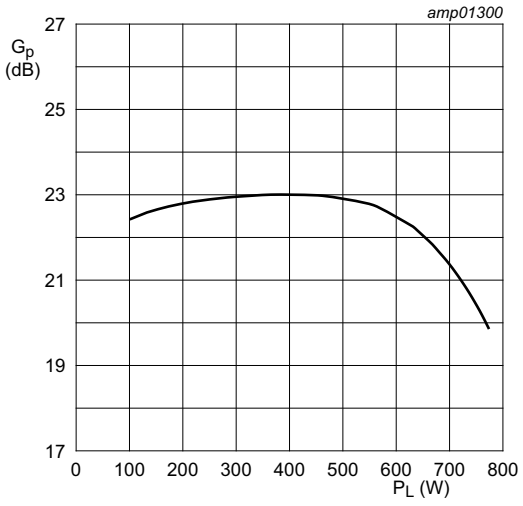
Fig 6. Output power as a function of input power; typical values

7.3.2 Pulsed CW performance (f = 700 MHz)



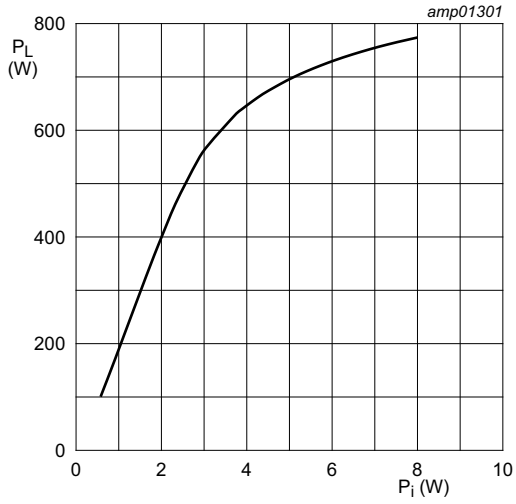
V_{DS} = 50 V; I_{Dq} = 1300 mA; t_p = 100 μs; δ = 10 %.

Fig 7. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 1300 mA; t_p = 100 μs; δ = 10 %.

Fig 8. Power gain as a function of output power; typical values

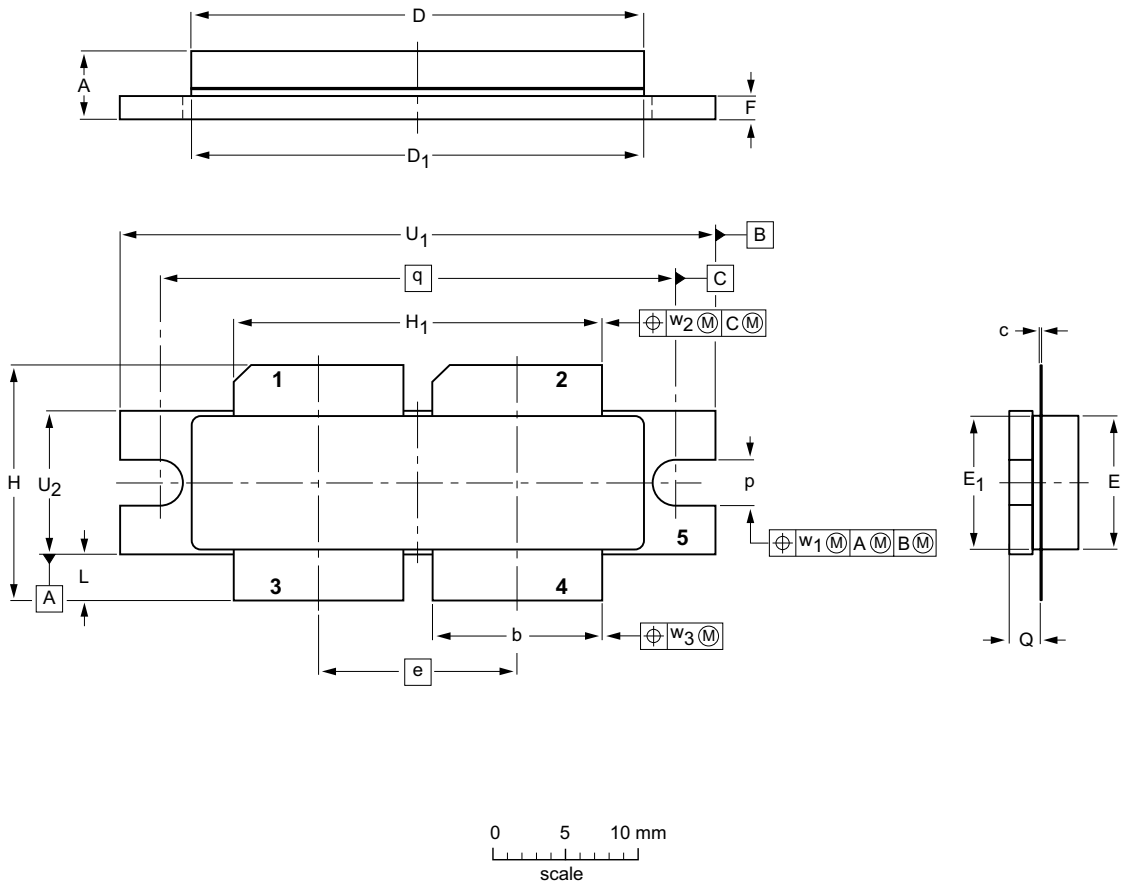


V_{DS} = 50 V; I_{Dq} = 1300 mA; t_p = 100 μs; δ = 10 %.

Fig 9. Output power as a function of input power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 10. Package outline SOT539A

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
UHF	Ultra High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLU9H0408L-800P v.2	20241014	Product data sheet	-	BLU9H0408L-800P v.1
Modifications:	• Table 4 on page 2: updated the value for V_{DS} • Table 7 on page 3: added table			
BLU9H0408L-800P v.1	20200326	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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