BLS9G2735S-15G

Power LDMOS transistor

Rev. 1 — 23 July 2019

AMPLEON

Product data sheet

1. Product profile

1.1 General description

15 W LDMOS power transistor for S-band applications in the frequency range from 2700 MHz to 3500 MHz.

Table 1. Typical performance

RF performance at T_{case} = 25 °C; t_p = 100 µs; δ = 10 %; I_{Dq} = 70 mA; in a common source class-AB production test circuit.

Test signal	f	I_{Dq}	V_{DS}	P_L	G_p	η_D
	(MHz)	(mA)	(V)	(W)	(dB)	(%)
pulsed RF	2700 to 3100	70	32	15	14	55
	3100 to 3500	70	32	15	14	52
	3100	70	32	15	14	59

1.2 Features and benefits

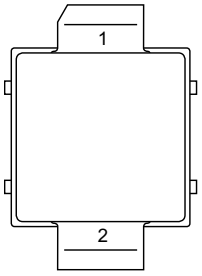
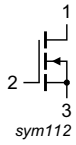
- High efficiency
- Integrated ESD protection
- Excellent ruggedness
- Excellent thermal stability
- Designed for broadband operation in S-band radar applications
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for S-band radar applications in the 2700 MHz to 3500 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS9G2735S-15G	-	earless flanged ceramic package; 2 leads	SOT975C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−6	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal resistance from junction to case	T_{case} = 80 °C; P_L = 15 W		
		t_p = 100 µs; δ = 10 %	1.3	K/W
		t_p = 200 µs; δ = 10 %	1.6	K/W
		t_p = 300 µs; δ = 10 %	1.8	K/W
		t_p = 500 µs; δ = 10 %	2.1	K/W
		t_p = 100 µs; δ = 20 %	1.7	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.11 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 10.5 mA	1.5	2	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	2.2	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.53 A	-	0.78	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 368 mA	-	1200	-	mΩ

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 100 µs; δ = 10 % at V_{DS} = 32 V; I_{Dq} = 70 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production circuit measured at frequency of 3100 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 15 W	11.5	14	-	dB
RL_{in}	input return loss	P_L = 15 W	-	−11	-	dB
η_D	drain efficiency	P_L = 15 W	52	59	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLS9G2735S-15G is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 70 mA; P_L = 15 W (pulsed CW); f = 2900 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data of device; I_{Dq} = 70 mA (main); V_{DS} = 32 V; pulsed CW (t_p = 100 μs: δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2700	1.9 – j10.0	7.2 – j3.3	15.5	55.9	17.5
2800	2.2 – j10.8	7.2 – j4.0	15.2	54.8	18.1
2900	2.5 – j11.8	6.5 – j5.1	15.9	56.4	18.3
3000	2.9 – j13.3	6.2 – j6.0	15.7	56.5	18.9
3100	4.5 – j15.2	6.2 – j7.2	16.4	56.9	19.2
3200	6.7 – j15.4	6.7 – j7.7	15.6	54.7	19.1
3300	9.5 – j15.8	6.9 – j8.5	16.1	55.4	19.0
3400	13.5 – j12.0	6.6 – j9.1	15.4	54.6	19.2
3500	13.0 – j7.4	7.0 – j10.0	15.6	54.3	18.9
Maximum drain efficiency load					
2700	1.9 – j10.0	4.8 – j1.4	12.8	60.1	19.7
2800	2.2 – j10.8	3.6 – j2.6	12.5	61.2	19.9
2900	2.5 – j11.8	3.7 – j3.7	13.3	62.7	20.1
3000	2.9 – j13.3	3.7 – j4.5	12.8	61.9	21.1
3100	4.5 – j15.2	3.9 – j5.6	13.5	62.5	21.3
3200	6.7 – j15.4	4.1 – j6.6	13.3	59.9	20.7
3300	9.5 – j15.8	3.8 – j7.7	13.2	60.5	21.2
3400	13.5 – j12.0	4.3 – j8.2	13.0	57.8	20.8
3500	13.0 – j7.4	4.2 – j9.5	13.0	57.7	20.4

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

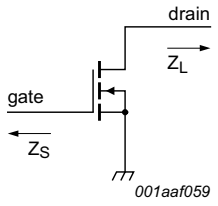
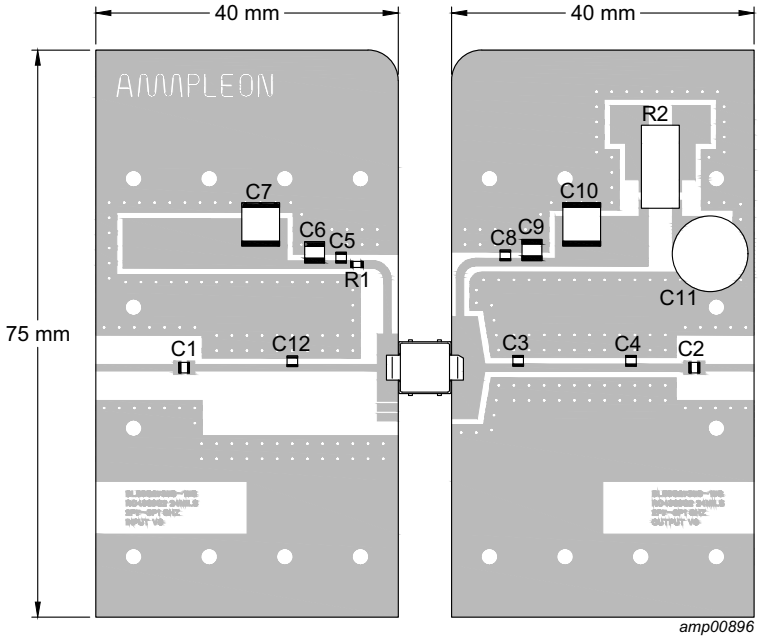


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4360G2; thickness = 0.61 mm.

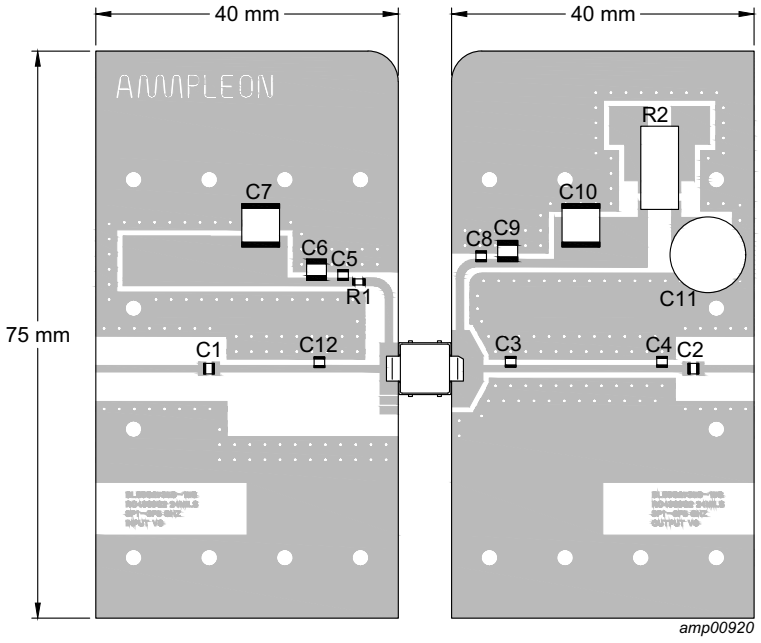
See Table 9 for a list of components.

Fig 2. Component layout for test circuit f = 2700 MHz to 3100 MHz

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	1 pF	
C2	multilayer ceramic chip capacitor	4.7 pF	
C3	multilayer ceramic chip capacitor	1.1 pF	
C4	multilayer ceramic chip capacitor	0.1 pF	
C5, C8	multilayer ceramic chip capacitor	15 pF	
C6, C9	multilayer ceramic chip capacitor	1 nF	
C7, C10	multilayer ceramic chip capacitor	10 μF	
C11	electrolytic capacitor	1000 μF	
C12	multilayer ceramic chip capacitor	0.8 pF	
R1	SMD resistor	5 Ω	
R2	current sense resistor	5 mΩ	



Printed-Circuit Board (PCB): Rogers RO4360G2; thickness = 0.61 mm.

See Table 10 for a list of components.

Fig 3. Component layout for test circuit f = 3100 MHz to 3500 MHz

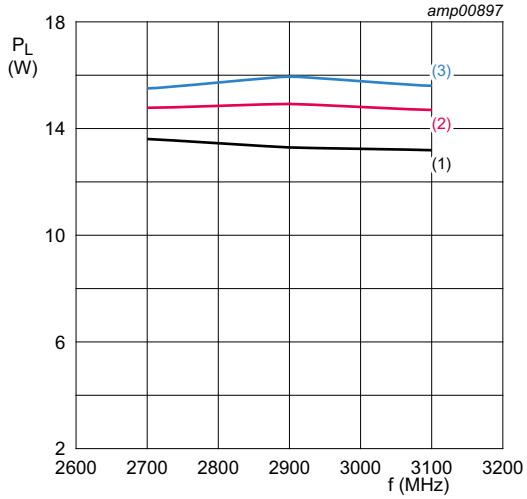
Table 10. List of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	22 pF	
C2	multilayer ceramic chip capacitor	4.7 pF	
C3	multilayer ceramic chip capacitor	0.5 pF	
C4	multilayer ceramic chip capacitor	0.1 pF	
C5, C8	multilayer ceramic chip capacitor	15 pF	
C6, C9	multilayer ceramic chip capacitor	1 nF	
C7, C10	multilayer ceramic chip capacitor	10 μF	
C11	electrolytic capacitor	1000 μF	
C12	multilayer ceramic chip capacitor	0.5 pF	
R1	SMD resistor	5 Ω	
R2	current sense resistor	5 mΩ	

7.4 Graphical data

7.4.1 Pulsed CW; f = 2700 MHz to 3100 MHz



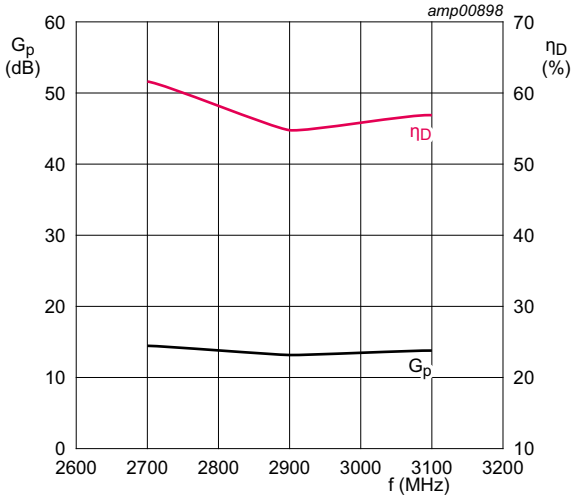
V_{DS} = 32 V; I_{Dq} = 70 mA; t_p = 100 µs; δ = 10 %.

(1) at $P_{L(1dB)}$

(2) at $P_{L(2dB)}$

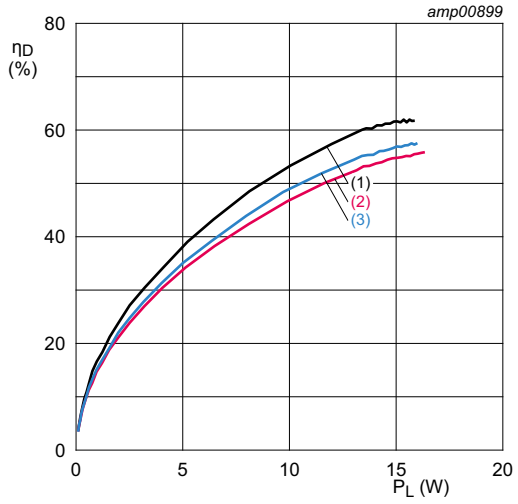
(3) at $P_{L(3dB)}$

Fig 4. Output power as a function of frequency; typical values



V_{DS} = 32 V; I_{Dq} = 70 mA; P_L = 15 W; t_p = 100 µs; δ = 10 %.

Fig 5. Power gain and drain efficiency as function of frequency; typical values



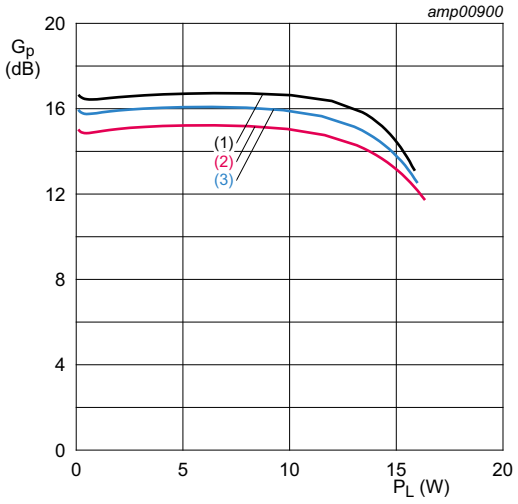
V_{DS} = 32 V; I_{Dq} = 70 mA; t_p = 100 µs; δ = 10 %.

(1) f = 2700 MHz

(2) f = 2900 MHz

(3) f = 3100 MHz

Fig 6. Drain efficiency as a function of output power; typical values



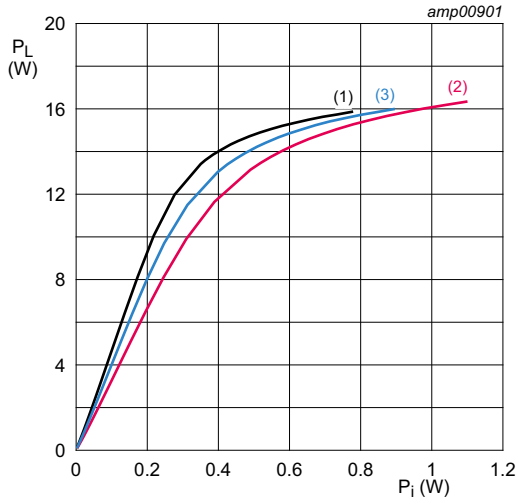
V_{DS} = 32 V; I_{Dq} = 70 mA; t_p = 100 µs; δ = 10 %.

(1) f = 2700 MHz

(2) f = 2900 MHz

(3) f = 3100 MHz

Fig 7. Power gain as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 70 mA; t_p = 100 μs; δ = 10 %.

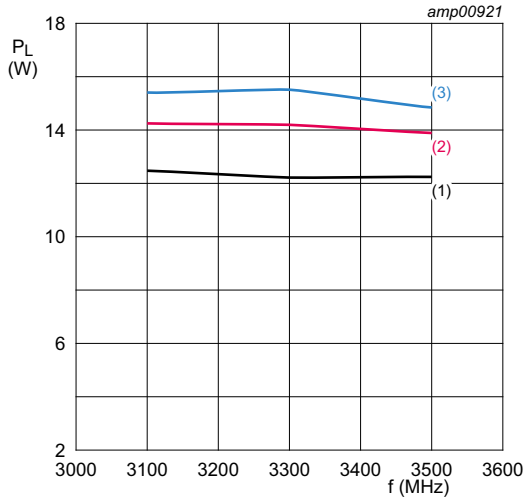
(1) f = 2700 MHz

(2) f = 2900 MHz

(3) f = 3100 MHz

Fig 8. Output power as a function of input power; typical values

7.4.2 Pulsed CW; f = 3100 MHz to 3500 MHz



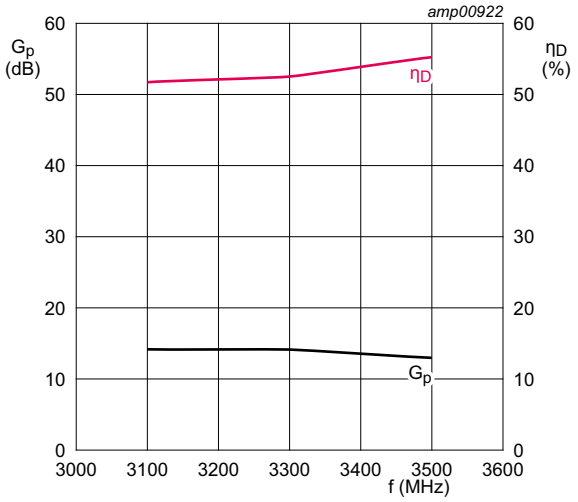
V_{DS} = 32 V; I_{Dq} = 70 mA; t_p = 100 μs; δ = 10 %.

(1) at $P_{L(1dB)}$

(2) at $P_{L(2dB)}$

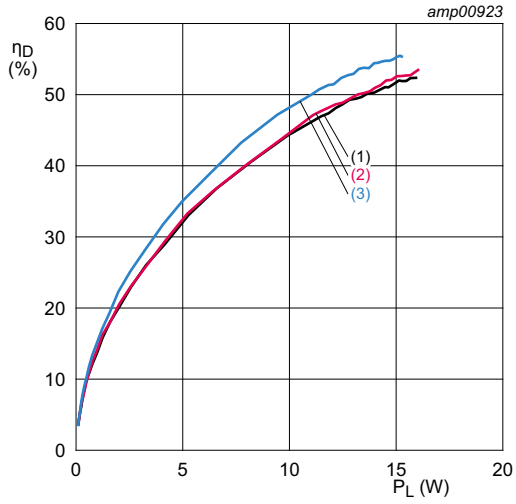
(3) at $P_{L(3dB)}$

Fig 9. Output power as a function of frequency; typical values



V_{DS} = 32 V; I_{Dq} = 70 mA; P_L = 15 W; t_p = 100 μs; δ = 10 %.

Fig 10. Power gain and drain efficiency as function of frequency; typical values



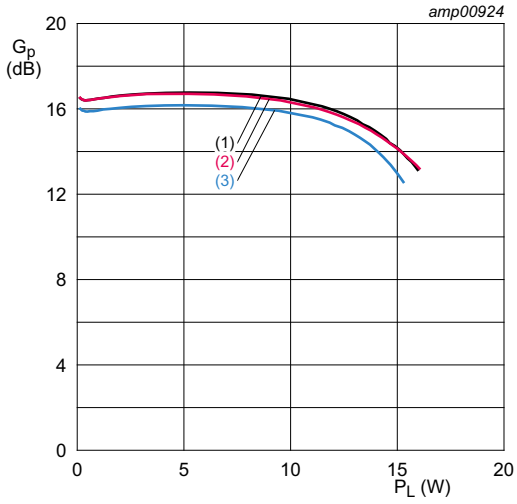
V_{DS} = 32 V; I_{Dq} = 70 mA; t_p = 100 μs; δ = 10 %.

(1) f = 3100 MHz

(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 11. Drain efficiency as a function of output power; typical values



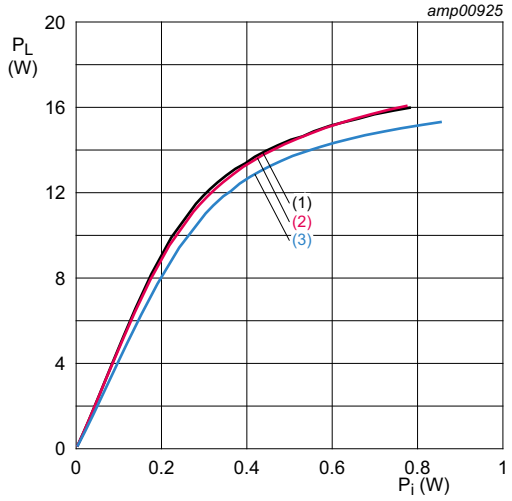
V_{DS} = 32 V; I_{Dq} = 70 mA; t_p = 100 μs; δ = 10 %.

(1) f =3100 MHz

(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 12. Power gain as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 70 mA; t_p = 100 μs; δ = 10 %.

(1) f = 3100 MHz

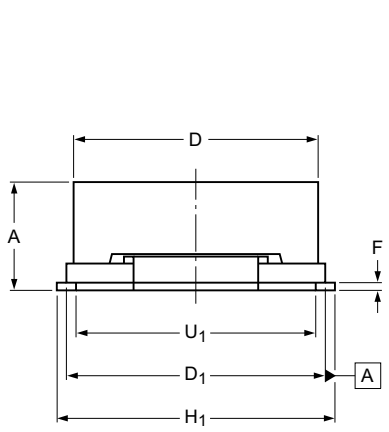
(2) f = 3300 MHz

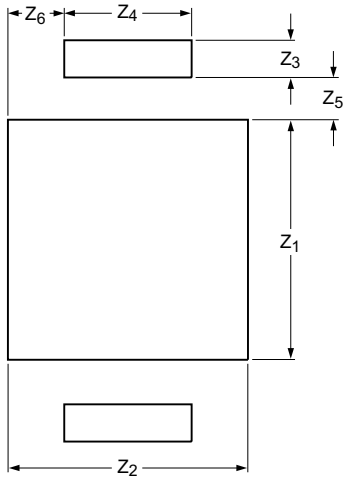
(3) f = 3500 MHz

Fig 13. Output power as a function of input power; typical values

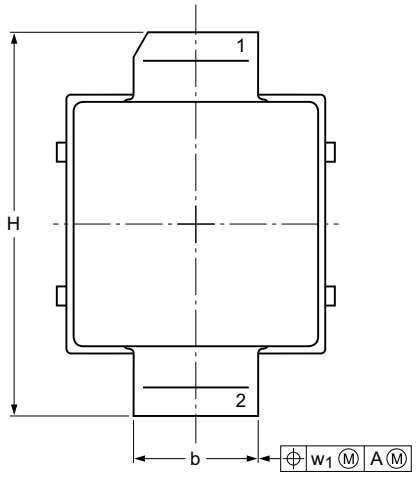
8. Package outline

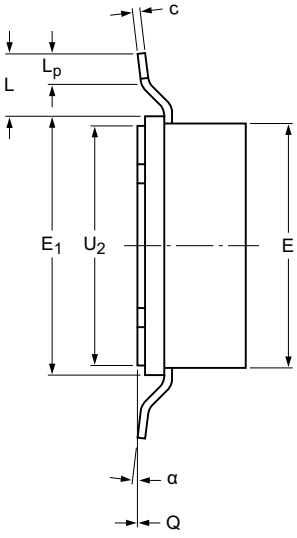
Earless flanged ceramic package; 2 leads **SOT975C**

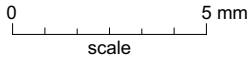




minimal dimensions for solder pattern







Z4	Z5	Z6	α
			7°
3.30	1.14	1.52	0°
			7°
0.130	0.045	0.060	0°

Dimensions (mm dimensions are derived from the original inch dimensions)

Unit		A	b	c	D	D_1	E	E_1	F	H	H_1	L	L_p	Q	U_1	U_2	w_1	Z_1	Z_2	Z_3
mm	max	3.15	3.38	0.23	6.55	6.93	6.55	6.93	0.23	10.29	7.49		1.02	+0.05	6.43	6.43				
	nom											1.65					0.51	6.35	6.35	1.02
	min	2.59	3.23	0.18	6.40	6.78	6.40	6.78	0.18	10.03	6.73		0.51	-0.05	6.27	6.27				
inches	max	0.124	0.133	0.009	0.258	0.273	0.258	0.273	0.009	0.405	0.295		0.040	+0.002	0.253	0.253				
	nom											0.065					0.020	0.250	0.250	0.040
	min	0.102	0.127	0.007	0.252	0.267	0.252	0.267	0.007	0.395	0.265		0.020	-0.002	0.247	0.247				

sot975c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT975C						~~08-07-10~~ 14-10-13

Fig 14. Package outline SOT975C

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
S-band	Short wave band
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS9G2735S-15G v.1	20190723	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

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