BLP9H10S-500AWT

Power LDMOS transistor

Rev. 2 — 18 December 2020

Product data sheet

1. Product profile

1.1 General description

500 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 600 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty circuit; V_{DS} = 48 V; I_{Dq} = 200 mA (main); $V_{GS(amp)peak}$ = 0.3 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	758 to 821	48	50.1	17.6	52.4	–29.8 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

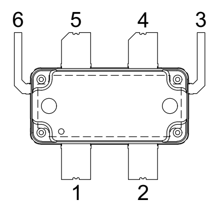
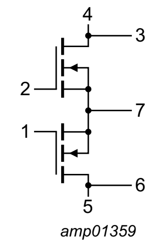
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internal integrated wideband input and output matching for ease of use
- Integrated double sided ESD protection
- Bias through video leads
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 600 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1, 2	gate		
3, 6	decoupling lead		
4, 5	drain		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP9H10S-500AWT	-	overmolded plastic earless flanged package; 6 leads	OMP-780-6F-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	105	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 48 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.3 V; T_{case} = 80 °C		
		P_L = 76 W	0.55	K/W
		P_L = 85 W	0.51	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.5 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 150 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 48 V; I_D = 500 mA	1.55	2.07	2.55	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	23.8	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.5 A	-	10.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.25 A	-	154	250	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.2 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 220 mA	1.5	1.9	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 48 V; I_D = 1100 mA	1.5	1.99	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	34.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11 A	-	15.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.7 A	-	109	174	mΩ

Table 7. RF characteristics

A derivative functional RF test is performed in production. The performance as mentioned below is based on an asymmetrical Doherty application board and correlated to the production circuit. Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; f_1 = 793.5 MHz; f_2 = 818.5 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.3 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty test circuit at frequencies from 791 MHz to 821 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 76 W	17.5	18.3	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 76 W	-	–12.7	–9	dB
η_D	drain efficiency	$P_{L(AV)}$ = 76 W	47	51	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 76 W	-	–34.8	–32	dBc

Table 8. RF characteristics

A derivative functional RF test is performed in production. The performance as mentioned below is based on an asymmetrical Doherty application board and correlated to the production circuit. Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; f_1 = 793.5 MHz; f_2 = 818.5 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.3 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty test circuit at frequencies from 791 MHz to 821 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 135 W	6.2	6.7	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 135 W	550	620	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLP9H10S-500AWT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.3 V; f = 791 MHz; P_L = 200 W (5 dB OBO); 1-carrier W-CDMA signal; f_c = 791 MHz; 100 % clipping.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 600 mA (main); V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
600	5.3 – j1.02	4.0 – j3.1	325.5	65.7	18.0
617	4.9 – j0.7	4.0 – j3.1	322.3	65.1	18.3
635	4.4 – j0.69	4.0 – j3.1	299.8	61.0	18.3
652	4.1 – j0.69	3.0 – j2.4	260.2	52.9	17.6
698	3.5 – j1.25	3.0 – j2.4	321.7	65.1	18.7
746	3.3 – j1.92	3.0 – j2.4	316.8	66.0	18.7
769	3.3 – j2.26	3.0 – j2.4	312.4	66.9	18.8
805	3.4 – j2.77	3.0 – j2.4	295.2	66.7	19.0
820	3.5 – j3.02	3.0 – j2.4	295.5	67.9	19.0
869	4.1 – j3.74	2.9 – j3.8	293.2	59.5	17.9
880	4.3 – j3.85	2.9 – j3.8	292.0	60.7	18.0
894	4.6 – j4.03	2.9 – j3.8	288.0	60.5	18.0
915	5.0 – j4.22	2.8 – j3.8	284.9	61.7	18.1
925	5.3 – j4.27	2.9 – j3.8	281.2	63.1	18.2
942	5.8 – j4.32	3.6 – j4.9	277.9	59.7	17.8
960	6.4 – j4.28	3.7 – j4.9	273.1	59.9	18.0

Table 9. Typical impedance of main device *…continued*

Measured load-pull data of main device; I_{Dq} = 600 mA (main); V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [2] (dB)
Maximum drain efficiency load					
600	4.8 – j1.33	11.3 – j5.5	172.5	70.9	20.6
617	4.6 – j0.90	8.4 – j3.6	217.9	69.9	20.1
635	4.3 – j0.74	6.3 – j2.6	249.6	66.4	19.6
652	3.9 – j0.80	6.2 – j2.5	202.3	59.4	19.4
698	3.4 – j1.47	6.7 – j0.4	194.9	71.8	21.0
746	3.2 – j2.07	5.0 – j0.3	214.0	72.7	20.7
769	3.2 – j2.37	5.0 – j0.3	206.7	72.5	20.7
805	3.3 – j2.82	3.7 – j0.2	198.4	72.3	20.7
820	3.4 – j3.06	3.7 – j0.2	197.6	72.1	20.7
869	4.0 – j3.78	3.5 – j0.2	175.3	71.1	20.7
880	4.2 – j3.86	3.3 – j1.3	211.1	70.1	20.1
894	4.5 – j3.97	3.3 – j1.3	197.0	69.2	20.2
915	4.9 – j4.12	3.2 – j1.3	184.8	69.1	20.2
925	5.2 – j4.14	3.2 – j1.3	176.3	69.2	20.4
942	5.7 – j4.20	2.8 – j2.2	200.7	68.0	19.9
960	6.3 – j4.08	2.8 – j2.2	186.2	67.2	20.1

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

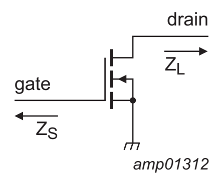


Fig 1. Definition of transistor impedance

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 880 mA (peak); V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
600	3.6 – j1.13	2.4 – j3.8	453.6	59.5	17.1
617	3.3 – j1.06	2.4 – j3.8	438.9	57.9	17.4
698	2.9 – j1.78	1.8 – j3.1	445.0	58.2	17.2
746	3.0 – j2.21	1.8 – j3.1	435.8	59.4	17.5
769	3.2 – j2.38	2.4 – j3.8	428.1	61.6	17.8
800	3.4 – j2.56	2.4 – j3.8	416.7	61.9	17.9
805	3.4 – j2.61	2.4 – j3.8	434.3	63.3	17.9
820	3.6 – j2.64	2.4 – j3.8	430.1	63.5	17.8
869	4.3 – j2.57	2.4 – j3.8	408.4	64.4	18.0
880	4.4 – j2.47	2.4 – j3.8	402.0	64.4	18.1
894	4.6 – j2.28	2.3 – j3.8	388.3	64.0	18.3
915	5.0 – j1.89	1.5 – j4.3	382.7	54.3	16.9
942	5.0 – j1.31	1.9 – j5.1	381.3	52.5	16.5
960	4.9 – j0.83	1.9 – j5.2	378.2	53.7	16.8
Maximum drain efficiency load					
600	3.5 – j1.19	4.0 – j3.9	399.5	69.1	18.7
617	3.1 – j1.12	5.0 – j2.9	346.6	68.7	19.7
698	2.8 – j1.85	3.8 – j2.2	336.0	70.9	19.6
746	2.9 – j2.22	2.9 – j1.7	326.6	70.1	19.6
769	3.0 – j2.38	2.9 – j1.7	306.2	69.9	19.7
800	3.3 – j2.54	2.9 – j1.7	278.3	68.9	20.0
805	3.3 – j2.78	2.3 – j0.7	263.7	73.8	20.5
820	3.5 – j2.62	2.9 – j1.7	299.2	72.5	20.0
869	4.2 – j2.42	2.9 – j1.7	257.3	70.1	20.1
880	4.4 – j2.38	2.4 – j2.5	312.8	69.8	19.5
894	4.5 – j2.15	2.4 – j2.5	293.7	68.4	19.7
915	4.7 – j1.72	2.4 – j2.5	270.8	68.0	19.8
942	4.5 – j1.12	2.4 – j2.5	238.7	66.1	19.9
960	4.6 – j0.78	2.4 – j3.8	318.0	64.1	18.9

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 750 mA (main); V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
720	3.3 – j1.7	3.6 – j2.1	304	35.1	22.6
800	3.5 – j3.0	3.5 – j2.3	303	34.9	22.5
820	3.7 – j3.4	3.4 – j2.3	298	35.3	21.9
869	4.5 – j4.2	3.0 – j2.2	297	39.3	22.5
894	5.1 – j4.5	3.1 – j2.0	295	37.4	22.2

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 76 W.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; I_{Dq} = 750 mA (main); V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
720	3.2 – j2.0	6.6 + j1.4	172	49.2	24.8
800	3.4 – j3.1	5.4 + j1.1	172	50.8	24.0
820	3.7 – j3.4	4.9 + j1.0	174	50.5	24.0
869	4.5 – j4.3	3.7 + j0.4	174	54.3	24.1
894	5.1 – j4.6	3.6 + j0.4	175	52.6	24.1

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 76 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; I_{Dq} = 1100 mA (peak); V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
720	2.7 – j2.0	3.0 – j2.4	401	34.3	22.8
800	3.2 – j2.5	2.8 – j2.7	400	32.0	22.1
820	3.4 – j2.6	2.5 – j3.0	412	30.8	21.6
869	4.1 – j2.6	2.4 – j3.2	399	30.6	21.5
894	4.5 – j2.4	2.3 – j3.3	387	30.9	21.3

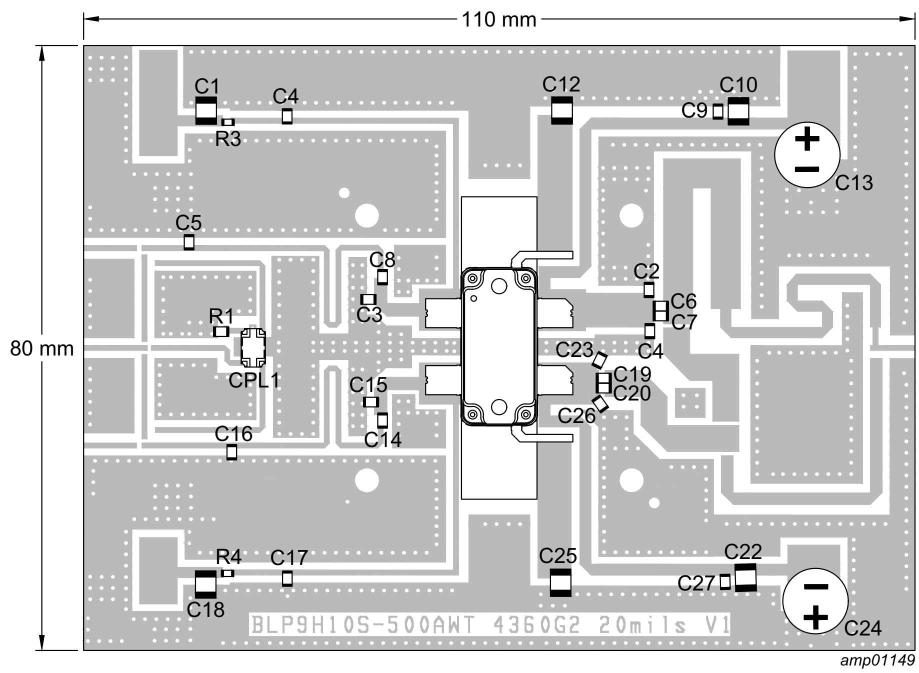
[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 76 W.

Table 14. Off-state impedances of peak device

f	Z_{off}
(MHz)	**(Ω)**
600	1.9 + j14.7
698	83.9 – j20.5
720	24.9 – j37.2
769	3.9 – j14.7
800	2.1 – j9.9
820	1.6 – j7.9
869	0.9 – j4.7
880	0.9 – j4.3
894	0.8 – j3.9
925	0.6 – j2.9
942	0.6 – j2.3
960	0.5 – j1.9

7.4 Test circuit



Printed-Circuit Board (PCB): RO4360: ε_r = 6.15; thickness = 0.508 mm; thickness copper plating = 35 μm. See Table 15 for a list of components.

Fig 2. Component layout

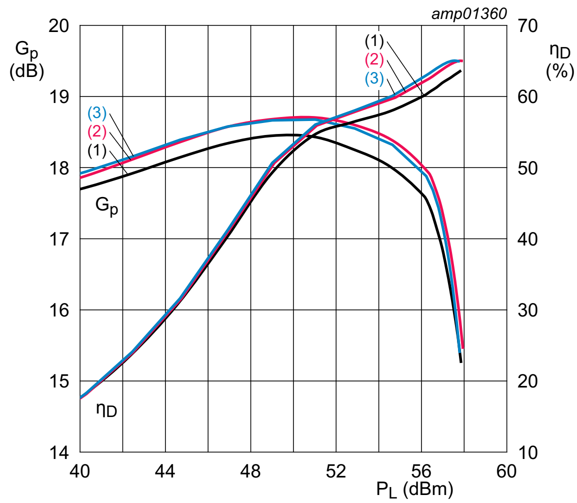
Table 15. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C10, C12, C18, C22, C25	multilayer ceramic chip capacitor	4.7 μF	Murata: SMD 1210
C2, C4	multilayer ceramic chip capacitor	5.1 pF	Murata: Hi-Q SMD 0805
C3	multilayer ceramic chip capacitor	8 pF	Murata: Hi-Q SMD 0805
C4, C9, C17, C27	multilayer ceramic chip capacitor	100 pF	Murata: Hi-Q SMD 0805
C5	multilayer ceramic chip capacitor	1.5 pF	Murata: Hi-Q SMD 0805
C6, C7, C19, C20	multilayer ceramic chip capacitor	100 pF	Murata: Hi-Q SMD 0805
C8	multilayer ceramic chip capacitor	10 pF	Murata: Hi-Q SMD 0805
C13, C24	electrolytic capacitor	470 μF, 63 V	
C14	multilayer ceramic chip capacitor	6.2 pF	Murata: Hi-Q SMD 0805
C15	multilayer ceramic chip capacitor	11 pF	Murata: Hi-Q SMD 0805
C16	multilayer ceramic chip capacitor	3.3 pF	Murata: Hi-Q SMD 0805
C23, C26	multilayer ceramic chip capacitor	8.2 pF	Murata: Hi-Q SMD 0805
R1	termination	50 Ω	Anaren: C16A50Z4
R3, R4	resistor	5.1 Ω, 1 %	SMD 805
CPL1	hybrid coupler	2 dB; 90°	Anaren: Xinger III, X3C07F1-02S

7.5 Graphical data

7.5.1 Pulsed CW



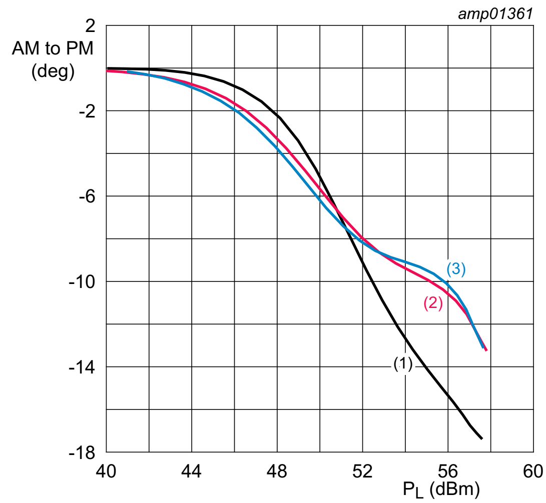
V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.34 V;
t_p = 100 μs; δ = 10 %.

(1) f = 758 MHz

(2) f = 798 MHz

(3) f = 821 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.34 V;
t_p = 100 μs; δ = 10 %.

(1) f = 758 MHz

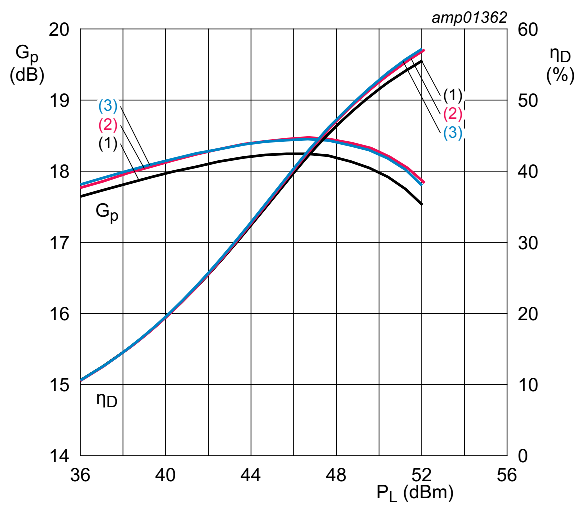
(2) f = 798 MHz

(3) f = 821 MHz

Fig 4. Normalized AM to PM as a function of output power; typical values

7.5.2 1-Carrier W-CDMA

PAR = 9.9 dB per carrier at 0.01 % probability on CCDF; 3GPP test model 1 with 64 DPCH (100 % clipping).



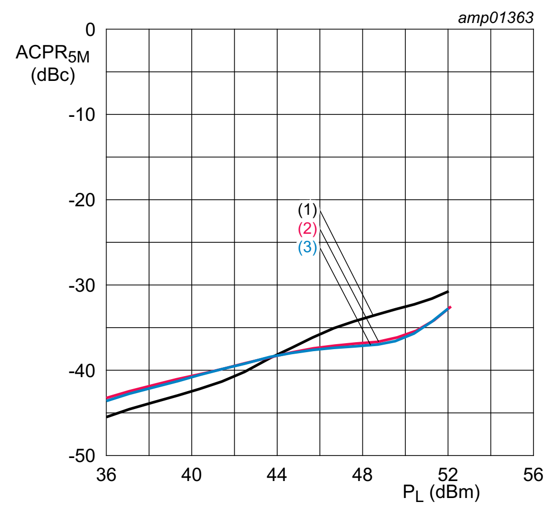
V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.34 V.

(1) f = 758 MHz

(2) f = 798 MHz

(3) f = 821 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



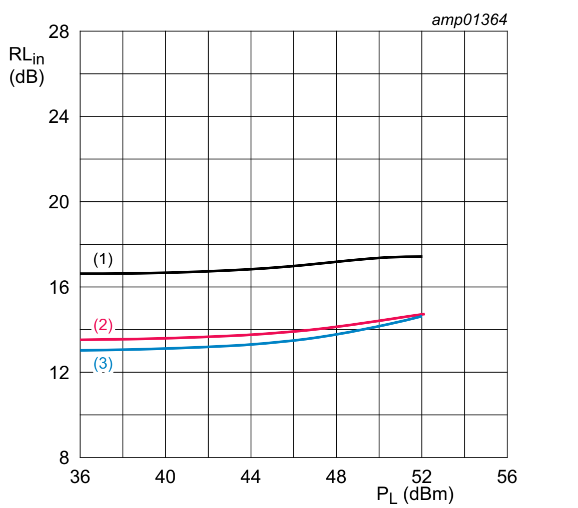
V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.34 V.

(1) f = 758 MHz

(2) f = 798 MHz

(3) f = 821 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



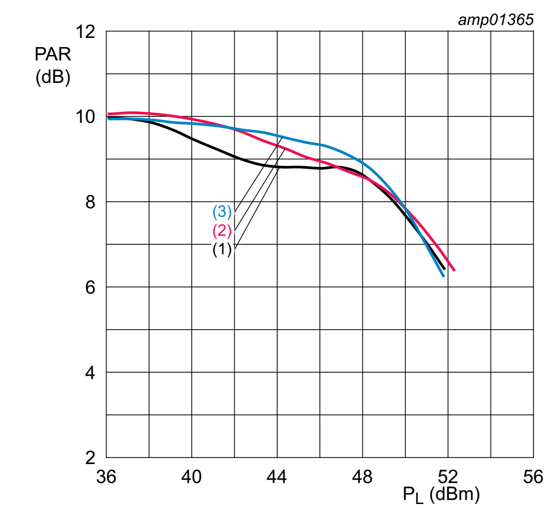
V_{DS} = 48 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.34 V.

(1) f = 758 MHz

(2) f = 798 MHz

(3) f = 821 MHz

Fig 7. Input return loss as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 500 mA; $V_{GS(amp)peak}$ = 0.4 V.

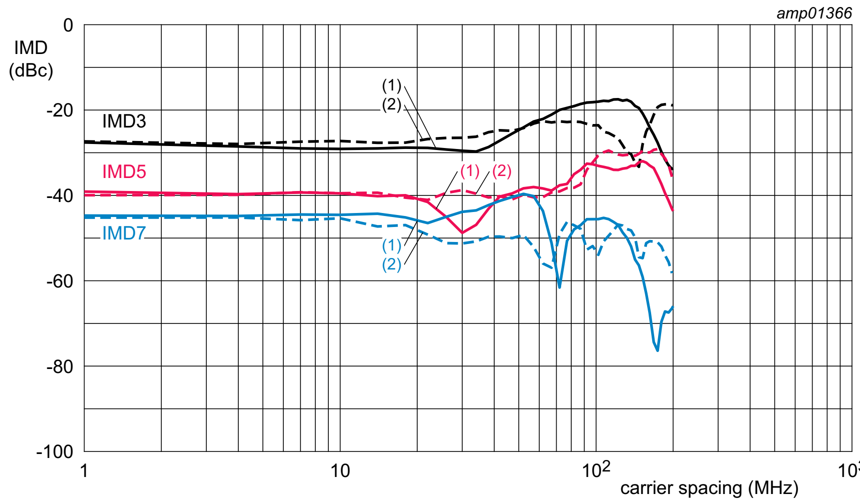
(1) f = 746 MHz

(2) f = 798 MHz

(3) f = 859 MHz

Fig 8. Peak-to-average power ratio as a function of output power; typical values

7.5.3 2-Tone VBW



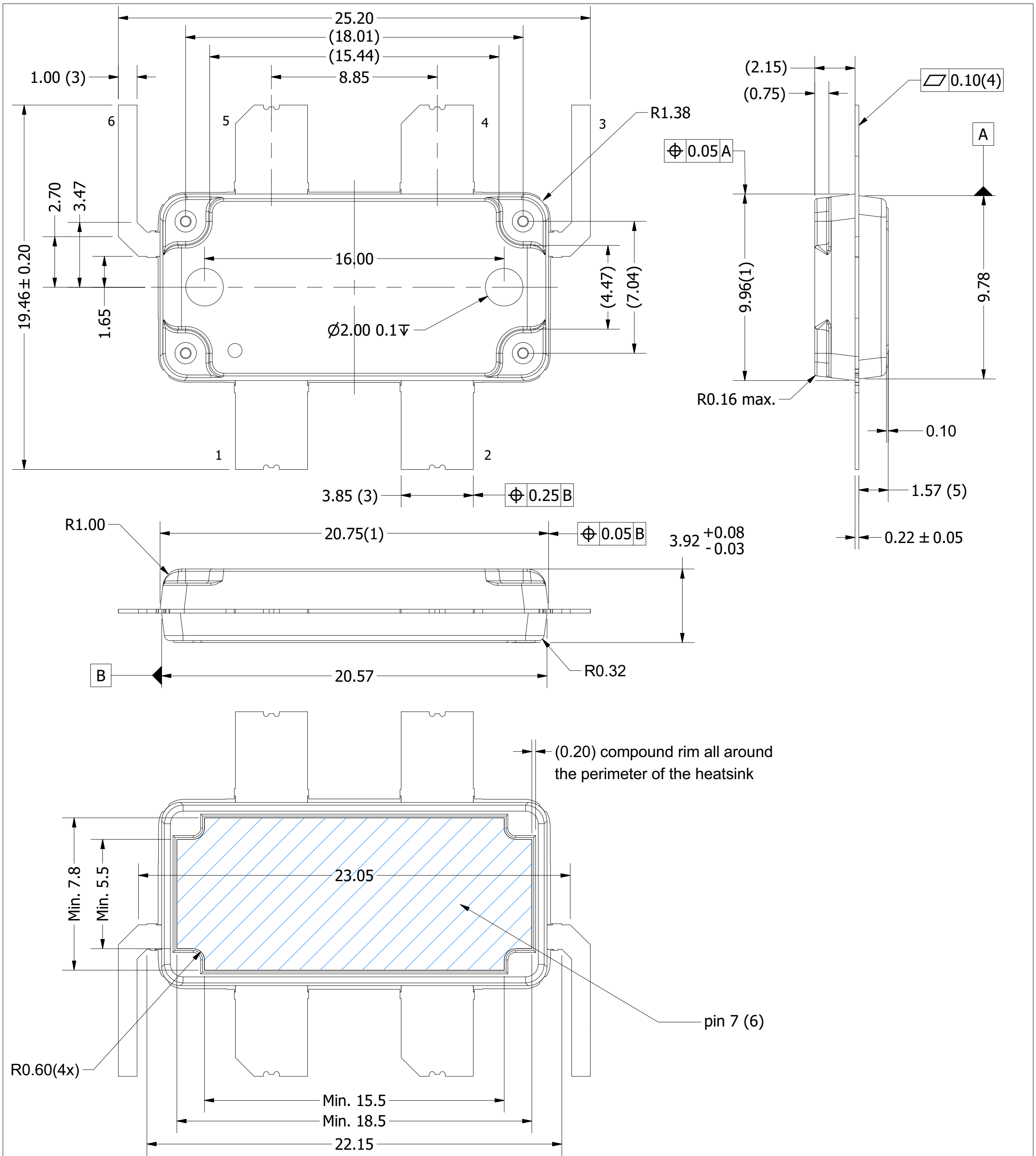
V_{DS} = 50 V; I_{Dq} = 520 mA; $V_{GS(amp)peak}$ = 0.25 V; f_c = 798 MHz; P_L = 48.8 dBm.

(1) IMD low

(2) IMD high

Fig 9. VBW capability in Doherty demo board

8. Package outline

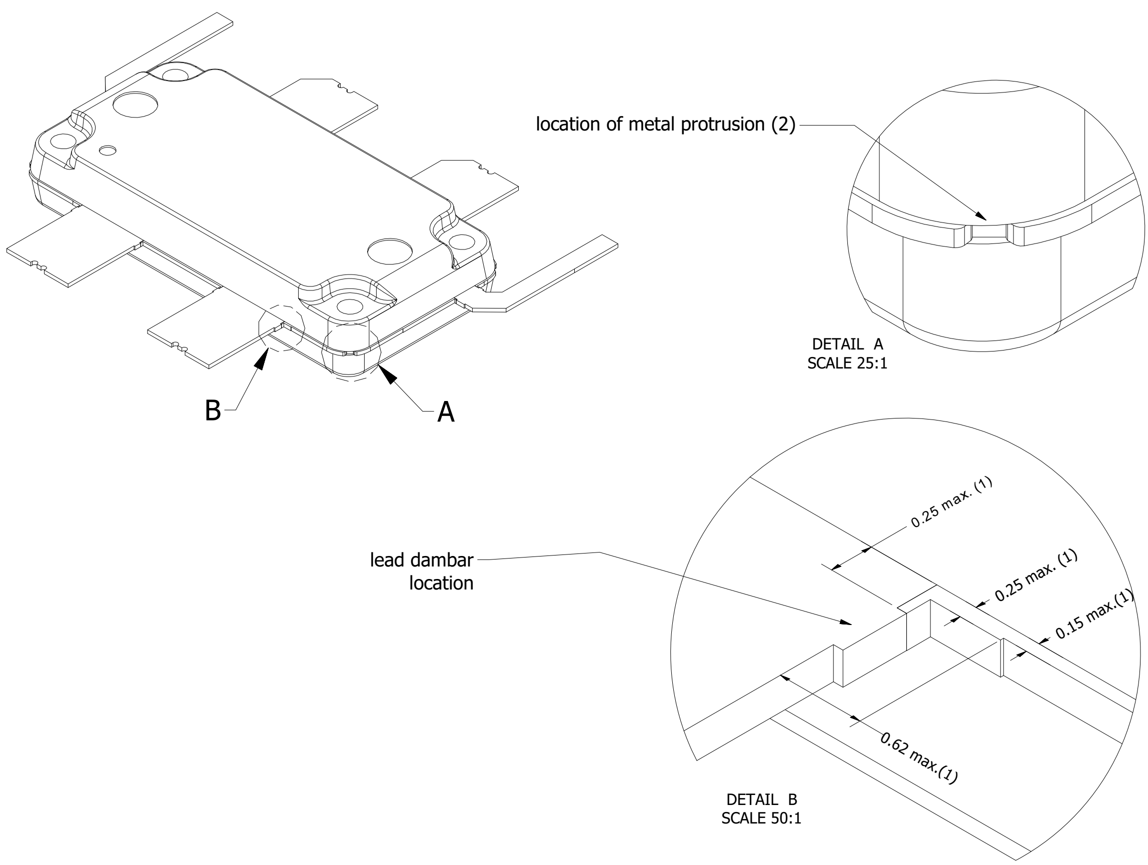


Package outline drawing: OMP-780-6F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
		Third angle projection	Sheet 1 of 2

Fig 10. Package outline OMP-780-6F-1 (sheet 1 of 2)

OMP-780-6F-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. Areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and 0.62 mm max. in length. In between the 14 leads the protrusion is 0.25 mm. max. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The lead coplanarity over all leads is 0.1 mm maximum.
(5)	Dimension is measured 0.5 mm from the edge of the top package body.
(6)	The hatched area indicates the exposed metal heatsink.
(7)	The leads and exposed heatsink are plated with matte Tin (Sn).



Package outline drawing: OMP-780-6F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
		Third angle projection	Sheet 2 of 2

Fig 11. Package outline OMP-780-6F-1 (sheet 2 of 2)

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
OBO	Output Back Off
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
PM	Phase Modulation
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP9H10S-500AWT v.2	20201218	Product data sheet	-	BLP9H10S-500AWT v.1
Modifications:	• Changed data sheet status from objective to product • Table 6 on page 3: updated table • Table 7 on page 3: updated table • Table 8 on page 4: updated table • Section 7.1 on page 4: changed I_{Dq} from 490 mA to 500 mA • Table 14 on page 8: updated table			
BLP9H10S-500AWT v.1	20200717	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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