

1. Product profile

1.1 General description

A 170 W LDMOS transistor for broadcast, avionics and non-cellular communication applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications in the frequency range from HF to 1400 MHz.

Table 1. Application information

Test signal	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)
pulsed CW	700	50	170	23.8	73

1.2 Features and benefits

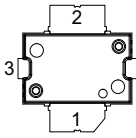
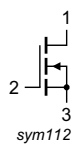
- Designed for broadband operation
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- Excellent stability
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Broadcast transmitter applications
- Avionics applications up to 1400 MHz
- Non-cellular communication applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		 sym112
2	gate		
3	source ^[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
TO-270-2F-1	BLP981Z	934961024515	TR13; 500-fold; 24 mm; dry pack	500
	BLP981XY	934961024538	TR7; 100-fold; 24 mm; dry pack	100

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	108	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature ^[1]		-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 60\text{ °C}; V_{DS} = 50\text{ V}; P_L = 170\text{ W}$	0.50	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 1.11\text{ mA}$	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 111\text{ mA}$	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50\text{ V}$; $I_D = 25\text{ mA}$	1.5	1.9	2.5	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	20	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 3.885\text{ A}$	-	0.19	-	Ω

Table 7. AC characteristics

$T_j = 25\text{ }^\circ\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	0.79	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	111	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	32.8	-	pF

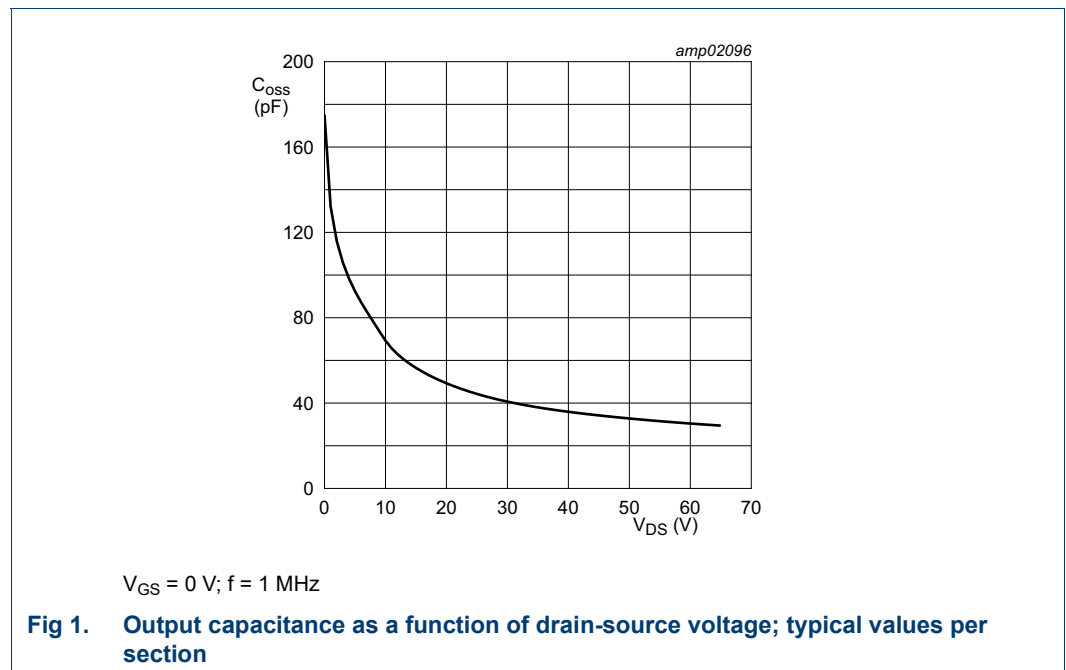


Table 8. RF characteristics

Test signal: pulsed CW; $t_p = 100 \mu s$; $\delta = 10 \%$; $f = 700 \text{ MHz}$; RF performance at $V_{DS} = 50 \text{ V}$; $I_{DQ} = 25 \text{ mA}$; $T_{case} = 25 \text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 170 \text{ W}$	22.5	23.8	-	dB
RL_{in}	input return loss	$P_L = 170 \text{ W}$	-	-12	-9	dB
η_D	drain efficiency	$P_L = 170 \text{ W}$	69	73	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLP981 is capable of withstanding a load mismatch corresponding to $VSWR = 40 : 1$ through all phases under the following conditions: $V_{DS} = 50 \text{ V}$; $I_{DQ} = 50 \text{ mA}$; $P_L = 170 \text{ W}$; $f = 700 \text{ MHz}$; pulsed CW ($t_p = 100 \mu s$; $\delta = 10 \%$).

7.2 Test circuit

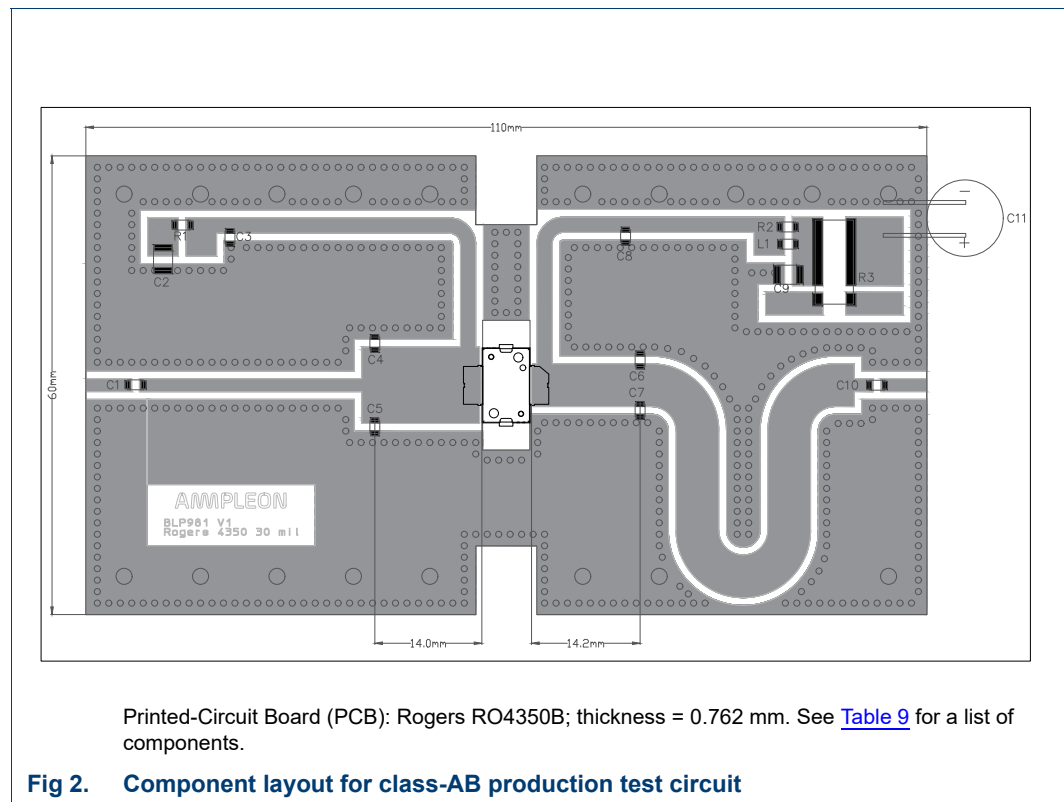


Table 9. List of components

For test circuit see [Figure 2](#)

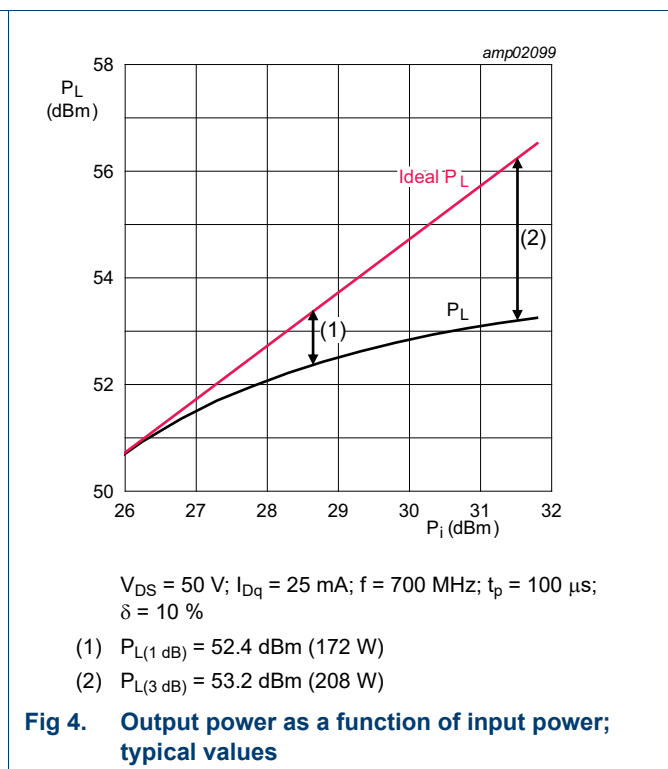
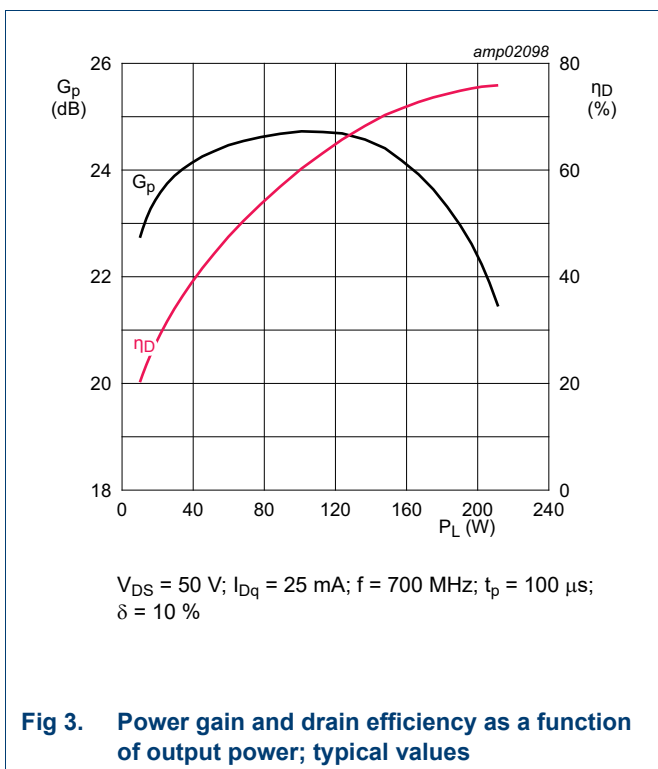
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 pF	[1] [2]
C3	multilayer ceramic chip capacitor	30 pF	[1] [2]
C4, C5	multilayer ceramic chip capacitor	22 pF	[1] [2]
C6, C7	multilayer ceramic chip capacitor	16 pF	[1] [2]
C8	multilayer ceramic chip capacitor	47 pF	[1] [2]
C10	multilayer ceramic chip capacitor	30 pF	[1] [2]
C2, C9	multilayer ceramic chip capacitor	4.7 μF	100 V
C11	electrolytic capacitor	470 μF	64 V
R1	chip resistor	9.1 Ω	SMD 1206
R2	chip resistor	4.7 Ω	SMD 1206
R3	shunt resistor	10 mΩ	
L1	inductor	9 nH	Coilcraft 1508-9N0GLB

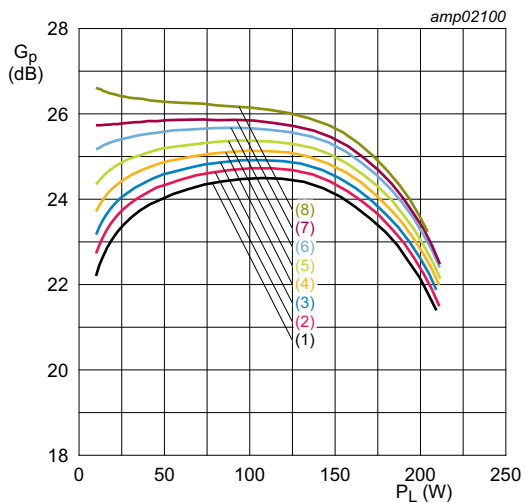
[1] American Technical Ceramics type 800A or capacitor of same quality

[2] Vertical mounted

7.3 Graphical data

7.3.1 Pulsed CW performance measured in production RF test circuit

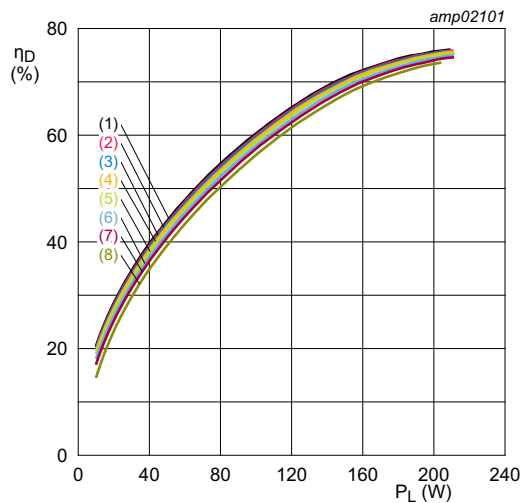




$V_{DS} = 50\text{ V}; f = 700\text{ MHz}; t_p = 100\ \mu\text{s}; \delta = 10\%$

- (1) $I_{Dq} = 10\text{ mA}$
- (2) $I_{Dq} = 25\text{ mA}$
- (3) $I_{Dq} = 50\text{ mA}$
- (4) $I_{Dq} = 100\text{ mA}$
- (5) $I_{Dq} = 200\text{ mA}$
- (6) $I_{Dq} = 400\text{ mA}$
- (7) $I_{Dq} = 600\text{ mA}$
- (8) $I_{Dq} = 1000\text{ mA}$

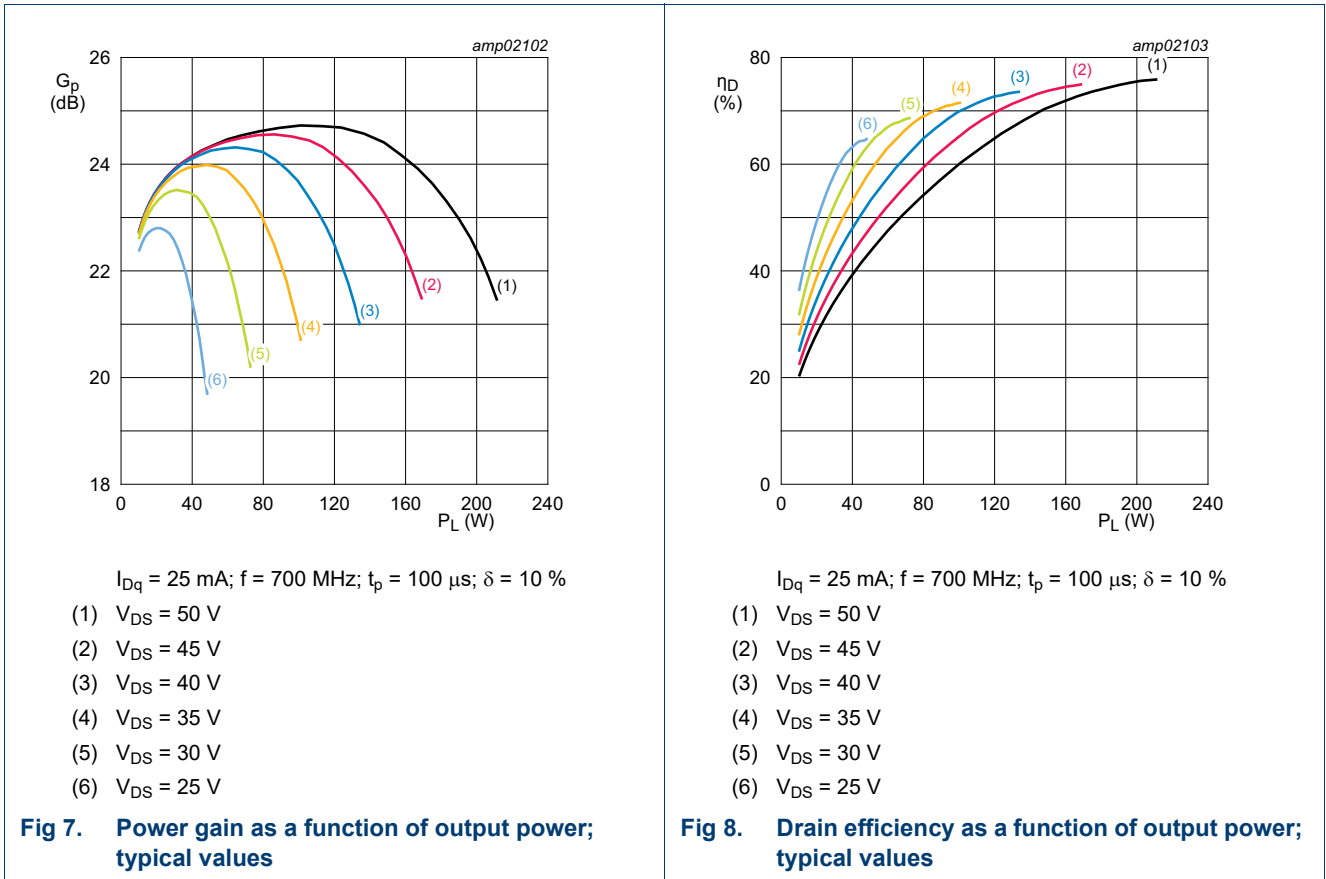
Fig 5. Power gain as a function of output power; typical values



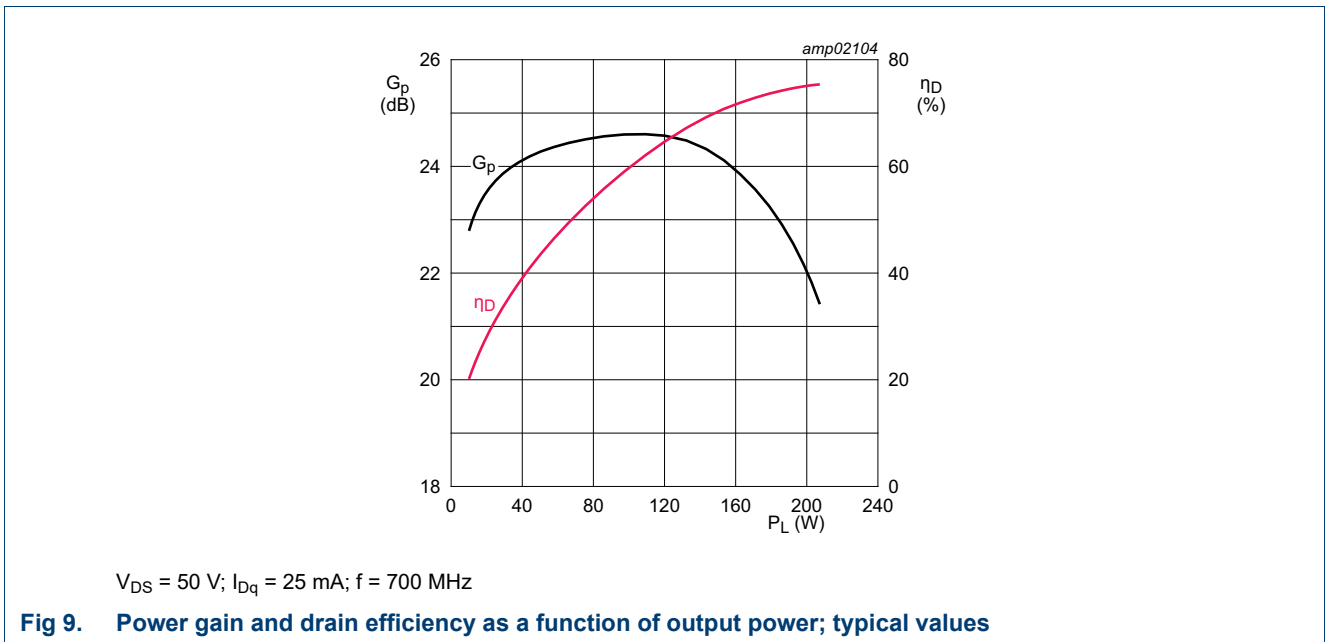
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- (6) $I_{Dq} = 400\text{ mA}$
- (7) $I_{Dq} = 600\text{ mA}$
- (8) $I_{Dq} = 1000\text{ mA}$

Fig 6. Drain efficiency as a function of output power; typical values



7.3.2 CW performance measured in production RF test circuit



8. Package outline

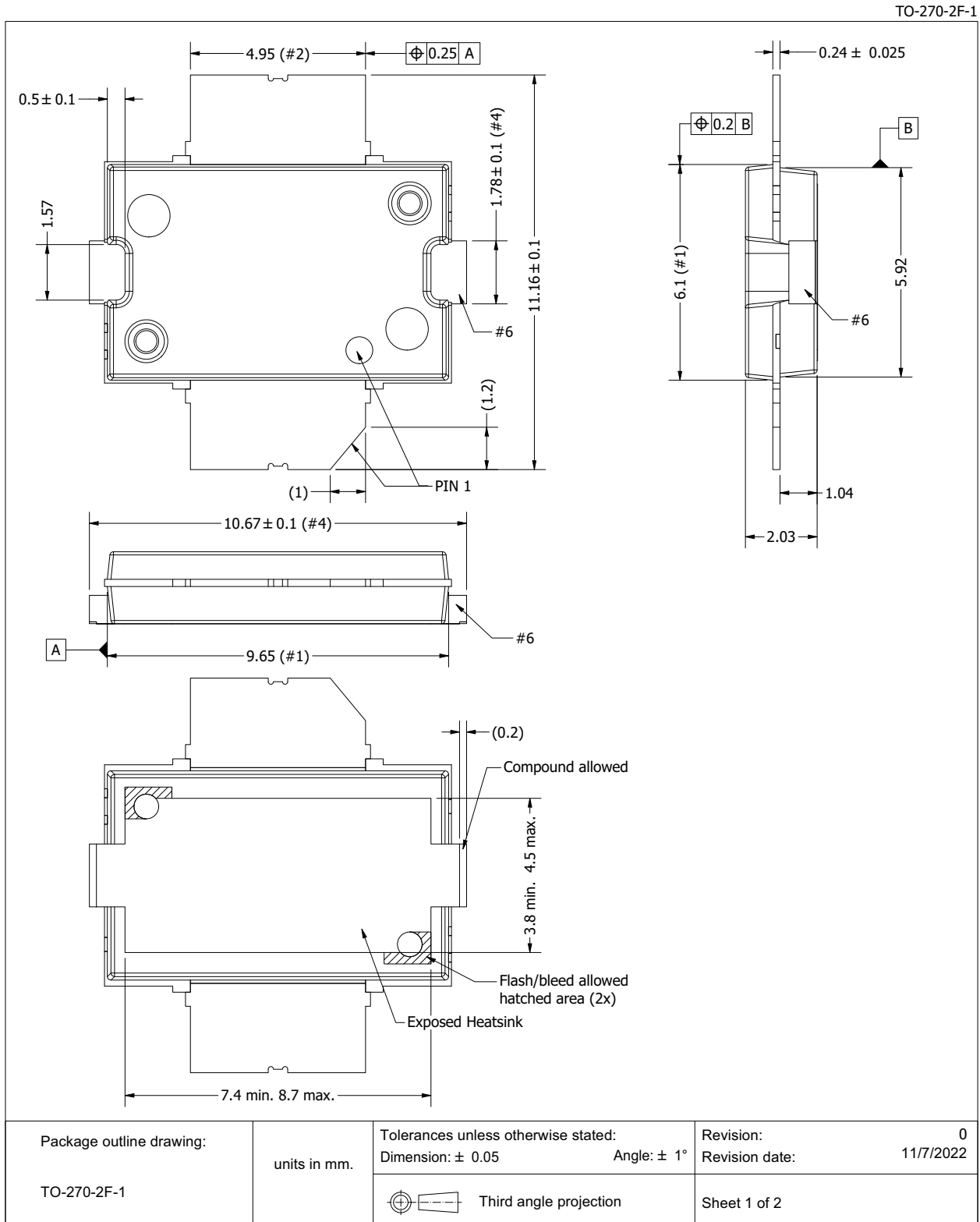


Fig 10. Package outline TO-270-2F-1 (sheet 1 of 2)

TO-270-2F-1

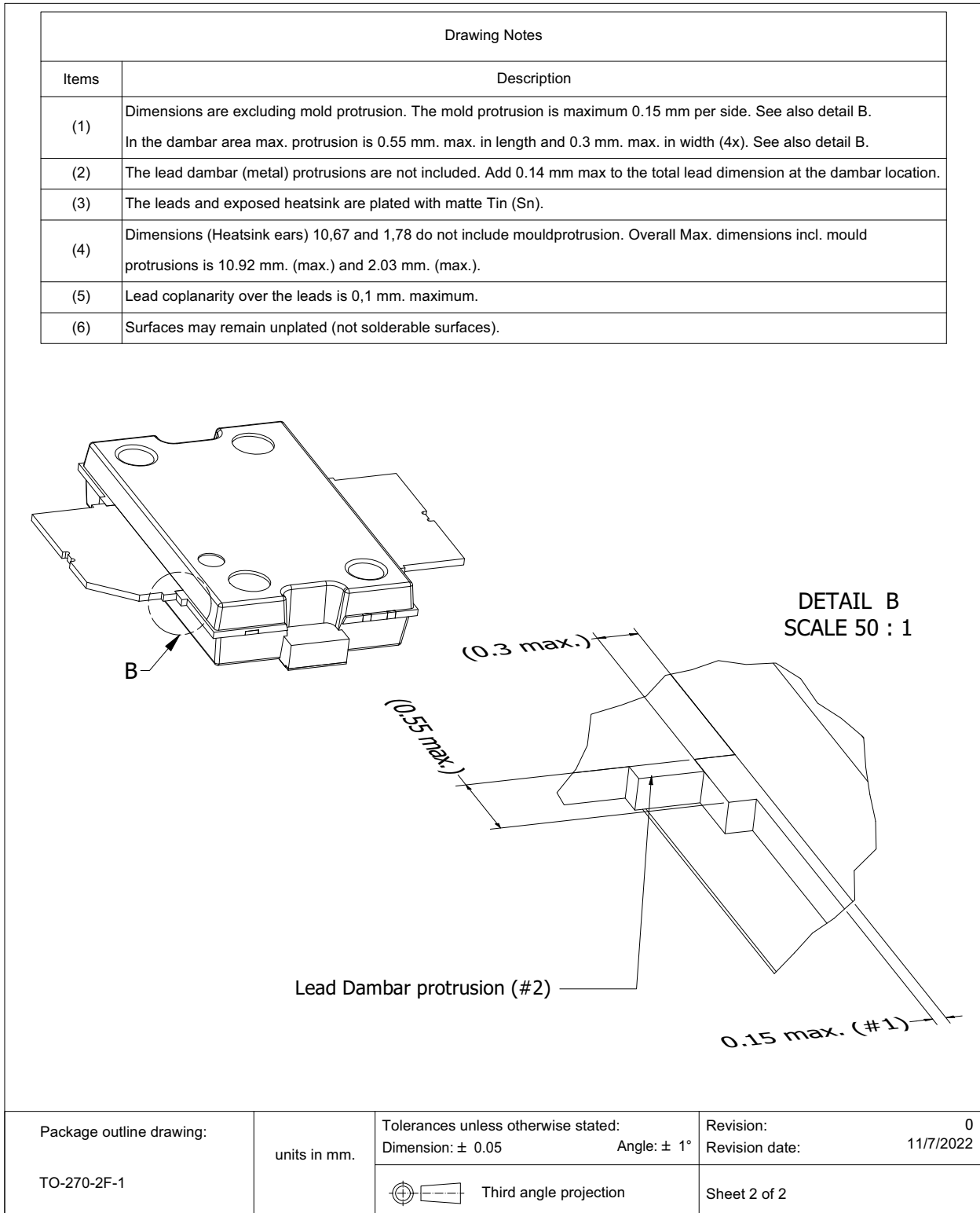


Fig 11. Package outline TO-270-2F-1 (sheet 2 of 2)

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP981 v1	20241216	Production data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contact information

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Date of release: 16 December 2024
 Document identifier: BLP981