BLM9D1822S-60PBG

LDMOS 2-stage integrated Doherty MMIC

AMPLEON

Rev. 3 — 16 April 2021 **Product data sheet**

1. Product profile

1.1 General description

The BLM9D1822S-60PBG is a dual section, 2-stage fully integrated Doherty MMIC solution using Ampleon's state of the art GEN9 LDMOS technology. For each section, the carrier and peaking device, input splitter and output combiner are integrated in a single package. This multiband device is perfectly suited as general purpose driver or small cell final in the frequency range from 1800 MHz to 2200 MHz. Available in gull wing outline.

Table 1. Performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 222 mA (carrier and peaking); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.9$ V. Test signal: 1-carrier LTE 20 MHz; measured in an Ampleon f = 1960 MHz combined integrated Doherty application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{20M}$
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier LTE 20 MHz	1960	28	3.16	28.7	22.8	–44.1

1.2 Features and benefits

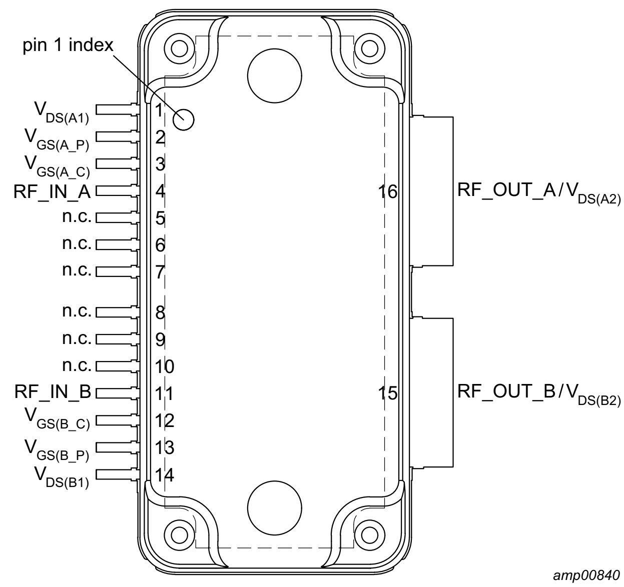
- Integrated input splitter
- Integrated output combiner
- High efficiency
- Designed for broadband operation (frequency 1800 MHz to 2200 MHz)
- High section-to-section isolation enabling multiple combinations
- Independent control of carrier and peaking bias
- Integrated ESD protection
- Excellent thermal stability
- Source impedance 50 Ω; high power gain
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power MMIC for multi-carrier and multi-standard GSM, W-CDMA and LTE base stations in the 1800 MHz to 2200 MHz frequency range. Possible circuit topologies are the following as also depicted in Section 8.1:
  - Dual section or single ended
  - Quadrature combined
  - Push-pull

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of driver stage of section A
$V_{GS(A\_P)}$	2	gate-source voltage of peaking of section A
$V_{GS(A\_C)}$	3	gate-source voltage of carrier of section A
RF_IN_A	4	RF input section A
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
RF_IN_B	11	RF input section B
$V_{GS(B\_C)}$	12	gate-source voltage of carrier of section B
$V_{GS(B\_P)}$	13	gate-source voltage of peaking of section B
$V_{DS(B1)}$	14	drain-source voltage of driver stages of section B

Table 2. Pin description *...continued*

Symbol	Pin	Description
RF_OUT_B/$V_{DS(B2)}$	15	RF output section B / drain-source voltage of final stages of section B
RF_OUT_A/$V_{DS(A2)}$	16	RF output section A / drain-source voltage of final stages of section A
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM9D1822S-60PBG		plastic, heatsink small outline package; 16 leads	OMP-780-16G-1

4. Block diagram

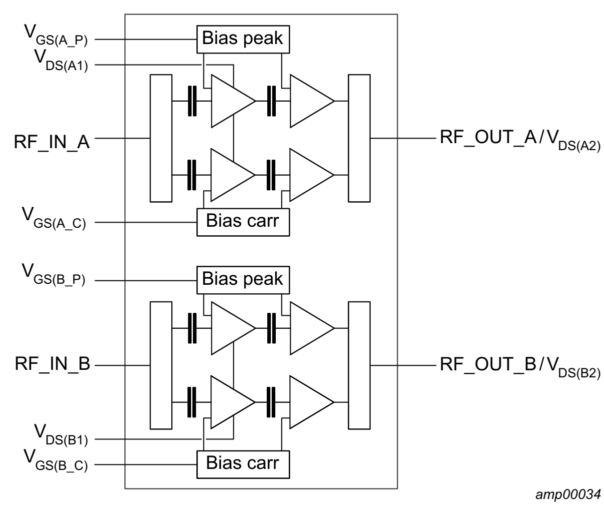


Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics
Measured for total device.

Symbol	Parameter	Conditions		Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; P_L = 3 W	[1]	2.8	K/W
		T_{case} = 90 °C; P_L = 6 W	[1]	2.6	K/W

[1] When operated with an 1-carrier W-CDMA with PAR = 9.9 dB.

7. Characteristics

Table 6. DC characteristics
T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 105 mA	1.7	2.1	2.5	V
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Peaking						
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA

Table 7. RF Characteristics
Typical RF performance at T_{case} = 25 °C; per section unless otherwise specified; V_{DS} = 28 V; I_{Dq} = 105 mA; $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.4$ V; $P_{L(AV)}$ = 2.51 W (34 dBm); f = 2200 MHz, measured in an Ampleon production circuit. Test signal: pulsed CW; t_p = 0.1 ms; δ = 10 %;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	f = 2200 MHz	26.3	28.3	-	dB
η_D	drain efficiency	P_L = 2.51 W (34 dBm)	23	25.5	-	%
		$P_L = P_{L(3dB)}$	50	53	-	%
RL_{in}	input return loss		-	-	−10	dB
$P_{L(3dB)}$	output power at 3 dB gain compression		44.9	45.4	-	dBm

8. Application information

Table 8. Typical performance
T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 222 mA (driver and final stages). Test signal: 1-carrier LTE 20 MHz; PAR = 7.2 dB; measured in an Ampleon 1800 MHz to 2200 MHz frequency band symmetrical integrated Doherty application circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	f = 1960 MHz	[1]	-	47.7	-	dBm
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 1960 MHz	[1]	-	48.7	-	dBm
$\varphi_{s21}/\varphi_{s21(norm)}$	normalized phase response	f = 1960 MHz at 3 dB compression point	[2]	-	-8.7	-	°

Table 8. Typical performance *...continued*

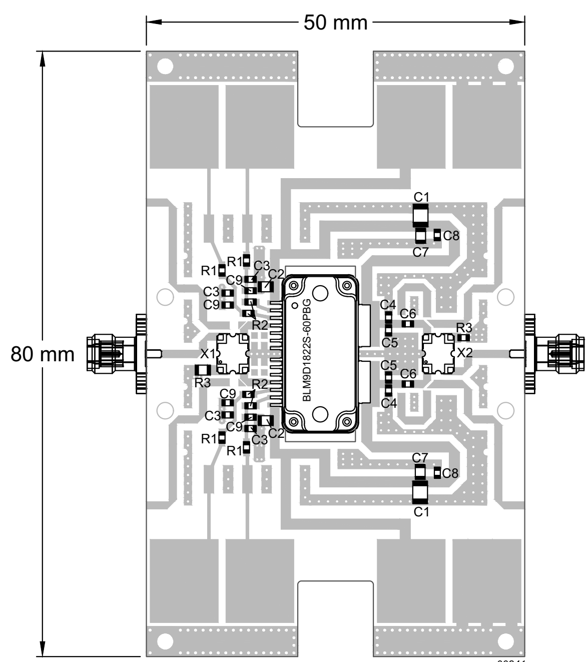
T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 222 mA (driver and final stages). Test signal: 1-carrier LTE 20 MHz; PAR = 7.2 dB; measured in an Ampleon 1800 MHz to 2200 MHz frequency band symmetrical integrated Doherty application circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
η_D	drain efficiency	13.7 dB OBO ($P_{L(AV)}$ = 35 dBm); f = 1960 MHz	-	22.8	-	%
G_p	power gain	$P_{L(AV)}$ = 35 dBm; f = 1960 MHz	-	28.7	-	dB
B_{video}	video bandwidth	$P_{L(AV)}$ = 35 dBm set to obtain IMD3 = –40 dBc; 2-tone CW; f = 1960 MHz	-	151	-	MHz
G_{flat}	gain flatness	$P_{L(AV)}$ = 35 dBm; f = 1800 MHz to 2200 MHz	-	1.1	-	dB
$ACPR_{20M}$	adjacent channel power ratio (20 MHz)	$P_{L(AV)}$ = 35 dBm; f = 1960 MHz	-	–44.1	-	dBc
$\Delta G/\Delta T$	gain variation with temperature	f = 1960 MHz [3]		0.045	-	dB/°C
K	Rollett stability factor	T_{case} = –40 °C; f = 0.2 GHz to 5 GHz [3]	-	>4	-	

[1] Pulsed CW power sweep measurement (δ = 10 %; t_p = 100 μs).

[2] 25 ms CW power sweep measurement.

[3] S-parameters measured with broadband demo board.



Printed-Circuit Board (PCB): RO4350; thickness = 0.508 mm.

Fig 3. Component layout

Table 9. List of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: SMD 1206
C2	multilayer ceramic chip capacitor	10 μF, 35 V	TDK: SMD 0805
C3	multilayer ceramic chip capacitor	10 μF, 6.3 V	Murata: SMD 0603
C4, C5	multilayer ceramic chip capacitor	0.8 pF	Murata: SMD 0603
C6	multilayer ceramic chip capacitor	7.5 pF	Murata: SMD 0603
C7	multilayer ceramic chip capacitor	1 nF	Murata: SMD 0805
C8	multilayer ceramic chip capacitor	18 pF	Murata: SMD 0603
C9	multilayer ceramic chip capacitor	22 pF	Murata: SMD 0603
R1	resistor	1 kΩ	Multicomp: SMD 0603
R2	resistor	5.1 Ω	Multicomp: SMD 0603
R3	resistor	50 Ω	Multicomp: SMD 0805
X1, X2	hybrid coupler	3 dB, 90°	Anaren: X3C25F1-03S

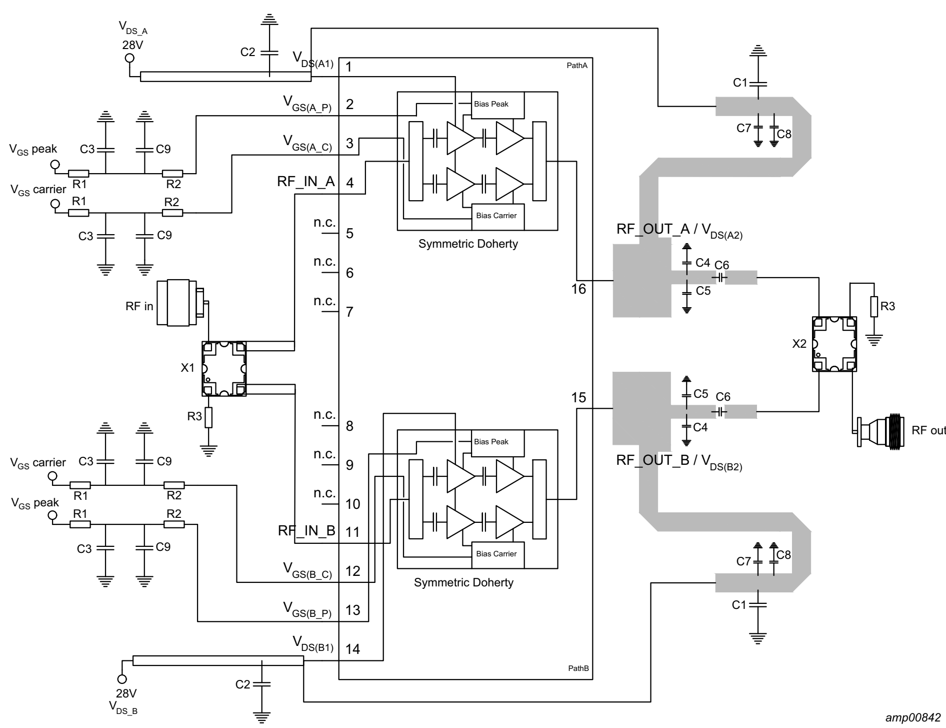


Fig 4. Electrical schematic

8.1 Possible circuit topologies

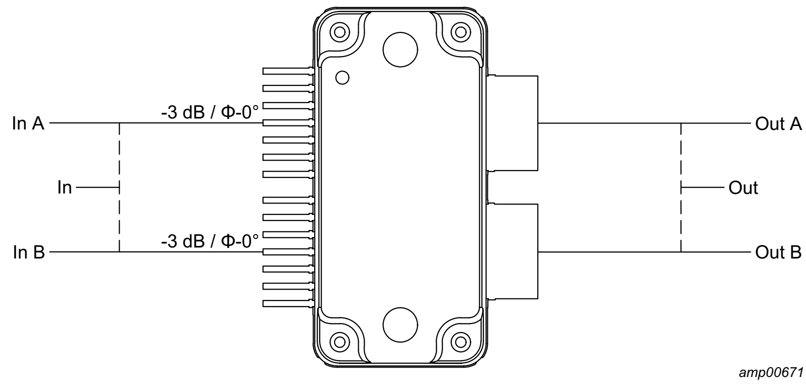


Fig 5. Dual section or single ended

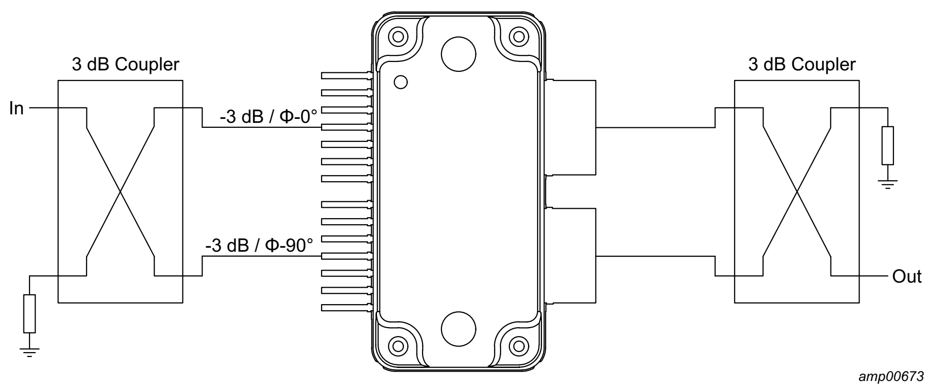


Fig 6. Quadrature combined

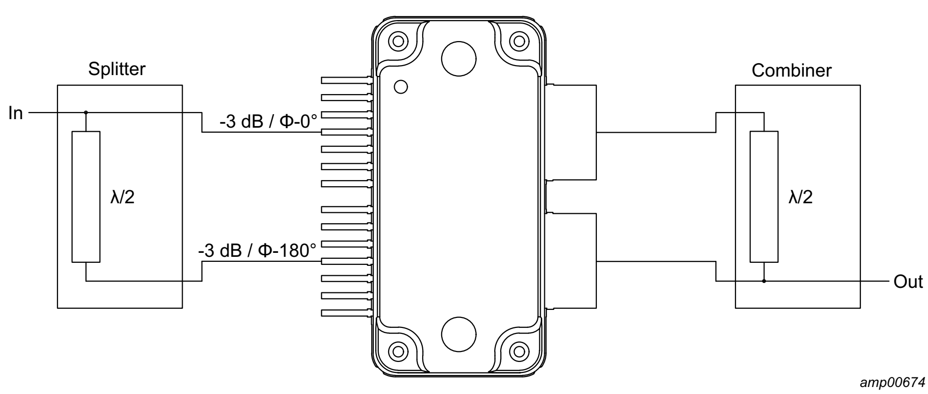


Fig 7. Push-pull

8.2 Ruggedness in a Doherty operation

The BLM9D1822S-60PBG is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 105 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.4$ V; P_i corresponding to $P_{L(3dB)}$ – 5 dB under Z_S = 50 Ω load; f = 2000 MHz (1-carrier W-CDMA; PAR = 9.9 dB); T_{case} = 25 °C per section unless otherwise specified.

8.3 Impedance information

Table 10. Typical impedance for optimum Doherty operation

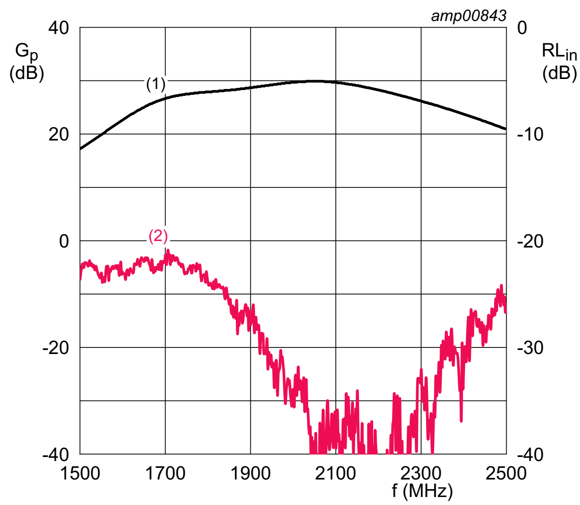
Measured load-pull data per section; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 105 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.4$ V; t_p = 100 μs; δ = 10 %. Typical values per section unless otherwise specified.

f	tuned for optimum Doherty operation				
	Z_L	$G_{p(max)}$	P_L	η_{add} [1]	η_{add} [2]
(MHz)	(Ω)	(dB)	(dBm)	(%)	(%)
1700	8.53 – j16.09	29.56	45.34	43.93	25.22
1800	11.78 – j16.68	29.24	45.45	46.98	25.25
1900	11.45 – j14.97	29.50	46.09	53.43	27.04
2000	13.24 – j14.44	30.24	46.09	56.24	27.04
2100	14.42 – j13.36	31.61	45.93	57.23	27.07
2200	19.19 – j12.70	30.90	45.69	54.20	28.75

[1] At $P_{L(3dB)}$.

[2] at 34 dBm.

8.4 Graphs



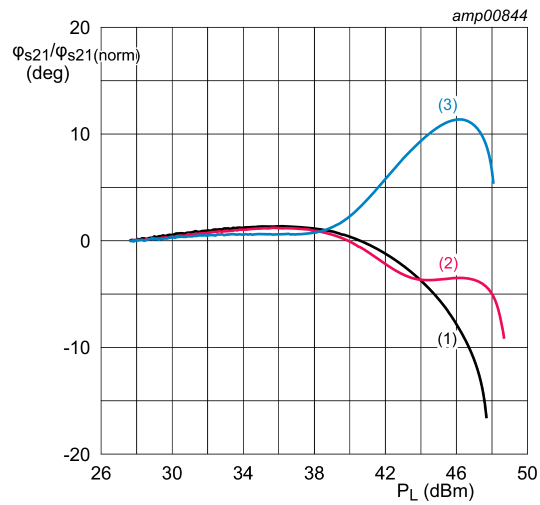
T_{case} = 25 °C; V_{DS} = 28 V;
I_{Dq1} + I_{Dq2} = 222 mA (carrier and peaking stages);
V_{GS} = 2.6 V (carrier stage);
V_{GS} = 1.7 V (peaking stage).

Test signal: CW.

(1) magnitude of G_p

(2) magnitude of RL_{in}

Fig 8. Wideband power gain and input return loss as function of frequency; typical values



T_{case} = 25 °C; V_{DS} = 28 V;
I_{Dq1} + I_{Dq2} = 222 mA (carrier and peaking stages);
V_{GS} = 2.6 V (carrier stage);
V_{GS} = 1.7 V (peaking stage).

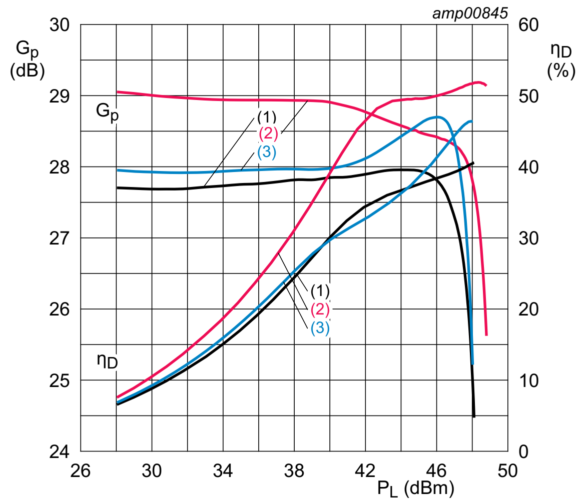
Test signal: 25 ms CW power sweep.

(1) f = 1800 MHz

(2) f = 1960 MHz

(3) f = 2200 MHz

Fig 9. Normalized phase response as a function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} + I_{Dq2} = 222 mA (carrier and peaking stages); V_{GS} = 2.6 V (carrier stage); V_{GS} = 1.7 V (peaking stage).

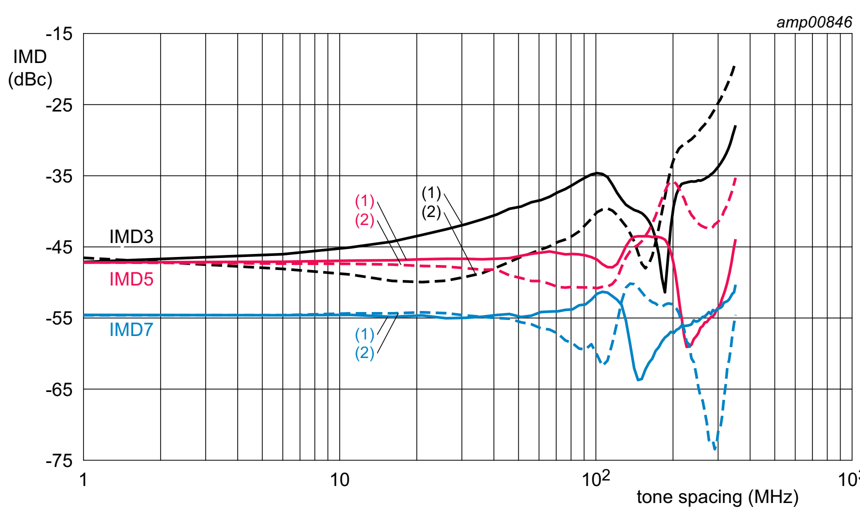
Test signal: pulsed CW power sweep; δ = 10 %; t_p = 100 μs.

(1) f = 1800 MHz

(2) f = 1960 MHz

(3) f = 2200 MHz

Fig 10. Power gain and drain efficiency as function of output power; typical values



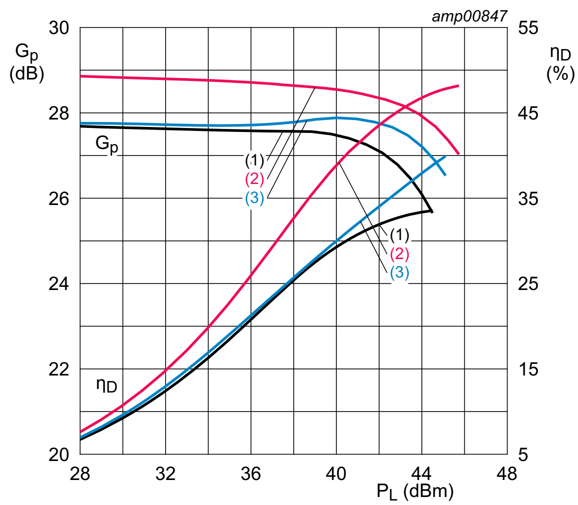
T_{case} = 25 °C; V_{DS} = 28 V; $P_{L(AV)}$ = 3.16 W; I_{Dq1} + I_{Dq2} = 222 mA (carrier and peaking stages); V_{GS} = 2.6 V (carrier stage); V_{GS} = 1.7 V (peaking stage).

Test signal: 2-tone CW; f_c = 1960 MHz.

(1) IMD low

(2) IMD high

Fig 11. Intermodulation distortion as a function of tone spacing; typical values



T_{case} = 25 °C; V_{DS} = 28 V;
$I_{Dq1} + I_{Dq2}$ = 222 mA (carrier and peaking stages);
V_{GS} = 2.6 V (carrier stage);
V_{GS} = 1.7 V (peaking stage).

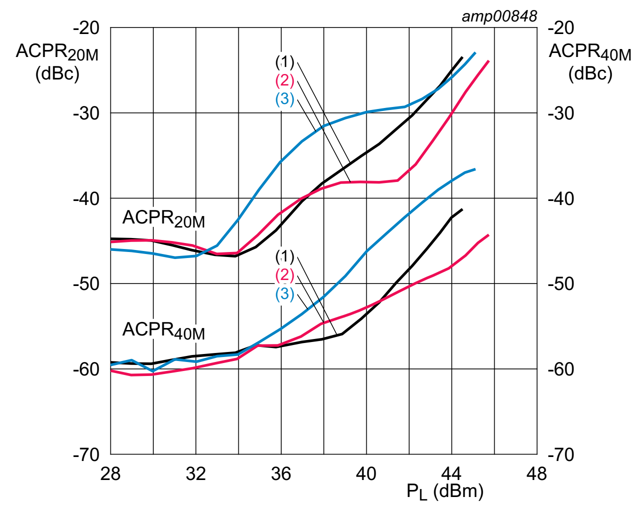
Test signal: 1-carrier LTE; PAR = 7.2 dB at 0.01 % probability CCDF.

(1) f = 1800 MHz

(2) f = 1960 MHz

(3) f = 2200 MHz

Fig 12. Power gain and drain efficiency as function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V;
$I_{Dq1} + I_{Dq2}$ = 222 mA (carrier and peaking stages);
V_{GS} = 2.6 V (carrier stage);
V_{GS} = 1.7 V (peaking stage).

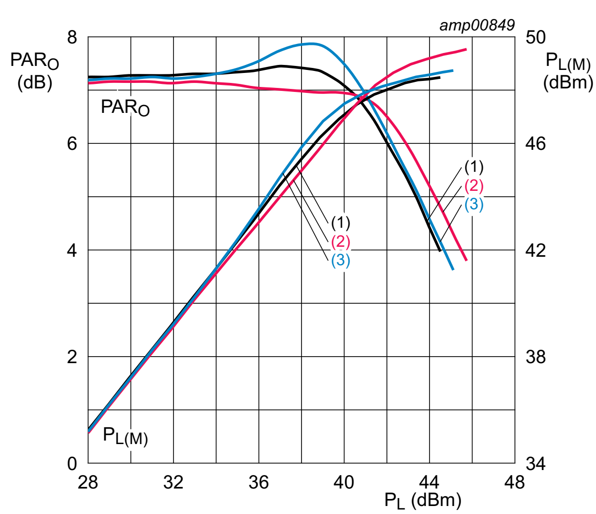
Test signal: 1-carrier LTE; PAR = 7.2 dB at 0.01 % probability CCDF.

(1) f = 1800 MHz

(2) f = 1960 MHz

(3) f = 2200 MHz

Fig 13. Adjacent channel power ratio as a function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V; $I_{Dq1} + I_{Dq2}$ = 222 mA (carrier and peaking stages);
V_{GS} = 2.6 V (carrier stage); V_{GS} = 1.7 V (peaking stage).

Test signal: 1-carrier LTE; PAR = 7.2 dB at 0.01 % probability CCDF.

(1) f = 1800 MHz

(2) f = 1960 MHz

(3) f = 2200 MHz

Fig 14. Output peak-to-average ratio and peak output power as function of output power; typical values

9. Package outline

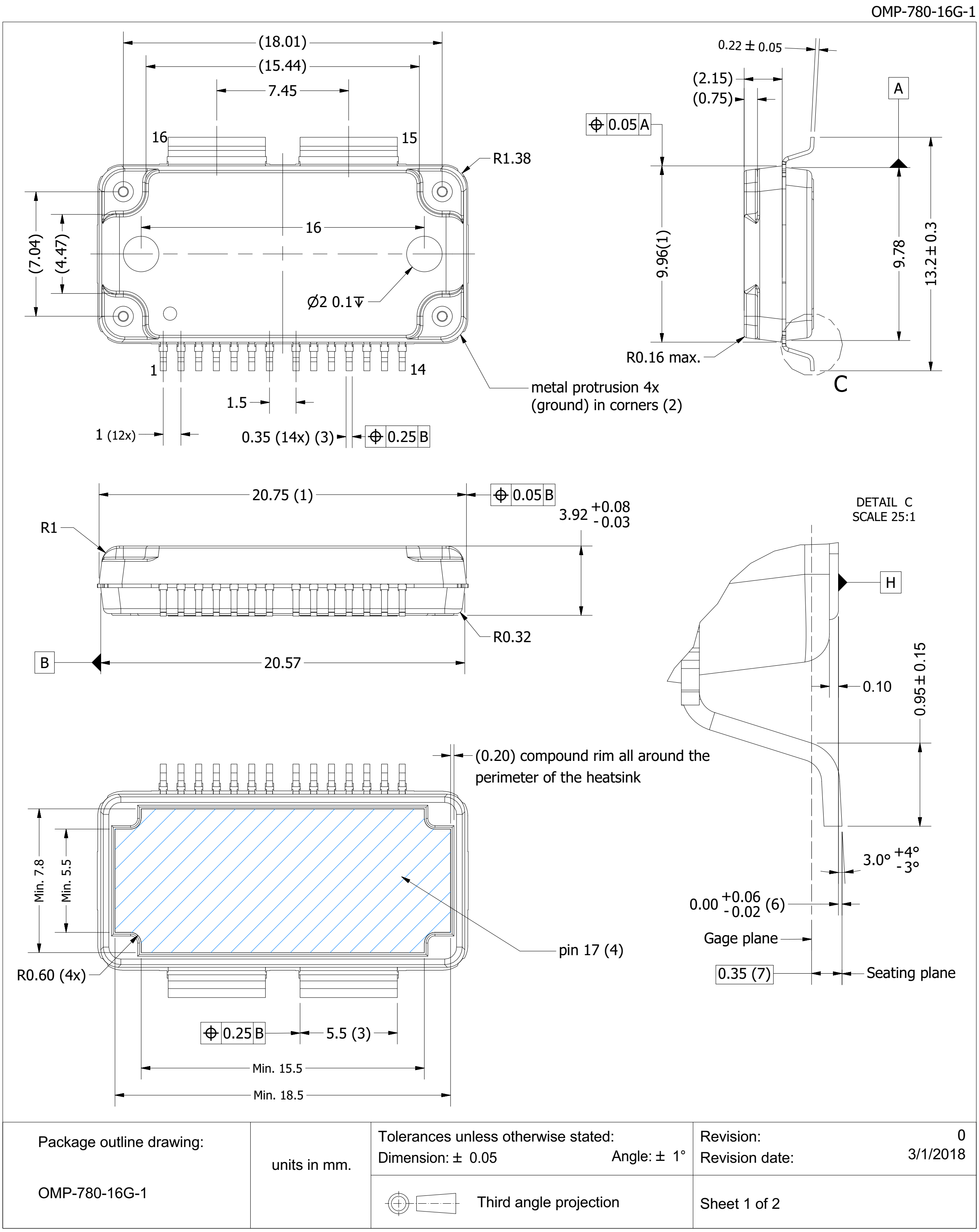
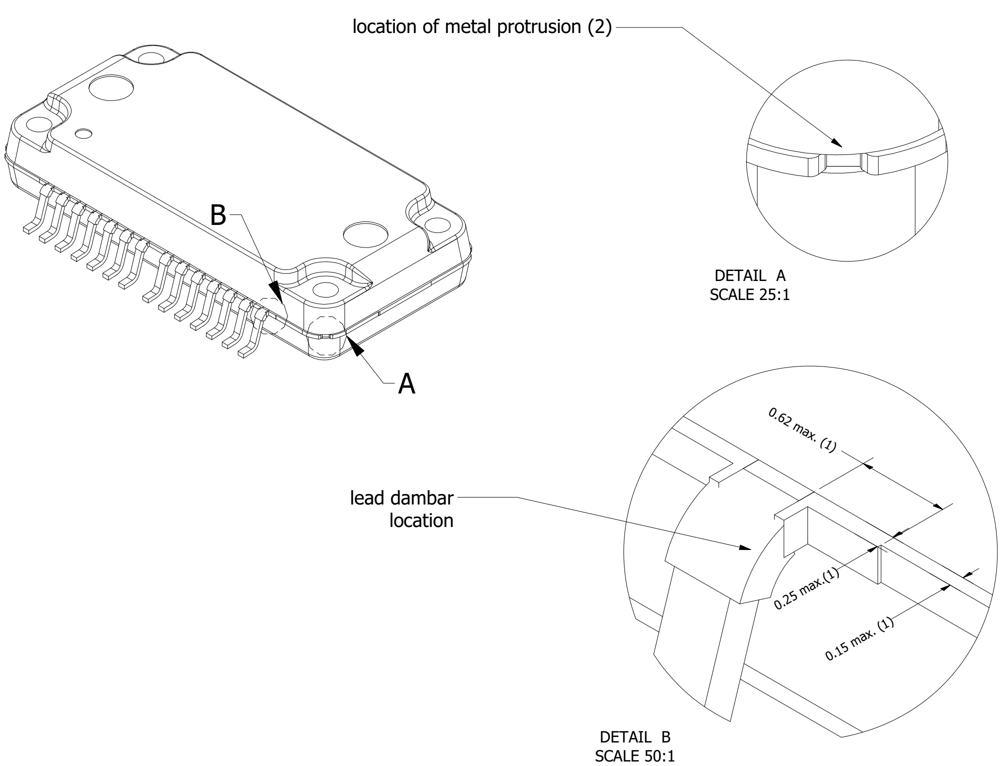


Fig 15. Package outline OMP-780-16G-1 (sheet 1 of 2)

OMP-780-16G-1

Drawing Notes

Items	Description
(1)	Dimensions are excluding mold protrusion. Areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and 0.62 mm max. in length. In between the 14 leads the protrusion is 0.25 mm max. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The hatched area indicated the exposed heatsink.
(5)	The leads and exposed heatsink are plated with matte Tin (Sn).
(6)	Dimension is measured with respect to the bottom of the heatsink Datum H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead.
(7)	Gage plane (foot length) to be measured from the seating plane.



Package outline drawing: OMP-780-16G-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
		Third angle projection	Sheet 2 of 2

Fig 16. Package outline OMP-780-16G-1 (sheet 2 of 2)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
ESD	ElectroStatic Discharge
GEN9	Ninth Generation
GSM	Global System for Mobile Communication
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM9D1822S-60PBG v.3	20210416	Product data sheet	-	BLM9D1822S-60PBG v.2
Modifications	• Section 8.2 on page 8: text updated			
BLM9D1822S-60PBG v.2	20190419	Product data sheet	-	BLM9D1822S-60PBG v.1
BLM9D1822S-60PBG v.1	20181220	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

13.2 Definitions

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14. Contact information

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