BLC10G16XS-600AVT

Power LDMOS transistor

AMPLEON

Rev. 1 — 16 December 2021 **Product data sheet**

1. Product profile

1.1 General description

600 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1427 MHz to 1518 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 32 V; I_{Dq} = 1450 mA (main); $V_{GS(amp)peak}$ = 1.1 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W/dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1427 to 1518	32	115/50.6	18.0	49.7	–31.0 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.7 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

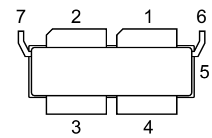
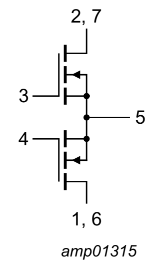
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1427 MHz to 1518 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain (peak)		
2	drain (main)		
3	gate (main)		
4	gate (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G16XS-600AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 30 V; I_{Dq} = 1300 mA (main); $V_{GS(amp)peak}$ = 1.3 V; T_{case} = 80 °C		
		P_L = 115 W	0.19	K/W
		P_L = 145 W	0.17	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.08 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 208 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 1300 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 2.37 V	-	39	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.3 A	-	20	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 2.37 V; I_D = 7.3 A	-	60	111	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 380 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 1900 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 2.37 V	-	63	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 13.3 A	-	37	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 2.37 V; I_D = 13.3 A	-	34	65.3	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 1429.5 MHz; f_2 = 1515.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 1300 mA (main); $V_{GS(amp)peak}$ = 1.27 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit [1] at frequencies from 1427 MHz to 1518 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 112 W	16.2	17.4	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 112 W	-	–16	–9	dB
η_D	drain efficiency	$P_{L(AV)}$ = 112 W	44	48.7	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 112 W	-	–30	–26	dBc

[1] The industrial test method is performed on special hardware to accommodate the requirements of production. The test results in this table are correlated to correspond with a performance in the application.

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 1429.5 MHz; f_2 = 1515.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 1300 mA (main); $V_{GS(amp)peak}$ = 1.27 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit [1] at frequencies from 1427 MHz to 1518 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 161 W	5.9	6.5	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 161 W	614	720	-	W

[1] The industrial test method is performed on special hardware to accommodate the requirements of production. The test results in this table are correlated to correspond with a performance in the application.

7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G16XS-600AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 1300 mA; $V_{GS(amp)peak}$ = 1.38 V; f = 1400 MHz; P_L = 270 W (5.0 dB OBO); 100 % clipping.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 1040 mA (main); V_{DS} = 32 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1410	1.5 – j5.5	1.3 – j3.2	350	57.6	17.2
1480	2.6 – j6.9	1.3 – j3.2	347	57.1	17.4
1526	4.4 – j8.3	1.2 – j3.2	340	55.7	17.6
Maximum drain efficiency load					
1410	1.6 – j5.6	2.3 – j3.6	276	64.8	18.7
1480	2.7 – j7.0	2.6 – j3.0	260	65.5	19.3
1526	4.8 – j8.4	2.5 – j2.6	252	65.7	19.7

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1900 mA (peak); V_{DS} = 32 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1410	1.3 – j5.4	2.0 – j3.0	586	57.4	16.9
1480	2.4 – j6.8	1.9 – j2.8	575	57.6	17.4
1526	4.4 – j8.2	1.8 – j2.8	586	58.9	17.5

Table 10. Typical impedance of peak device *...continued*

Measured load-pull data of peak device; I_{Dq} = 1900 mA (peak); V_{DS} = 32 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum drain efficiency load					
1410	1.3 – j5.4	3.3 – j2.6	494	62.8	18.0
1480	2.5 – j6.8	2.9 – j1.6	448	63.9	18.9
1526	4.4 – j8.3	2.3 – j1.7	469	65.7	18.9

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

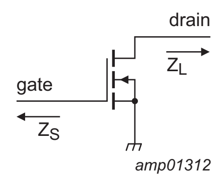


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main device at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 1040 mA (main); V_{DS} = 32 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1410	1.6 – j5.3	1.7 – j3.9	294	41.8	20.5
1480	2.6 – j6.8	1.6 – j3.2	333	39.5	20.9
1526	4.2 – j8.3	1.6 – j2.7	319	40.2	21.6

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 112 W.

Table 12. Typical impedance of main device at 1 : 2.8 load

Measured load-pull data of main device; I_{Dq} = 1040 mA (main); V_{DS} = 32 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1410	1.5 – j5.3	4.6 – j3.7	158	59.5	22.7
1480	2.6 – j6.8	4.5 – j3.2	164	58.8	22.6
1526	4.2 – j8.3	4.4 – j2.9	160	57.5	22.6

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 112 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; I_{Dq} = 1900 mA (peak); V_{DS} = 32 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1410	1.3 – j5.4	2.3 – j2.9	497	28.9	20.3
1480	2.3 – j6.8	2.2 – j2.5	568	31.0	20.7
1526	3.9 – j8.3	2.1 – j2.2	537	32.4	21.3

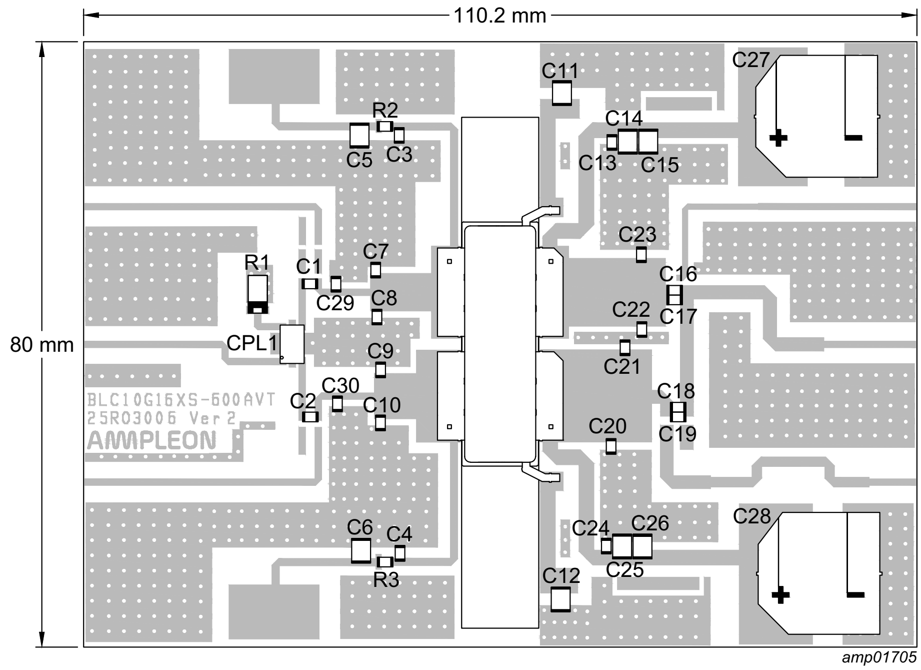
[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 112 W.

Table 14. Off-state impedances of peak device

f	Z_{off}
(MHz)	(Ω)
1410	1.0 – j4.9
1480	0.4 – j2.0
1526	0.3 – j1.2

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers RO3006; ε_r = 6.15; thickness = 0.635 mm; thickness copper plating = 35 μm.

See Table 15 for a list of components.

Fig 2. Component layout

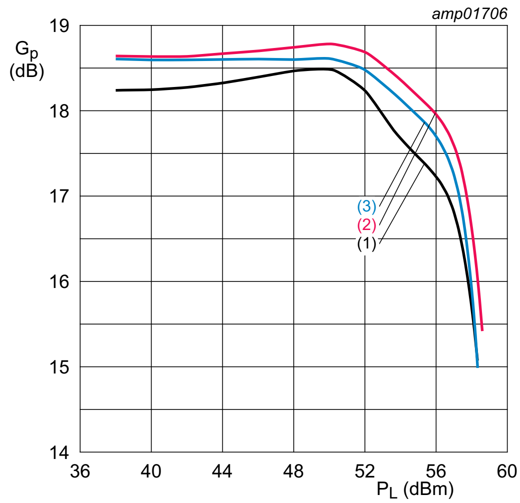
Table 15. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C2, C3, C4, C13, C24	multilayer ceramic chip capacitor	15 pF	Murata: HiQ, GQM21 series, 0805
C5, C6, C11, C12, C14, C15, C25, C26,	multilayer ceramic chip capacitor	10 μF, 100 V	Murata: SMD 1210
C7, C8	multilayer ceramic chip capacitor	1.7 pF	ATC 100A
C9, C10	multilayer ceramic chip capacitor	1.8 pF	ATC 100A
C16, C17, C18, C19	multilayer ceramic chip capacitor	6.8 pF	ATC 100A
C20	multilayer ceramic chip capacitor	1.6 pF	Murata: HiQ, GQM21 series, 0805
C21	multilayer ceramic chip capacitor	1.0 pF	Murata: HiQ, GQM21 series, 0805
C22	multilayer ceramic chip capacitor	0.6 pF	Murata: HiQ, GQM21 series, 0805
C23	multilayer ceramic chip capacitor	0.4 pF	ATC 100A
C27, C28	electrolytic capacitor	470 μF, 63 V	
C29, C30	multilayer ceramic chip capacitor	0.7 pF	Murata: HiQ, GQM21 series, 0805
R1	resistor	50 Ω, 16 W	Anaren: C16A50Z4
R2, R3	resistor	4.7 Ω, 1 % tolerance	SMD 0805
CPL1	coupler	2 dB, 90°	Anaren: X3C14F1-02S

7.5 Graphical data

7.5.1 Pulsed CW



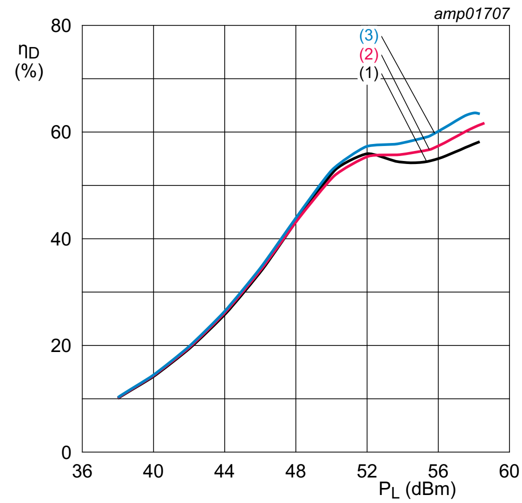
V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V; t_p = 100 μs; δ = 10 %.

(1) f = 1427 MHz

(2) f = 1472 MHz

(3) f = 1517 MHz

Fig 3. Power gain as a function of output power; typical values



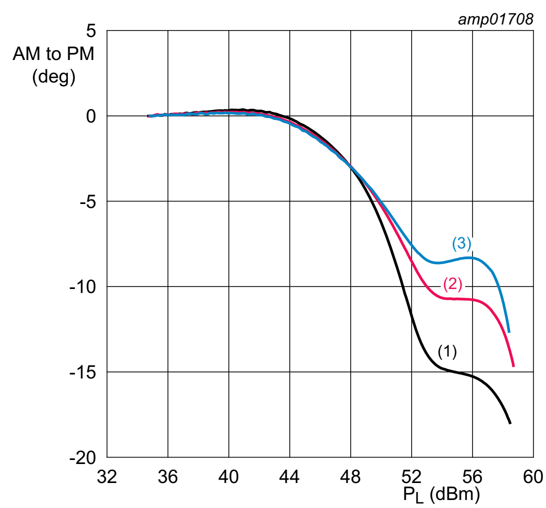
V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V; t_p = 100 μs; δ = 10 %.

(1) f = 1427 MHz

(2) f = 1472 MHz

(3) f = 1517 MHz

Fig 4. Drain efficiency as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V; t_p = 100 μs; δ = 10 %.

(1) f = 1427 MHz

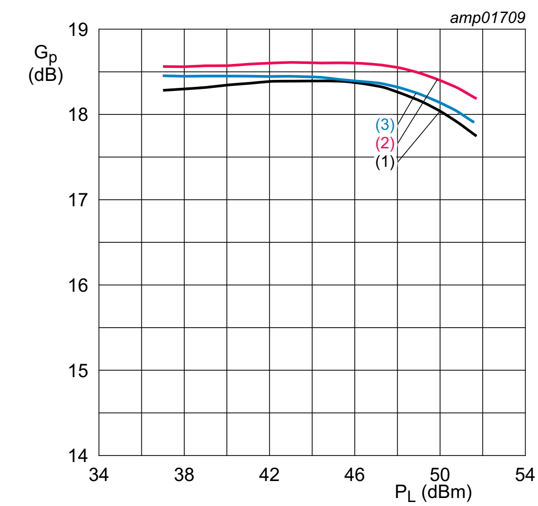
(2) f = 1472 MHz

(3) f = 1517 MHz

Fig 5. Normalized AM to PM as a function of output power; typical values

7.5.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping); PAR = 9.9 dB at 0.01 % probability on CCDF per carrier.



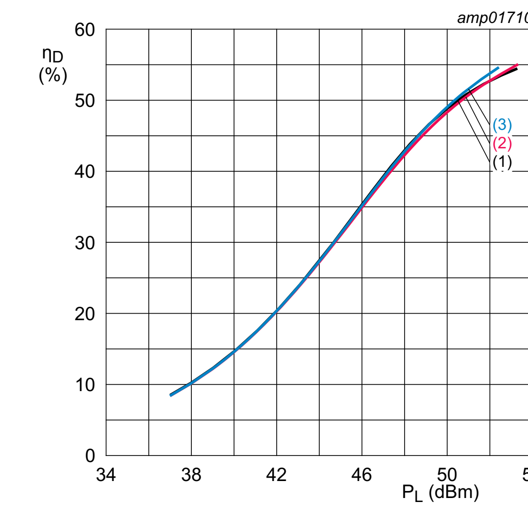
V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V.

(1) f = 1427 MHz

(2) f = 1472 MHz

(3) f = 1517 MHz

Fig 6. Power gain as a function of output power; typical values



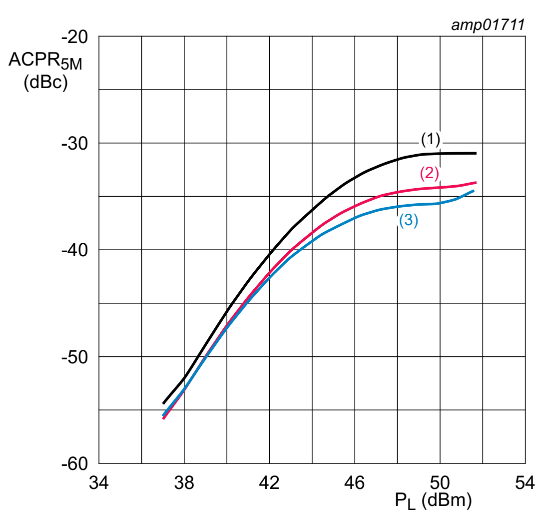
V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V.

(1) f = 1427 MHz

(2) f = 1472 MHz

(3) f = 1517 MHz

Fig 7. Drain efficiency as a function of output power; typical values



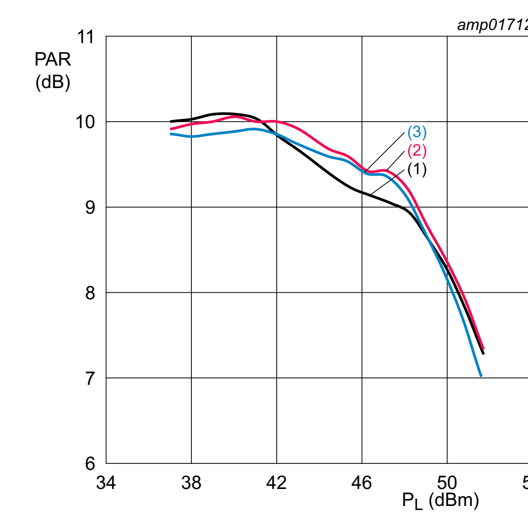
V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V.

(1) f = 1427 MHz

(2) f = 1472 MHz

(3) f = 1517 MHz

Fig 8. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V.

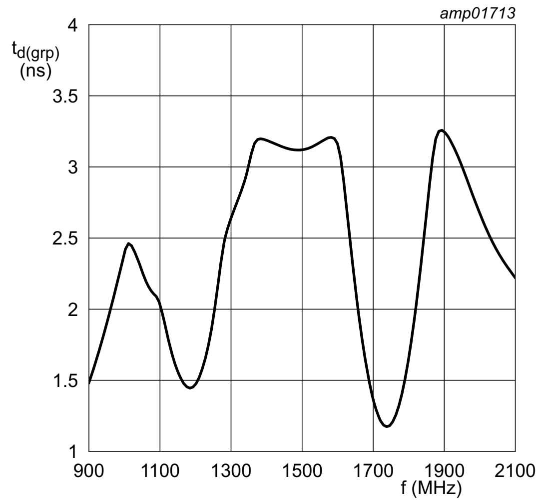
(1) f = 1427 MHz

(2) f = 1472 MHz

(3) f = 1517 MHz

Fig 9. Peak-to-average power ratio as a function of output power; typical values

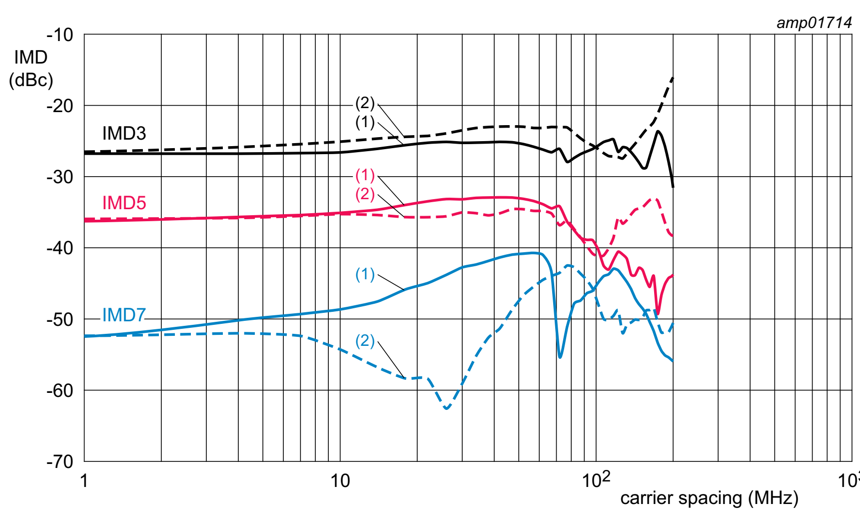
7.5.3 Group delay



V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V.

Fig 10. Group delay time as a function of frequency; typical values

7.5.4 2-Tone VBW



V_{DS} = 32 V; I_{Dq} = 1450 mA; $V_{GS(amp)peak}$ = 1.1 V: P_L = 50 dBm; f = 1472 MHz.

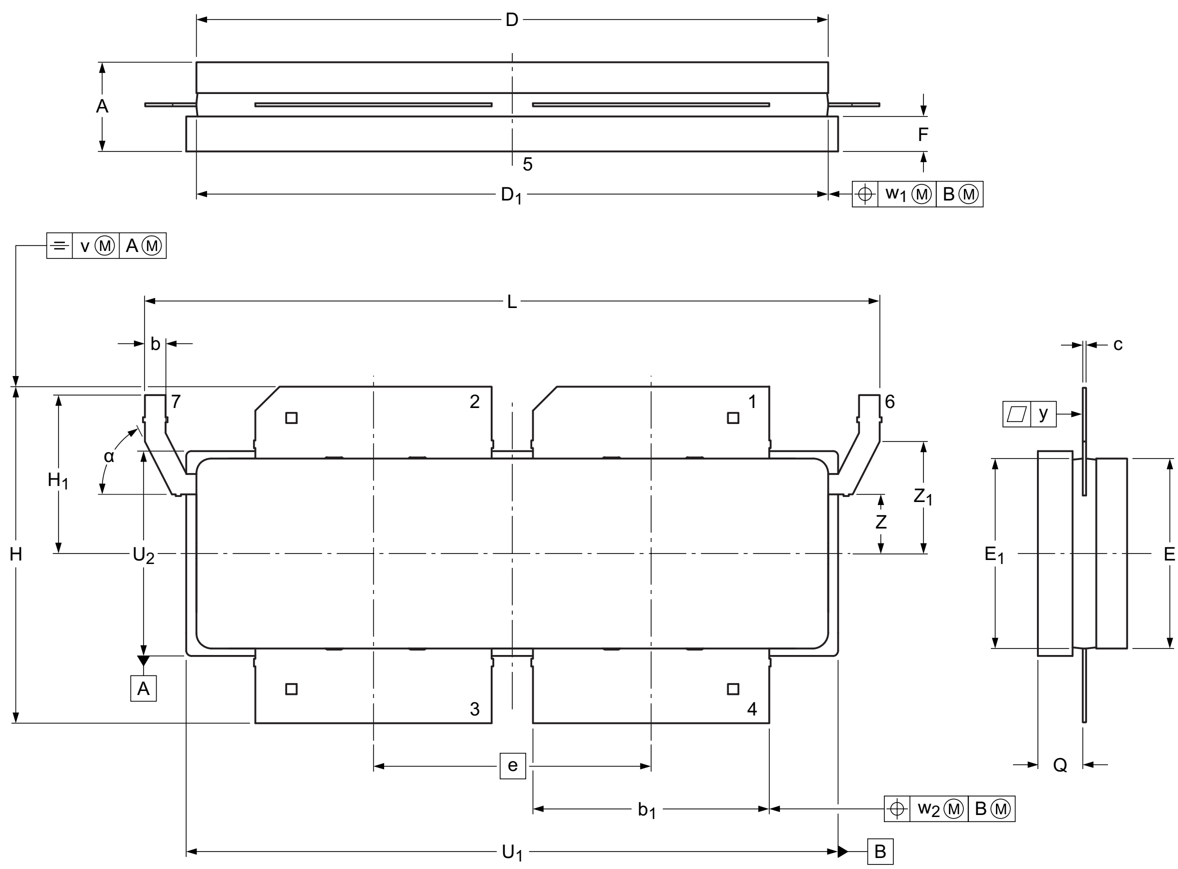
(1) IMD low

(2) IMD high

Fig 11. VBW capability

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-4**



0 10 mm
scale

y	α	Z	Z_1
0.1	65°	3.17	5.79
	61°	2.67	5.29

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	L	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2
mm	max	4.52	1.12	11.78	0.18	31.44	31.34	9.60	9.50		36.42	1.73	16.71	8.12	2.25	32.33	10.23	0.5	0.5	0.5
	nom									13.72										
	min	4.12	0.91	11.58	0.13	31.04	31.14	9.20	9.30		36.22	1.53	16.51	7.62	2.03	32.13	10.03			

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-4						17-08-31

Fig 12. Package outline SOT1258-4

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G16XS-600AVT v.1	20211216	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Ampleon does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Ampleon sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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12.3 Disclaimers

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13. Contact information

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