B11G2327N70D

LDMOS 2-stage integrated Doherty MMIC

Rev. 2 — 7 April 2022

AMPLEON

Product data sheet

1. Product profile

1.1 General description

The B11G2327N70D is a dual path 2-stage fully integrated Doherty MMIC solution using Ampleon's state of the art LDMOS technology. The carrier and peaking device, input splitter, output combiner and pre-match are integrated in a single package. This multiband device is perfectly suited as general purpose driver in the frequency range 2300 MHz to 2700 MHz. Available in PQFN outline.

Table 1. Application performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 290 mA (carrier and peaking); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.39$ V. Test signal: 1-carrier W-CDMA; PAR = 9.9 dB measured in an Ampleon f = 2500 MHz integrated Doherty application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
1-carrier W-CDMA	2500	28	5	30.3	20.7

1.2 Features and benefits

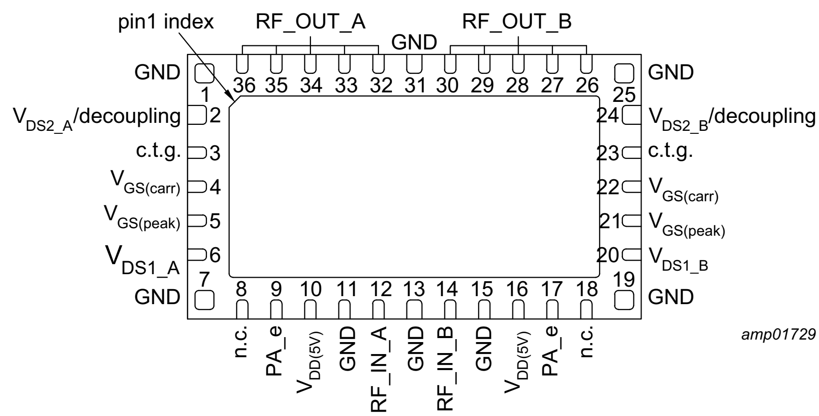
- Integrated input splitter
- Integrated output combiner
- 20 Ω output impedance thanks to integrated pre-match
- High linearity
- Designed for large RF and instantaneous bandwidth operation
- Independent control of carrier and peaking bias
- Integrated bias gate switch
- Integrated ESD protection
- Source impedance 50 Ω; high power gain
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Macrocell base station driver
- Microcell base station
- 5G mMIMO
- W-CDMA/LTE
- Active antenna
- General purpose applications

2. Pinning information

2.1 Pinning



Transparent top view.

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	1	ground
V_{DS2_A}/decoupling	2	drain-source voltage of final stages of section A
c.t.g.	3	connect to ground
$V_{GS(carr)}$	4	gate-source voltage of carrier [1]
$V_{GS(peak)}$	5	gate-source voltage of peaking [2]
V_{DS1_A}	6	drain-source voltage of driver stages of section A
GND	7	ground
n.c.	8	not connected
PA_e	9	PA enable trigger signal, 0 V to 5 V, I_{Dq}-bias ON/OFF corresponds to logic HIGH/LOW [3]
$V_{DD(5V)}$	10	supply voltage (5 V) [4]
GND	11	ground
RF_IN_A	12	RF input of section A
GND	13	ground
RF_IN_B	14	RF input of section B
GND	15	ground
$V_{DD(5V)}$	16	supply voltage (5 V) [4]
PA_e	17	PA enable trigger signal, 0 V to 5 V, I_{Dq}-bias ON/OFF corresponds to logic HIGH/LOW [3]
n.c.	18	not connected
GND	19	ground

Table 2. Pin description *...continued*

Symbol	Pin	Description
V_{DS1_B}	20	drain-source voltage of driver stages of section B
$V_{GS(peak)}$	21	gate-source voltage of peaking [2]
$V_{GS(carr)}$	22	gate-source voltage of carrier [1]
c.t.g.	23	connect to ground
V_{DS2_B}/decoupling	24	drain-source voltage of final stages of section B
GND	25	ground
RF_OUT_B	26, 27, 28, 29, 30	RF output of section B
GND	31	ground
RF_OUT_A	32, 33, 34, 35, 36	RF output of section A

[1] Pins connected together.

[2] Pins connected together.

[3] Pins connected together.

[4] Pins connected together.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
PQFN-12x7-36-1	B11G2327N70DX	9349 604 69525	TR13; 1500-fold; 24 mm; dry pack	1500
PQFN-12x7-36-1	B11G2327N70DYZ	9349 604 69535	TR7; 300-fold; 24 mm; dry pack	300

4. Block diagram

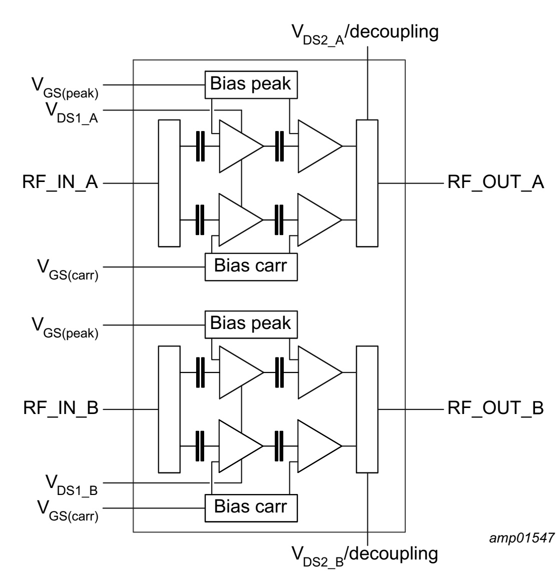


Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	200	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics

Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C		
		P_L = 5 W [1]	1.3	K/W
		P_L = 10 W [1]	1.2	K/W

[1] When operated with a 1-carrier W-CDMA with PAR = 9.9 dB.

7. Characteristics

Table 6. DC characteristics

T_{case} = 25 °C; $V_{DD(5V)}$ = 5 V; $V_{on(PA\_e)}$ = 5 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 274 mA	1.6	2.2	2.7	V
I_{GSS}	gate leakage current	V_{GS} = 2 V; V_{DS} = 0 V	-	-	140	nA
Peaking						
I_{GSS}	gate leakage current	V_{GS} = 2 V; V_{DS} = 0 V	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA

Table 7. RF characteristics

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 274 mA (carrier); f = 2500 MHz; $V_{DD(5V)}$ = 4.8 V; $V_{on(PA\_e)}$ = 5 V; $V_{GSq(peaking)}$ = $V_{GSq(carrier)}$ − 0.33 V; $P_{L(AV)}$ = 5 W; unless otherwise specified, measured in an Ampleon combined production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: pulsed CW [1]						
G_p	power gain	P_L = 5 W (37 dBm)	27.5	30.0	33.5	dB
η_D	drain efficiency	P_L = 5 W (37 dBm)	16	22	-	%
		P_L = $P_{L(3dB)}$	46	54	-	%
RL_{in}	input return loss		-	–15	–10	dB
$P_{L(3dB)}$	output power at 3 dB gain compression		48.0	49.5	-	dBm

[1] Pulsed CW power sweep measurement (δ = 10 %, t_p = 100 μs).

8. Application information

8.1 Typical performance

Table 8. Typical performance

T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 290 mA (carrier and peaking); $V_{GSq(peaking)}$ = $V_{GSq(carrier)}$ − 0.39 V; $V_{DD(5V)}$ = 5 V; $V_{on(PA\_e)}$ = 5 V. Test signal: 1-carrier W-CDMA; PAR = 9.9 dB; unless otherwise specified, measured in an Ampleon 2300 MHz to 2700 MHz frequency band combined application circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	f = 2500 MHz [1]	-	49.5	-	dBm
$\varphi_{s21}/\varphi_{s21(norm)}$	normalized phase response	at 1 dB compression point; f = 2500 MHz [2]	-	–7.2	-	°
η_D	drain efficiency	13.1 dB OBO ($P_{L(AV)}$ = 37 dBm); f = 2500 MHz	-	20.7	-	%
G_p	power gain	$P_{L(AV)}$ = 37 dBm; f = 2500 MHz	-	30.3	-	dB
B_{video}	video bandwidth	$P_{L(AV)}$ = 37 dBm set to obtain IMD3 = –45 dBc; f = 2500 MHz	-	320	-	MHz
G_{flat}	gain flatness	$P_{L(AV)}$ = 37 dBm; f = 2300 MHz to 2700 MHz	-	0.9	-	dB
$ACPR_{20M}$	adjacent channel power ratio (20 MHz)	$P_{L(AV)}$ = 37 dBm; f = 2500 MHz	-	–46.2	-	dBc
ΔG/ΔT	gain variation with temperature	f = 2500 MHz	-	0.047	-	dB/°C
K	Rollett stability factor	T_{case} = –40 °C to +125 °C; f = 0.1 GHz to 8 GHz	-	>1	-	
Bias gate switch						
t_r	rise time	Z_S = 500 Ω (max); T_{case} = –40 °C to +120 °C; $V_{on(PA\_e)}$ ≥ 4.8 V [3]	-	200	-	ns
t_f	fall time	T_{case} = –40 °C to +120 °C; $V_{off(PA\_e)}$ ≤ 1 V [4]	-	80	-	ns

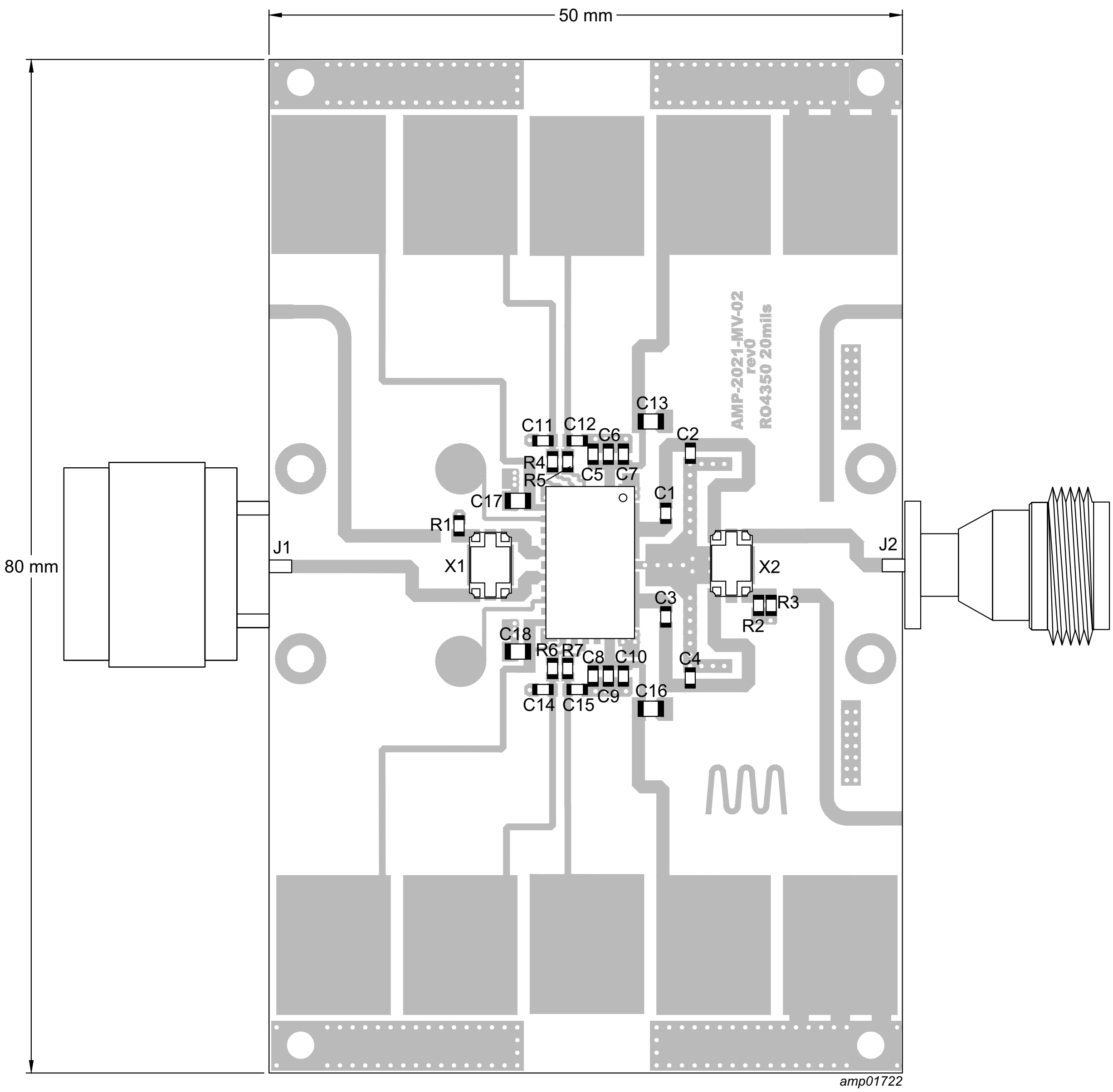
[1] Pulsed CW power sweep measurement (δ = 10 %, t_p = 100 μs).

[2] 25 ms CW power sweep measurement.

[3] RF output rise time 10 % to 90 % RF power.

[4] RF output fall time 90 % to 10 % RF power.

8.2 PCB layout and electrical schematic



Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.508 mm

Fig 3. Component layout

Table 9. Demo test circuit list of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C3	multilayer ceramic chip capacitor	3.3 pF, ± 0.1 %	Murata: GQM1875C2E3R3BB12
C2, C4	multilayer ceramic chip capacitor	0.8 pF, ± 0.1 %	Murata: GQM1875C2ER80BB12
C5, C6, C7, C8, C9, C10	multilayer ceramic chip capacitor	100 nF, 50 V	Murata: 06035C104KAT2A

Table 9. Demo test circuit list of components *...continued*

See Figure 3 for component layout.

Component	Description	Value	Remarks
C11, C12, C14, C15	multilayer ceramic chip capacitor	1 μF, 50 V	Murata: C1608X5R1H105K080AB
C13, C16, C17, C18	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: GRM21BR6YA106KE43
R1	resistor	49.9 Ω, ± 1 %, 100 mW	Multicomp Pro: MCWF06R49R9BTL
R2, R3	resistor	100 Ω, ± 1 %, 200 mW	Multicomp Pro: MP001293
R4, R5, R6, R7	resistor	1 kΩ, ± 1 %, 100 mW	Multicomp Pro: MCSR06X1001FTL
X1, X2	hybrid coupler	2.1 GHz – 2.7 GHz, 20 W	Anaren: X3C25F1-03S
J1	N Coaxial panel connector male		Radiall: R161.438.200
J2	N Coaxial panel connector female		Huber & Suhner: 23_N-50-0-16/133_NE

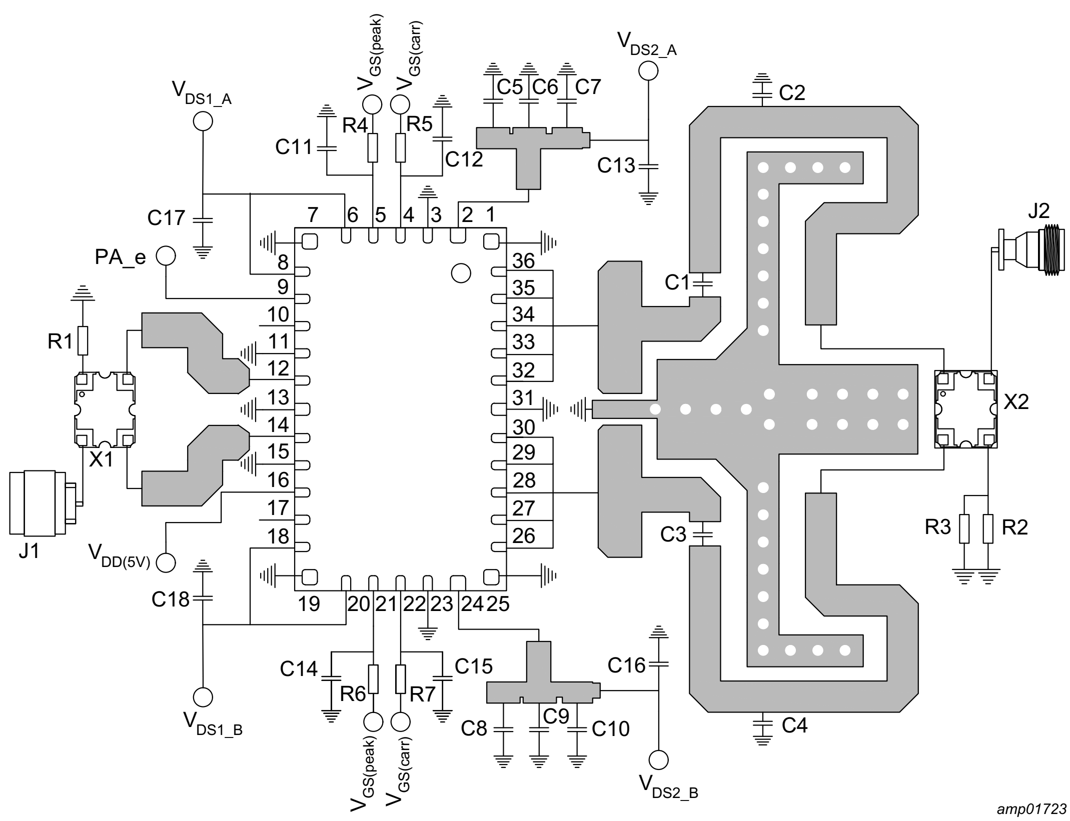


Fig 4. Electrical schematic

8.3 Recommendations

- RC circuit at gate bias must be implemented to insure improved linearity and stability of the circuit. The implementation has to be symmetrical between both amplifier sections Pin 5/21 and Pin 4/22.
- In TDD mode controlled by an external bias switch, the outputs of the switches must be connected on both amplifier sections. As shown in Fig.4, gate bias supply must be connected before RC circuit of Pin 5/21 and Pin 4/22 respectively by default.

8.4 Ruggedness in a Doherty operation

8.4.1 Output mismatch ruggedness

The B11G2327N70D is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 137 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.33$ V; $V_{DD(5V)}$ = 5 V; $V_{on(PA\_e)}$ = 5 V; P_i corresponding to $P_{L(1dB)}$ – 9 dB under Z_S = 50 Ω load; f = 2700 MHz (1-carrier W-CDMA); T_{case} = 25 °C; per section.

8.4.2 Wideband noise ruggedness

The B11G2327N70D is capable of withstanding an AWGN (Additive White Gaussian Noise) with 11.2 dB PAR, OBW (Occupied BandWidth) of 400 MHz, under the following conditions: V_{DS} = 32 V; I_{Dq} = 137 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.33$ V; $V_{DD(5V)}$ = 5 V; $V_{on(PA\_e)}$ = 5 V; 3 dB P_i overdrive from $P_{L(AV)}$ = 34 dBm (corresponding to $P_{L(3dB)}$ – 12 dB); f = 2500 MHz as central frequency; T_{case} = 25 °C; per section.

8.5 Impedance information

Table 10. Typical impedance for optimum Doherty operation

Measured load-pull data per section; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 75 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.46$ V; $V_{DD(5V)}$ = 5 V; $V_{on(PA\_e)}$ = 5 V; t_p = 100 μs; δ = 10 %.

f	tuned for optimum Doherty operation				
	Z_L [1]	$P_{L(1dB)}$	$G_{p(max)}$	η_{add} [2]	η_{add} [3]
(MHz)	(Ω)	(dBm)	(dB)	(%)	(%)
2200	18.7 – j18.5	46.5	30.7	48.5	22.0
2300	18.7 – j13.1	46.3	30.8	51.8	21.6
2500	19.1 – j4.4	46.3	31.1	57.2	20.7
2700	23.8 – j4.9	46.5	31.1	57.3	20.8
2800	25.7 – j3.9	46.2	30.2	55.3	19.3

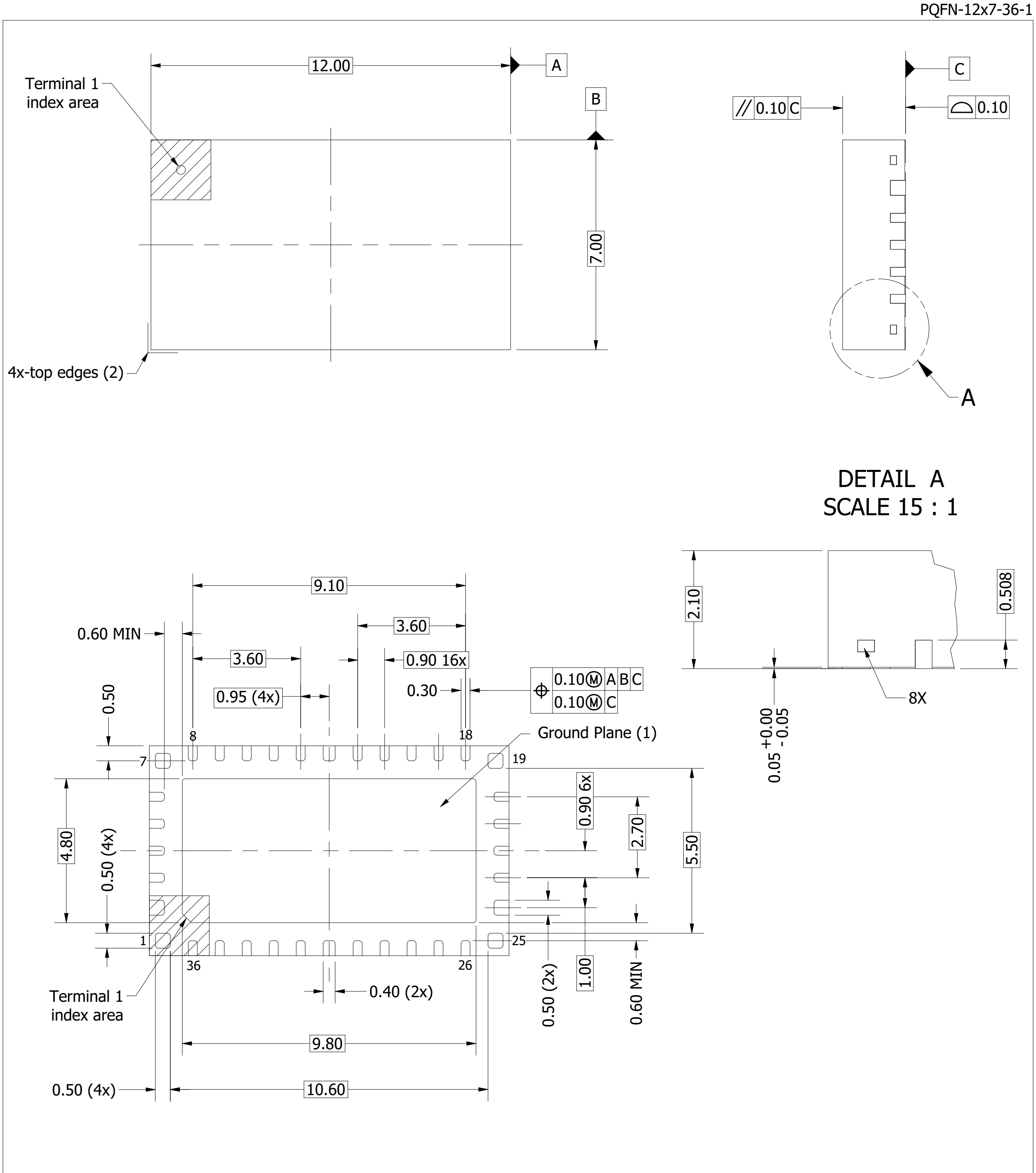
[1] Reference package plane.

[2] At $P_{L(1dB)}$.

[3] At 34 dBm.

9. Package outline

PQFN-12x7-36-1



Package outline drawing: PQFN-12x7-36-1 Publication	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.10 Angle: ± 1°	Revision: 1 Revision date: 23-Nov-21
		Third angle projection	Sheet 1 of 2

Fig 5. Package outline PQFN-12x7-36-1 (sheet 1 of 2)

PQFN-12x7-36-1

Drawing Notes	
Items	Description
(1)	Terminals (bottom View), Ground-plane (bottom View) and Lead step-cut are plated with matte Sn.
(2)	Plastic protrusions of 0.075 mm. max. per side are not included.

Package outline drawing:	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.10 Angle: ± 1°	Revision: 1 Revision date: 23-Nov-21
PQFN-12x7-36-1 Publication		Third angle projection	Sheet 2 of 2

Fig 6. Package outline PQFN-12x7-36-1 (sheet 2 of 2)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
5G	Fifth Generation
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
mMIMO	massive Multiple Input Multiple Output
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
OBO	Output Back Off
PA	Power Amplifier
PAR	Peak-to-Average power Ratio
RC	resistor-capacitor
RoHS	Restriction of Hazardous Substances
TDD	Time Division Duplex
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
B11G2327N70D v.2	20220407	Product data sheet	-	B11G2327N70D v.1
Modifications:	• Table 3 on page 3: added second orderable part number • Section 13.2 on page 13: updated section • Section 13.3 on page 13: updated section			
B11G2327N70D v.1	20211224	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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15. Contents

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