B10H0710N40D

LDMOS 2-stage integrated Doherty MMIC

AMPLEON

Rev. 1 — 11 September 2023 Product data sheet

1. Product profile

1.1 General description

The B10H0710N40D is a dual section 2-stage fully integrated Doherty MMIC solution using Ampleon's state of the art 50 V LDMOS technology. The carrier and peaking device, input splitter, output combiner and pre-match are integrated in each section. This multiband device is perfectly suited as general purpose driver in the frequency range 700 MHz to 1 GHz. Available in LGA outline.

Table 1. Application performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 72 mA (carrier and peaking); $V_{GSq(peaking)}$ = $V_{GSq(carrier)}$ − 0.5 V. Test signal: 1-carrier LTE 20 MHz measured in an Ampleon quad-combined application circuit at f = 845 MHz.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
1-carrier LTE 20 MHz PAR = 7.6 dB	845	48	2.512	30.3	28.1

1.2 Features and benefits

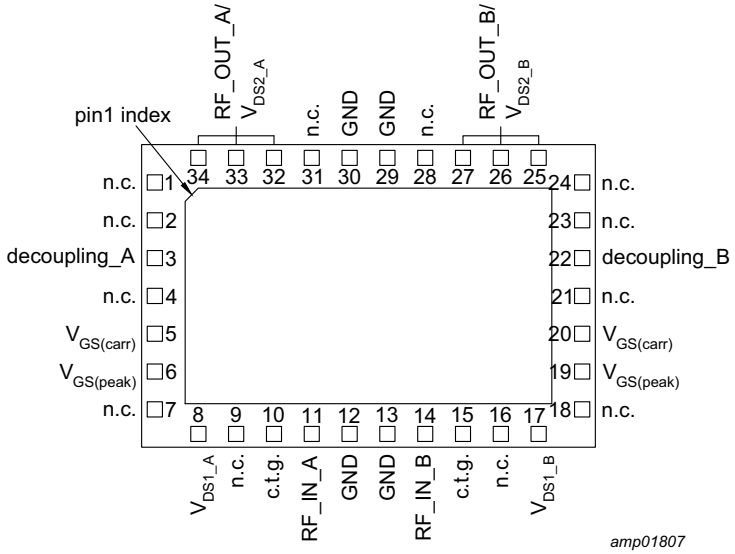
- Integrated input splitter
- Integrated output combiner
- Source impedance 50 Ω
- Pre-matched output
- No output circulator needed thanks to quad-combined configuration
- High linearity
- Designed for large RF and instantaneous bandwidth operation
- Independent control of carrier and peaking bias
- Integrated ESD protection
- High power gain
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- 4G/5G macrocell base station driver
- 4G/5G microcell base station

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
n.c.	2	not connected
decoupling_A	3	video-lead for decoupling of section A
n.c.	4	not connected
$V_{GS(carr)}$	5	gate-source voltage of carrier [1]
$V_{GS(peak)}$	6	gate-source voltage of peaking [2]
n.c.	7	not connected
V_{DS1_A}	8	drain-source voltage of driver stages of section A
n.c.	9	not connected
c.t.g.	10	connect to ground
RF_IN_A	11	RF input of section A
GND	12	ground
GND	13	ground
RF_IN_B	14	RF input of section B
c.t.g.	15	connected to ground
n.c.	16	not connected
V_{DS1_B}	17	drain-source voltage of driver stages of section B

Table 2. Pin description *…continued*

Symbol	Pin	Description
n.c.	18	not connected
$V_{GS(peak)}$	19	gate-source voltage of peaking [2]
$V_{GS(carr)}$	20	gate-source voltage of carrier [1]
n.c.	21	not connected
decoupling_B	22	video-lead for decoupling of section B
n.c.	23	not connected
n.c.	24	not connected
RF_OUT_B/V_{DS2_B}	25, 26, 27	RF output and drain-source voltage of final stages of section B
n.c.	28	not connected
GND	29	ground
GND	30	ground
n.c.	31	not connected
RF_OUT_A/V_{DS2_A}	32, 33, 34	RF output and drain-source voltage of final stages of section A

[1] Pins connected together.

[2] Pins connected together.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
LGA-12x8-34-2	B10H0710N40DX	9349 606 85525	TR13; 3000-fold; 24 mm; dry pack	3000
	B10H0710N40DYZ	9349 606 85535	TR7; 500-fold; 24 mm; dry pack	500

4. Block diagram

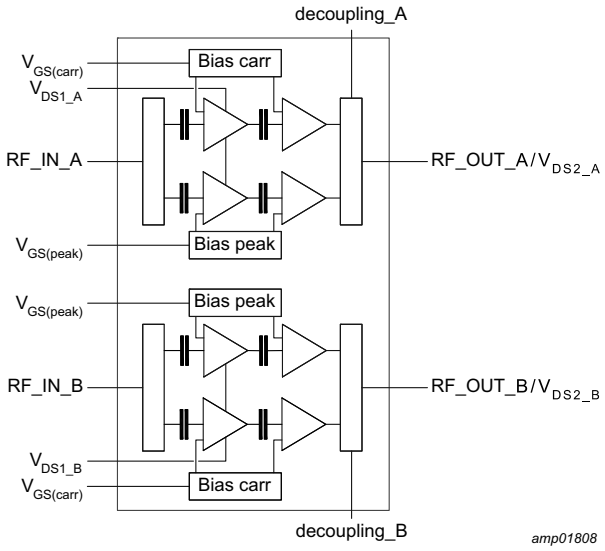


Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–55	+125	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	[1]	-	125	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain source voltage	T_{case} = –40 °C to +120 °C	40	52	V
T_{case}	case temperature		–40	+120	°C
$P_{i(M)}$	peak input power	T_{case} = 25 °C; VSWR = 1 : 1; V_{DS} = V_{DS} (max); pulsed CW power sweep measurement (δ = 10 %; t_p = 100 µs).	-	19	dBm

7. Thermal characteristics

Table 6. Thermal characteristics
Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; P_L = 2.512 W	4.1	K/W

[1] When operated with a 1-carrier W-CDMA with PAR = 9.9 dB.

8. Characteristics

Table 7. DC characteristics
T_{case} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 48 V; I_D = 70 mA	1.65	2.0	2.65	V
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	120	nA
Peaking						
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	120	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 105 V	-	-	1.4	µA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 105 V	-	-	1.4	µA

Table 8. RF characteristics
Typical RF performance at T_{case} = 25 °C; V_{DS} = 48 V; I_{Dq} = 70 mA (carrier); f = 848 MHz; $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; $P_{L(AV)}$ = 34 dBm; unless otherwise specified, measured in an Ampleon combined production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: pulsed CW [1]						
G_p	power gain	P_L = 2.51 W (34 dBm)	27	31	35	dB
η_D	drain efficiency	P_L = 2.51 W (34 dBm)	20	25	-	%
		$P_L = P_{L(1db)}$	50	54	-	%
RL_{in}	input return loss	P_L = 2.51 W (34 dBm)	-	−20	−10	dB
$P_{L(1dB)}$	output power at 1 dB gain compression	$P_L = P_{L(1db)}$	46.5	47.0	-	dBm

[1] Pulsed CW power sweep measurement (δ = 10 %, t_p = 100 µs).

9. Application information

9.1 Typical performance

Table 9. Typical performance

T_{case} = 25 °C; V_{DS} = 48 V; I_{Dq} = 72 mA; $V_{GSq(peaking)}$ = $V_{GSq(carrier)}$ − 0.5 V. Test signal: 1-carrier W-CDMA; PAR = 9.9 dB; measured at 730 MHz to 960 MHz frequency band in an Ampleon quad-combined application circuit.

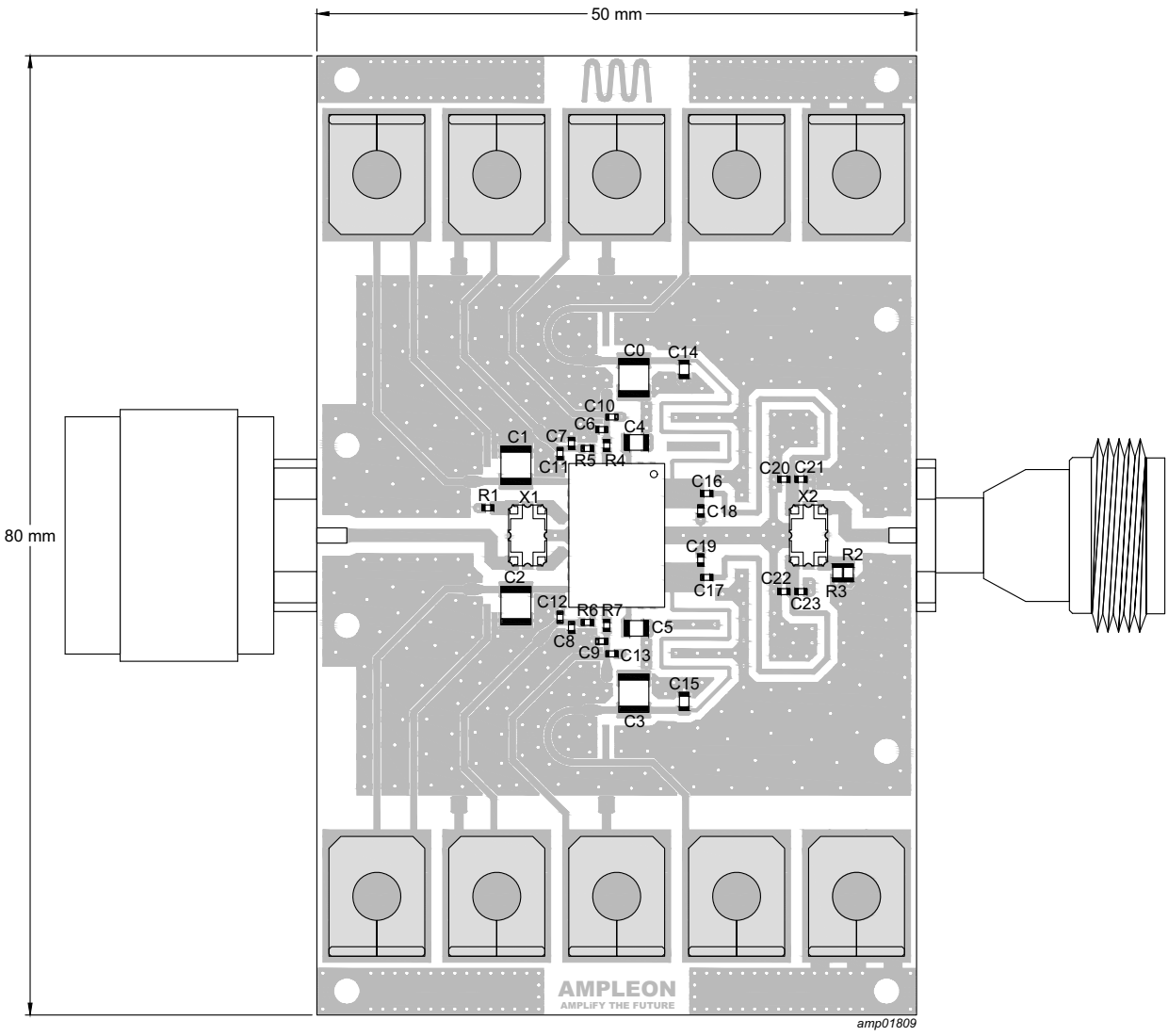
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	f = 845 MHz [1]	-	47.4	-	dBm
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 845 MHz [1]	-	48.0	-	dBm
$\varphi_{s21}/\varphi_{s21(norm)}$	normalized phase response	at 1 dB compression point; f = 845 MHz [2]	-	−9.3	-	°
η_D	drain efficiency	$P_{L(AV)}$ = 34 dBm; f = 845 MHz	-	28.1	-	%
G_p	power gain	$P_{L(AV)}$ = 34 dBm; f = 845 MHz	-	30.5	-	dB
B_{video}	video bandwidth	$P_{L(AV)}$ = 37.5 dBm set to obtain IMD3 = −30 dBc; 2-tone CW; f = 845 MHz	-	161	-	MHz
G_{flat}	gain flatness	$P_{L(AV)}$ = 34 dBm; f = 730 MHz to 960 MHz	-	0.3	-	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 34 dBm; f = 845 MHz	-	−37.3	-	dBc
$\Delta G/\Delta T$	gain variation with temperature	f = 845 MHz [3]	-	0.05	-	dB/°C
K	Rollett stability factor	T_{case} = −40 °C; f = 0.1 GHz to 3 GHz [3]	-	>1	-	

[1] Pulsed CW power sweep measurement (t_p = 100 μs; δ = 10 %).

[2] 25 ms CW power sweep measurement.

[3] Small-signal s-parameters.

9.2 Component layout



Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.508 mm.

Fig 3. Component layout

Table 10. Demo test circuit list of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C0, C1, C2, C3	multilayer ceramic chip capacitor	10 µF, 100 V	Murata: GRM32EC72A106KE05K
C4, C5	multilayer ceramic chip capacitor	1 µF, 100 V	Murata: CGA4J3X7S2A105K125AB
C6, C7, C8, C9	multilayer ceramic chip capacitor	100 nF, 6.3 V	Murata: GRM155R70J104KA01D
C10, C11, C12, C13	multilayer ceramic chip capacitor	4.7 µF, 6.3 V	Murata: GCJ188C70J475ME02D
C14, C15	multilayer ceramic chip capacitor	51 pF, 250 V	Murata: GQM1875C2E510FB12D
C16, C17	multilayer ceramic chip capacitor	6.2 pF, 200 V	Murata: GQM1555C2D6R2BB01D
C18, C19	multilayer ceramic chip capacitor	2 pF, 200 V	Murata: GQM1555C2D2R0BB01D

Table 10. Demo test circuit list of components *…continued*
See Figure 3 for component layout.

Component	Description	Value	Remarks
C20, C21, C22, C23	multilayer ceramic chip capacitor	1.5 pF, 200 V	Murata: GQM1555C2D1R5BB01D
R1	resistor	50 Ω, ±1 %, 100 mW	Vishay: FC0402E50R0BST1
R2, R3	resistor	100 Ω, ±1 %, 200 mW	Multicomp Pro: MP001293
R4, R5, R6, R7	resistor	0 Ω, ±1 %, 100 mW	Multicomp Pro: MCSR06X000PTL
X1, X2	hybrid coupler	600 MHz – 1000 MHz, 25 W	Anaren: X3C07F1-03S
J1	N coaxial panel connector male		Radiall: R161.438.200
J2	N coaxial panel connector female		Huber & Suhner: 23_N-50-0-16/133_NE

9.3 Recommendations

It is mandatory to use the B10H0710N40D in quad-combined configuration.

9.4 Ruggedness in a Doherty operation

9.4.1 Output mismatch ruggedness

The B10H0710N40D is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 52 V; I_{Dq} = 70 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; P_i corresponding to $P_{L(1dB)} - 9$ dB under Z_S = 50 Ω load; f = 730 MHz (1-carrier W-CDMA); T_{case} = 25 °C.

9.4.2 Wideband noise ruggedness

The B10H0710N40D is capable of withstanding an AWGN (Additive White Gaussian Noise) with 11.2 dB PAR, OBW (Occupied BandWidth) of 900 MHz, under the following conditions: V_{DS} = 52 V; I_{Dq} = 70 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; 3 dB P_{out} overdrive from $P_{L(AV)}$ = 34 dBm; f = 845 MHz; T_{case} = 25 °C.

9.5 Impedance information

Table 11. Typical impedance for optimum Doherty operation
Measured load-pull data per section; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 48 V; I_{Dq} = 35 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; t_p = 100 µs; δ = 10 %.

f	tuned for optimum Doherty operation				
	Z_L	$P_{L(1dB)}$	$G_{p(max)}$	η_{add} [1]	η_{add} [2]
(MHz)	(Ω)	(dBm)	(dB)	(%)	(%)
729	33.30 – 6.50j	44.46	31.82	27.07	55.88
758	32.98 – 2.60j	44.55	32.20	28.22	56.88
803	32.91 – 0.13j	44.49	32.53	28.63	56.56
840	34.34 + 3.31j	44.31	32.62	27.69	56.18
900	33.62 + 5.03j	44.14	32.23	26.35	55.49
960	34.54 + 11.68j	43.82	31.92	26.60	56.98

[1] At 31 dBm.

[2] At $P_{L(1dB)}$.

10. Package outline

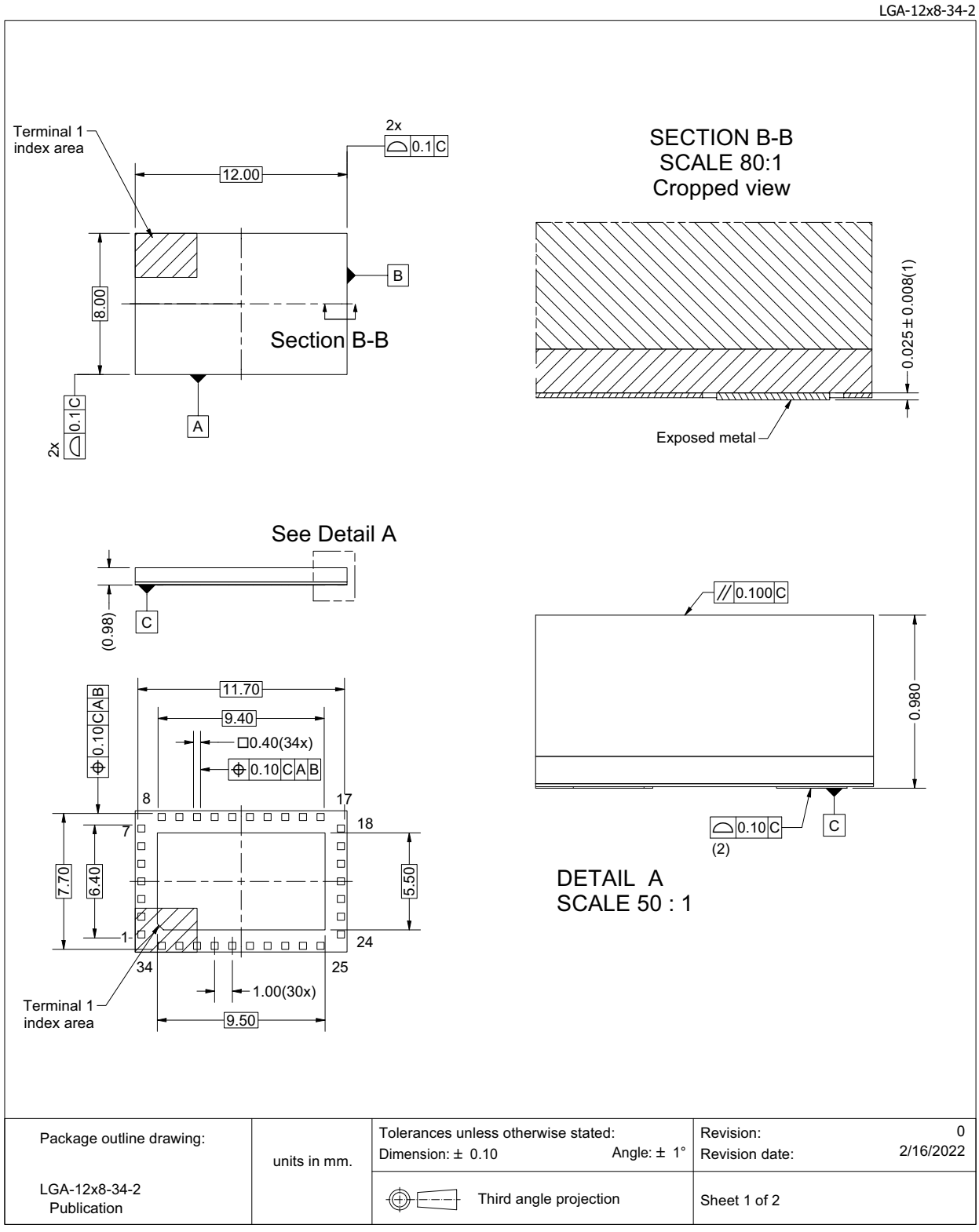


Fig 4. Package outline LGA-12x8-34-2 (sheet 1 of 2)

LGA-12x8-34-2

Drawing Notes	
Items	Description
(1)	Metal thickness of solder pads.
(2)	Flatness with respect to exposed metal

Package outline drawing: LGA-12x8-34-2	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.10 Angle: ± 1° Third angle projection	Revision: 0 Revision date: 2/16/2022 Sheet 2 of 2

Fig 5. Package outline LGA-12x8-34-2 (sheet 2 of 2)

11. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C1 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C1 is granted to any part that passes after exposure to an ESD pulse of 250 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V.

12. Abbreviations

Table 13. Abbreviations

Acronym	Description
4G	Fourth Generation
5G	Fifth Generation
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
PAR	Peak-to-Average power Ratio
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

13. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
B10H0710N40D v.1	20230911	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

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Date of release: 11 September 2023
Document identifier: B10H0710N40D