ART450FE

Power LDMOS transistor

Rev. 2 — 25 January 2024

AMPLEON

Product data sheet

1. Product profile

1.1 General description

Based on Advanced Rugged Technology (ART), this 450 W LDMOS RF transistor has been designed to cover a wide range of applications for ISM, broadcast and communications. The unmatched transistor has a frequency range of 1 MHz to 650 MHz.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	41	50	300	24.5	76
CW	41	65	450	25	72
CW pulsed [1][2]	108	50	350	28	75
CW pulsed [1][2]	225	65	450	27	77.5
CW [2]	225	65	450	26.5	77.0

[1] t_p = 100 μs; δ = 10 %.

[2] Test circuit.

1.2 Features and benefits

- High breakdown voltage enables class E operation up to V_{DS} = 53 V
- Qualified up to a maximum of V_{DS} = 65 V
- Characterized from 30 V to 65 V to support a wide range of applications
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness with no device degradation
- High efficiency
- Excellent thermal stability
- Designed for broadband operation
- For RoHS compliance see the product details on the Ampleon website

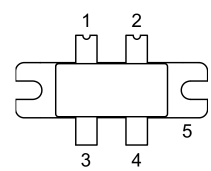
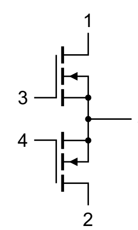
1.3 Applications

- Industrial, scientific and medical applications
  - Plasma generators
  - MRI systems
  - CO_2 lasers
  - Particle accelerators
  - Defrosting
- Broadcast
  - FM radio
  - VHF TV

- Radar
  - Non cellular communications
  - UHF radar

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
1	drain1			 sym117
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1121A	ART450FEU	9349 606 65112	Tray; 20-fold; non-dry pack	60

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	[1]	-	200	V
V_{GS}	gate-source voltage		–9	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[2]	-	225	°C

[1] Specified over lifetime at maximum operating temperature.

[2] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

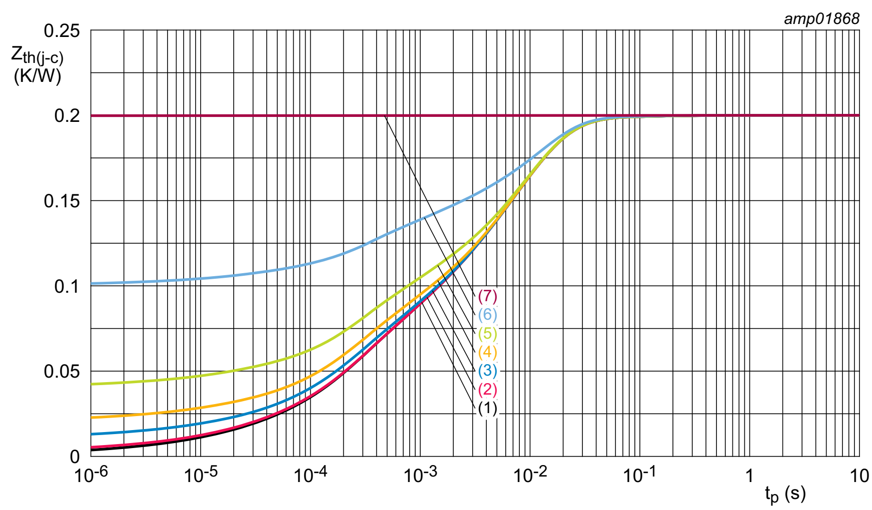
5. Thermal characteristics

Table 5. Thermal characteristics
According to standard MIL-STD-883E.

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 75 °C, measured under RF condition	[1][2]	0.2	K/W

[1] Refer to application note *AN221014* on the Ampleon website.

[2] See Figure 1.



(1) δ = 0.1 % (single pulse)

(2) δ = 1 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (steady state)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.5 mA	203	208	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 111 mA	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 65 V	-	-	1.4	μA

Table 6. DC characteristics *...continued*

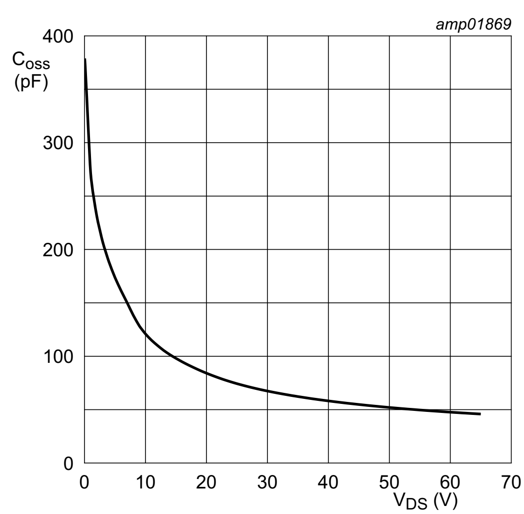
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 20 V	-	21	-	A
I_{GSS}	gate leakage current	V_{GS} = 13 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 3.885 A	-	0.340	-	Ω

Table 7. AC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; f = 1 MHz				
		V_{DS} = 50 V	-	-	0.36	pF
		V_{DS} = 65 V	-	-	0.33	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz				
		V_{DS} = 50 V	-	-	178	pF
		V_{DS} = 65 V	-	-	178	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz				
		V_{DS} = 50 V	-	-	52	pF
		V_{DS} = 65 V	-	-	46	pF



V_{GS} = 0 V; f = 1 MHz

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

Table 8. RF characteristics

Test signal: CW pulsed; t_p = 100 μs; δ = 10 %; f = 225 MHz; RF performance at V_{DS} = 65 V; I_{Dq} = 25 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 450 W	25.7	27.0	-	dB
RL_{in}	input return loss	P_L = 450 W	-	–15.5	–9	dB
η_D	drain efficiency	P_L = 450 W	70	74	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The ART450FE is capable of withstanding a load mismatch corresponding to VSWR = 65 ≥ 1 through all phases under the following conditions: V_{DS} = 65 V; I_{Dq} = 25 mA per section; P_L = 450 W pulsed; t_p = 100 μs; δ = 10 %; f = 225 MHz.

7.2 Impedance information

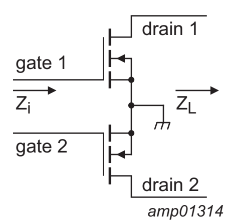


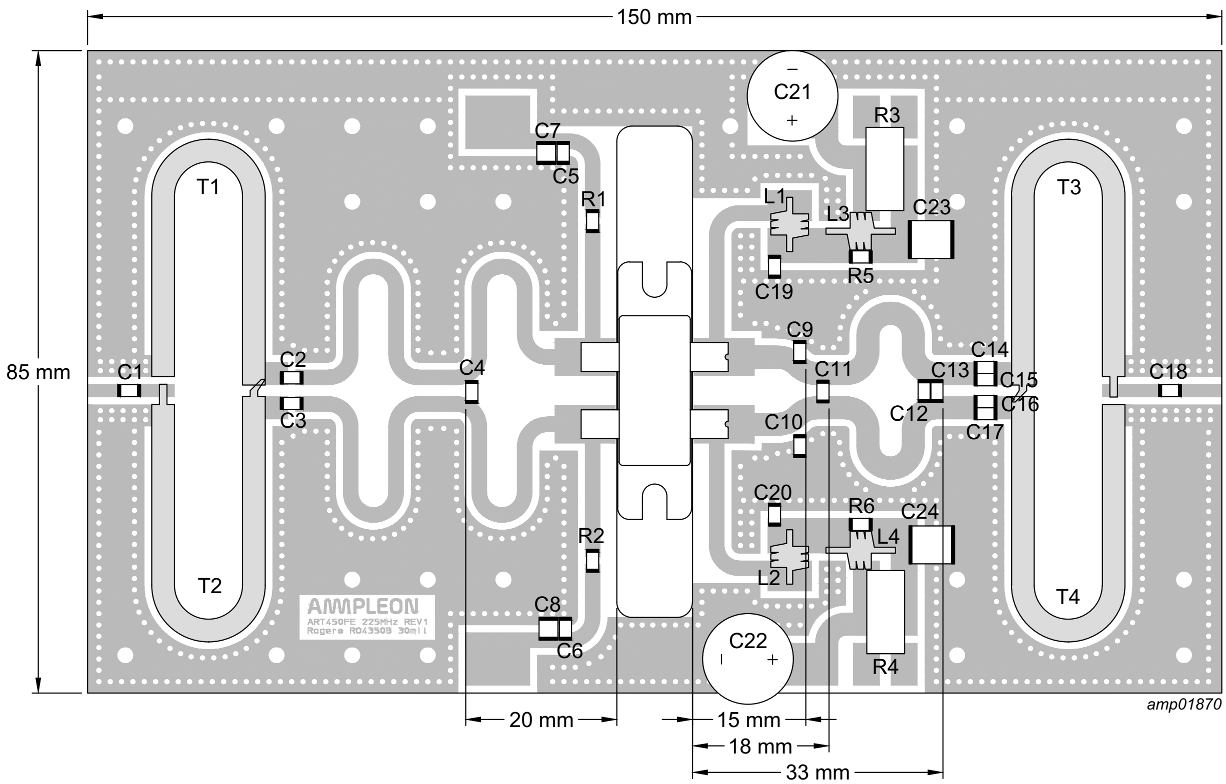
Fig 3. Definition of transistor impedance

Table 9. Typical impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 65 V and P_L = 450 W.

f	Z_i	Z_L
(MHz)	(Ω)	(Ω)
225	3.3 – j14.6	12.3 + j7.9

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.48 F/m; thickness = 0.762 mm.

See Table 10 for a list of components.

Fig 4. Component layout

Table 10. List of components

For test circuit see Figure 4.

Component	Description	Value	Remarks
C1, C18	multilayer ceramic chip capacitor	100 pF [1][2]	
C2, C3	multilayer ceramic chip capacitor	18 pF [1][2]	
C4, C14, C15, C16, C17	multilayer ceramic chip capacitor	27 pF [1][2]	
C5, C6, C19, C20	multilayer ceramic chip capacitor	620 pF [1][2]	
C7, C8	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata: GRM31CC72A475KE11L
C9, C10, C11	multilayer ceramic chip capacitor	22 pF [1][2]	
C12, C13	multilayer ceramic chip capacitor	15 pF [1][2]	
C21, C22	electrolytic capacitor	1000 μF, 100 V	
C23, C24	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK: CGA9N2X7R2A465K230
L1, L2	air core inductor	33 nH	Coilcraft: 1812SMS-33NGL
L3, L4	air core inductor	82 nH	Coilcraft 1812SMS-82NGL
R1, R2	chip resistor	510 Ω	SMD 1206

Table 10. List of components *...continued*
For test circuit see Figure 4.

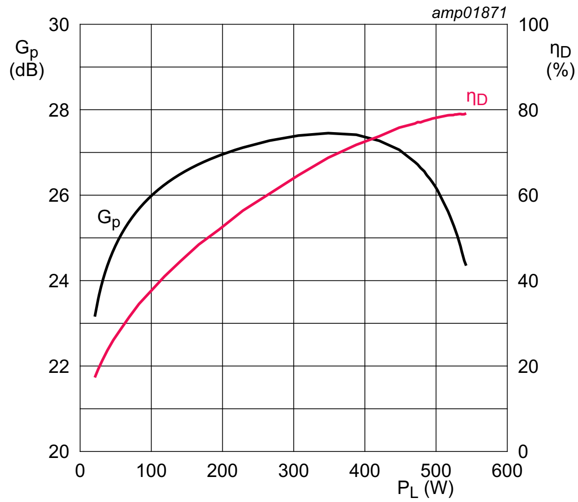
Component	Description	Value	Remarks
R3, R4	chip resistor	0.01 Ω	FC4L110R010FER
R5, R6	chip resistor	10 Ω, 2 x 20 Ω in parallel	SMD 1206
T1, T2, T3, T4	hand formable coax	50 Ω, 68 mm	Sucoform 141

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] Vertical mounted.

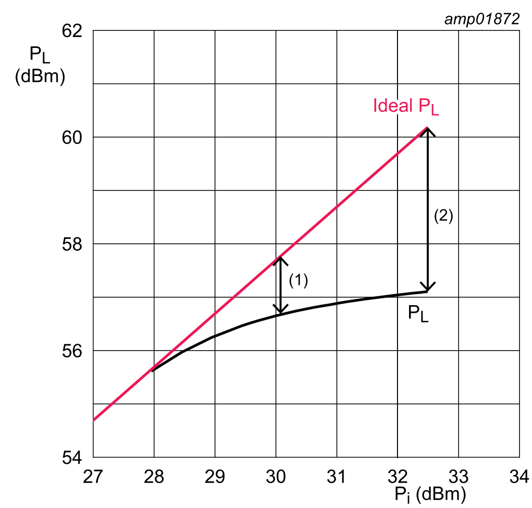
7.4 Graphical data

7.4.1 1-Tone CW pulsed



V_{DS} = 65 V; I_{Dq} = 25 mA per section; f = 225 MHz; t_p = 100 μs; δ = 10 %.

Fig 5. Power gain and drain efficiency as function of output power; typical values

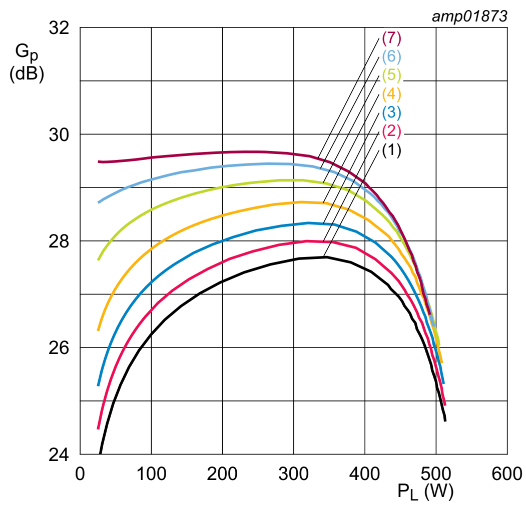


V_{DS} = 65 V; I_{Dq} = 25 mA per section; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) $P_{L(1dB)}$ = 56.63 dBm (460 W)

(2) $P_{L(3dB)}$ = 57.09 dBm (512 W)

Fig 6. Output power as a function of input power; typical values



V_{DS} = 65 V; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) I_{Dq} = 25 mA per section

(2) I_{Dq} = 50 mA per section

(3) I_{Dq} = 100 mA per section

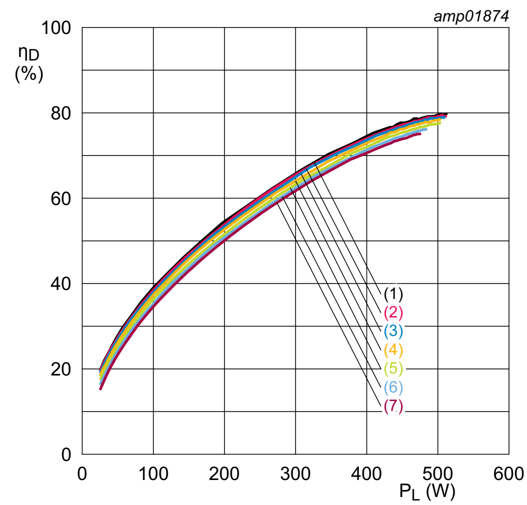
(4) I_{Dq} = 200 mA per section

(5) I_{Dq} = 400 mA per section

(6) I_{Dq} = 600 mA per section

(7) I_{Dq} = 800 mA per section

Fig 7. Power gain as a function of output power; typical values



V_{DS} = 65 V; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) I_{Dq} = 25 mA per section

(2) I_{Dq} = 50 mA per section

(3) I_{Dq} = 100 mA per section

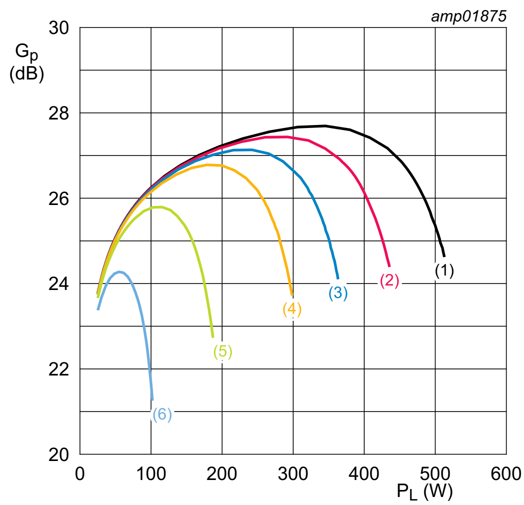
(4) I_{Dq} = 200 mA per section

(5) I_{Dq} = 400 mA per section

(6) I_{Dq} = 600 mA per section

(7) I_{Dq} = 800 mA per section

Fig 8. Drain efficiency as a function of output power; typical values



I_{Dq} = 25 mA per section; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 65 V

(2) V_{DS} = 60 V

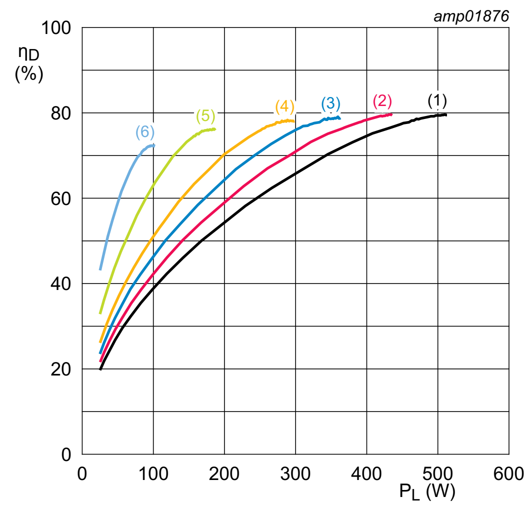
(3) V_{DS} = 55 V

(4) V_{DS} = 50 V

(5) V_{DS} = 40 V

(6) V_{DS} = 30 V

Fig 9. Power gain as a function of output power; typical values



I_{Dq} = 25 mA per section; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 65 V

(2) V_{DS} = 60 V

(3) V_{DS} = 55 V

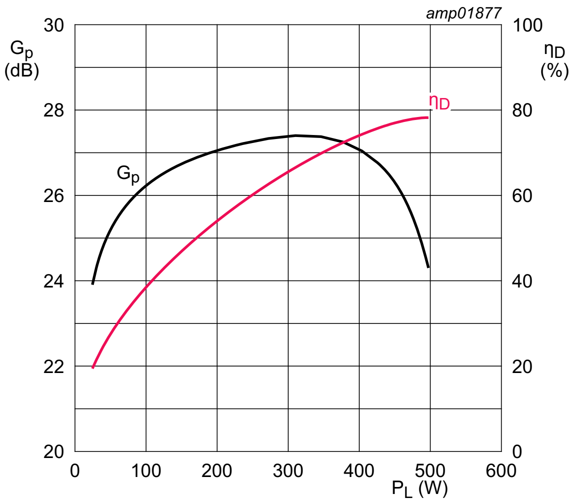
(4) V_{DS} = 50 V

(5) V_{DS} = 40 V

(6) V_{DS} = 30 V

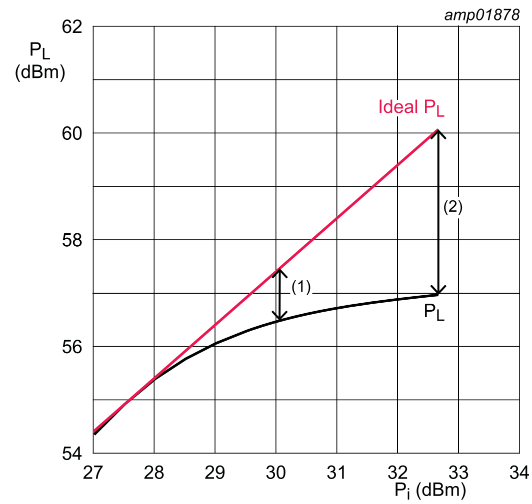
Fig 10. Drain efficiency as a function of output power; typical values

7.4.2 1- Tone CW



V_{DS} = 65 V; I_{Dq} = 25 mA per section; f = 225 MHz.

Fig 11. Power gain and drain efficiency as function of output power; typical values

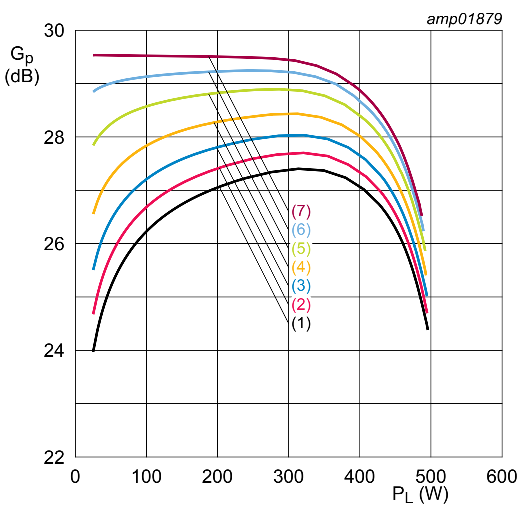


V_{DS} = 65 V; I_{Dq} = 25 mA per section; f = 225 MHz.

(1) $P_{L(1dB)}$ = 56.49 dBm (446 W)

(2) $P_{L(3dB)}$ = 56.95 dBm (496 W)

Fig 12. Output power as a function of input power; typical values



V_{DS} = 65 V; f = 225 MHz.

(1) I_{Dq} = 25 mA per section

(2) I_{Dq} = 50 mA per section

(3) I_{Dq} = 100 mA per section

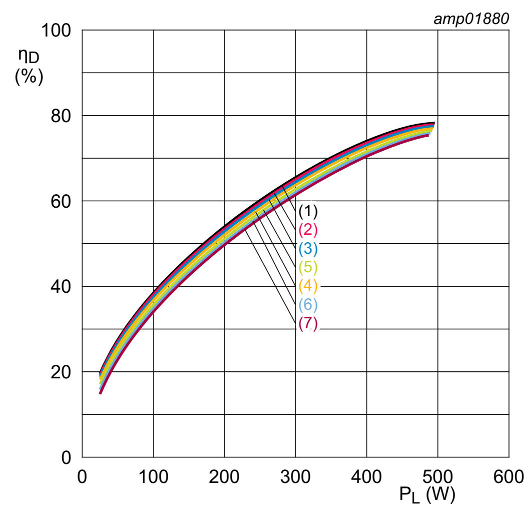
(4) I_{Dq} = 200 mA per section

(5) I_{Dq} = 400 mA per section

(6) I_{Dq} = 600 mA per section

(7) I_{Dq} = 800 mA per section

Fig 13. Power gain as a function of output power; typical values



V_{DS} = 65 V; f = 225 MHz.

(1) I_{Dq} = 25 mA per section

(2) I_{Dq} = 50 mA per section

(3) I_{Dq} = 100 mA per section

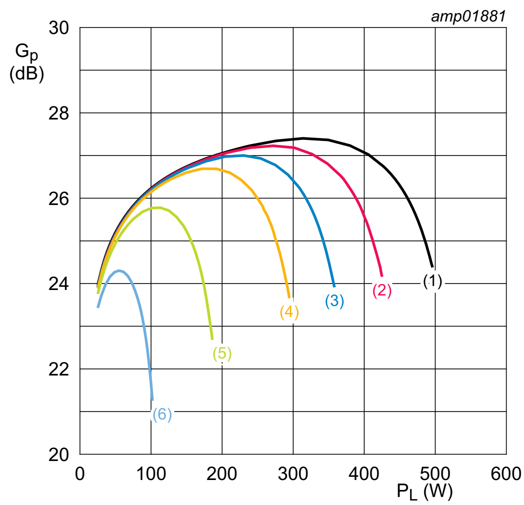
(4) I_{Dq} = 200 mA per section

(5) I_{Dq} = 400 mA per section

(6) I_{Dq} = 600 mA per section

(7) I_{Dq} = 800 mA per section

Fig 14. Drain efficiency as a function of output power; typical values



I_{Dq} = 25 mA per section; f = 225 MHz.

(1) V_{DS} = 65 V

(2) V_{DS} = 60 V

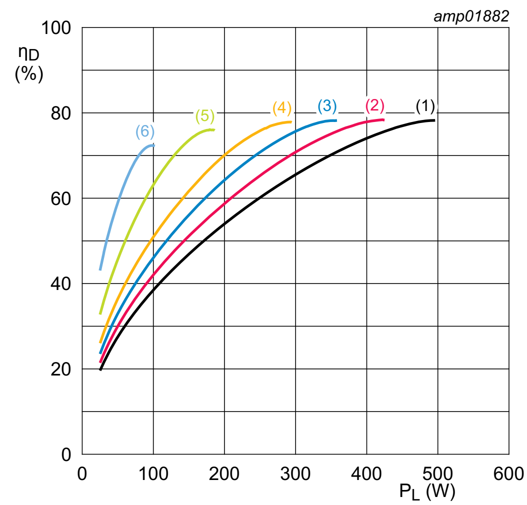
(3) V_{DS} = 55 V

(4) V_{DS} = 50 V

(5) V_{DS} = 40 V

(6) V_{DS} = 30 V

Fig 15. Power gain as a function of output power; typical values



I_{Dq} = 25 mA per section; f = 225 MHz.

(1) V_{DS} = 65 V

(2) V_{DS} = 60 V

(3) V_{DS} = 55 V

(4) V_{DS} = 50 V

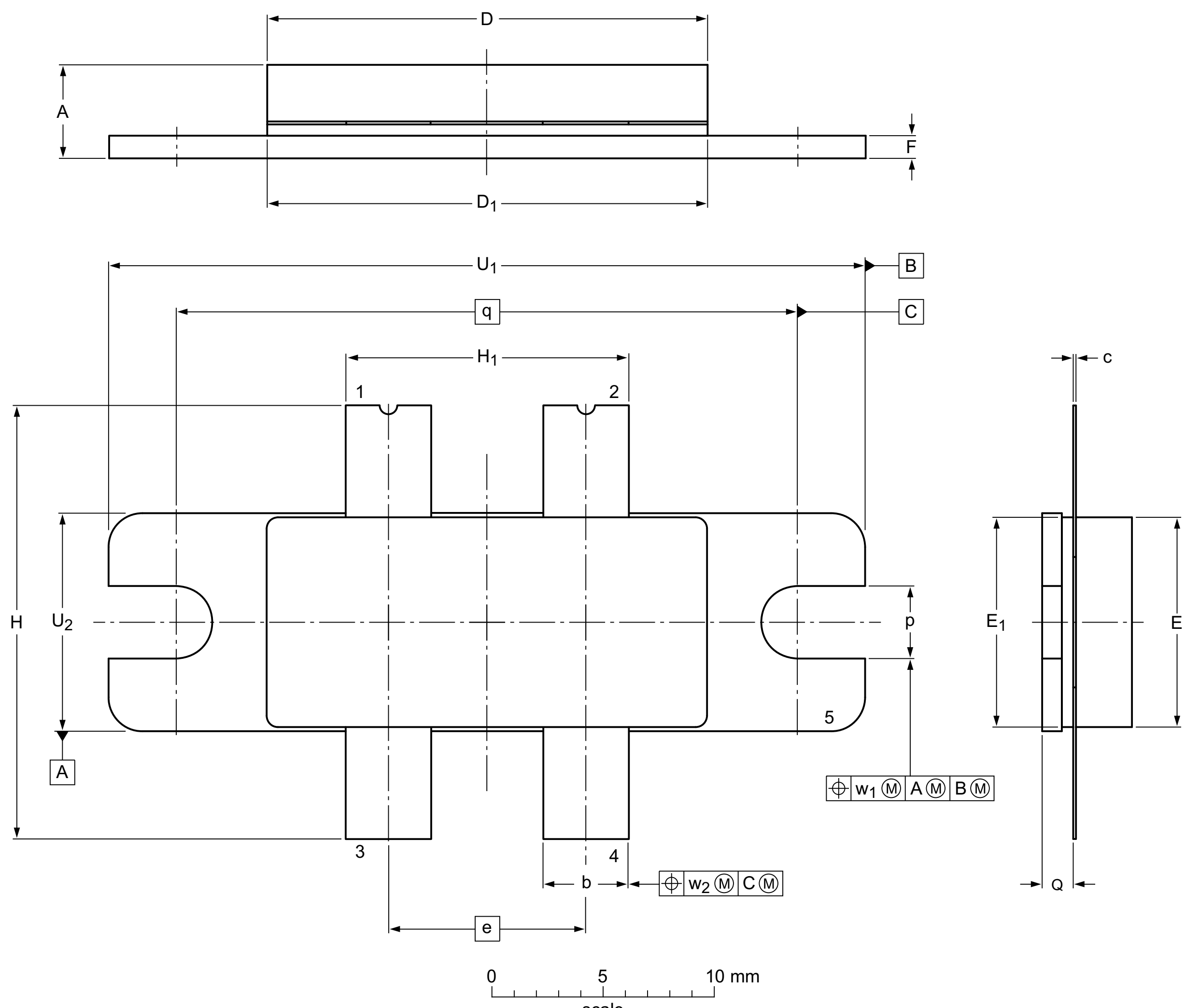
(5) V_{DS} = 40 V

(6) V_{DS} = 30 V

Fig 16. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT1121A**



Dimensions

Unit[1]		A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q[2]	q	U_1	U_2	w_1	w_2
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	3.38	1.70		34.16	9.91		
	nom						8.89								27.94			0.25	0.51
	min	3.45	3.68	0.10	19.61	19.66		9.27	9.27	0.89	18.92	12.57	3.12	1.45		33.91	9.65		
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.133	0.067		1.345	0.39		
	nom						0.35								1.1			0.01	0.02
	min	0.136	0.145	0.004	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.123	0.057		1.335	0.38		

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121A						~~09-10-12~~ 10-02-02

Fig 17. Package outline SOT1121A

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
FM	Frequency Modulation
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MRI	Magnetic Resonance Imaging
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ART450FE v.2	20240125	Product data sheet	-	ART450FE v.1
Modifications:	• Table 2 on page 2: changed name pin 2 to drain2 • Figure 1 on page 3: updated figure			
ART450FE v.1	20230714	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not guaranteed. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

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13. Contact information

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14. Contents

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