AR231062

ART800PE, 60 MHz

v1.0 — 23 May 2023

AMPLEON

Application Report

v1.0Document information	
Status	General Publication
Author(s)	Naser H.R Miveroud
Abstract	Measurement results of 57-63MHz amplifier with the ART800PE

1. Revision History

Table 1: Report revisions

Revision	Date	Description	Author
1.0	2023.05.23	Initial document	Naser H.R Miveroud

2. Contents

3. List of figures

4. List of tables

5. Description

5.1 General description

Ampleon has developed a family of reference designs based on ART2K0, Advanced Rugged Technology (ART) LDMOS power transistors. This family shares a unified board shape with the fixed positions of the mounting holes and cooling interface. The most common industry standards were followed to cover design for manufacturing (DFM), design for assembly (DFA), design for test (DFT), design for reliability (DFR) and design for service (DFS) requirements.

The reference design boards support transistors ART2K0 in both ceramic (ART2K0FES) and plastic (ART2K0PE) packages. However, these reference designs support applications of ART800 family as well, and by changing a few passive components the board is ready to deliver high performance with ART800 family of the transistors and hence, if needed, providing great flexibility for the end user to modify and adopt the system architecture/power with minimum possible effort and cost.

This report presents the measurement results of BPP0060E9X1600 with ART800PE LDMOS transistor. The amplifier was tuned to deliver high performance at 57-63MHz. The data relating to BPP0060E9X1600 and BPP0100E9X1600 reference designs are presented in AR211104 and AR211105 accordingly.

5.2 Theory of operation

The proposed amplifier has push-pull architecture. Input and output planar baluns are realized with a multilayer PCB. LDMOS transistor Q1 is soldered to an embedded copper heat spreader. The bottom side of the module is complete copper.

An applied signal goes through RF IN pin, input 0/180° splitter (balun) and LDMOS transistor to output pre-match, output 0/180° combiner (balun) and RF OUT pin.

The output balun is optimized as a compromise between compactness, insertion losses, ruggedness and thermal performance. Thermally conductive SMD bridges (Q-bridges) can be used to further improve power handling capability.

Gate voltage can be applied from any side of the board via VG1 or VG2 pin. Drain voltage can also be applied from any side of the board via VD1 or VD2 pin, but for best thermal performance in CW applications, it is recommended to use both pins in parallel.

T1 and T2 pins can be used to monitor the temperature of the module.

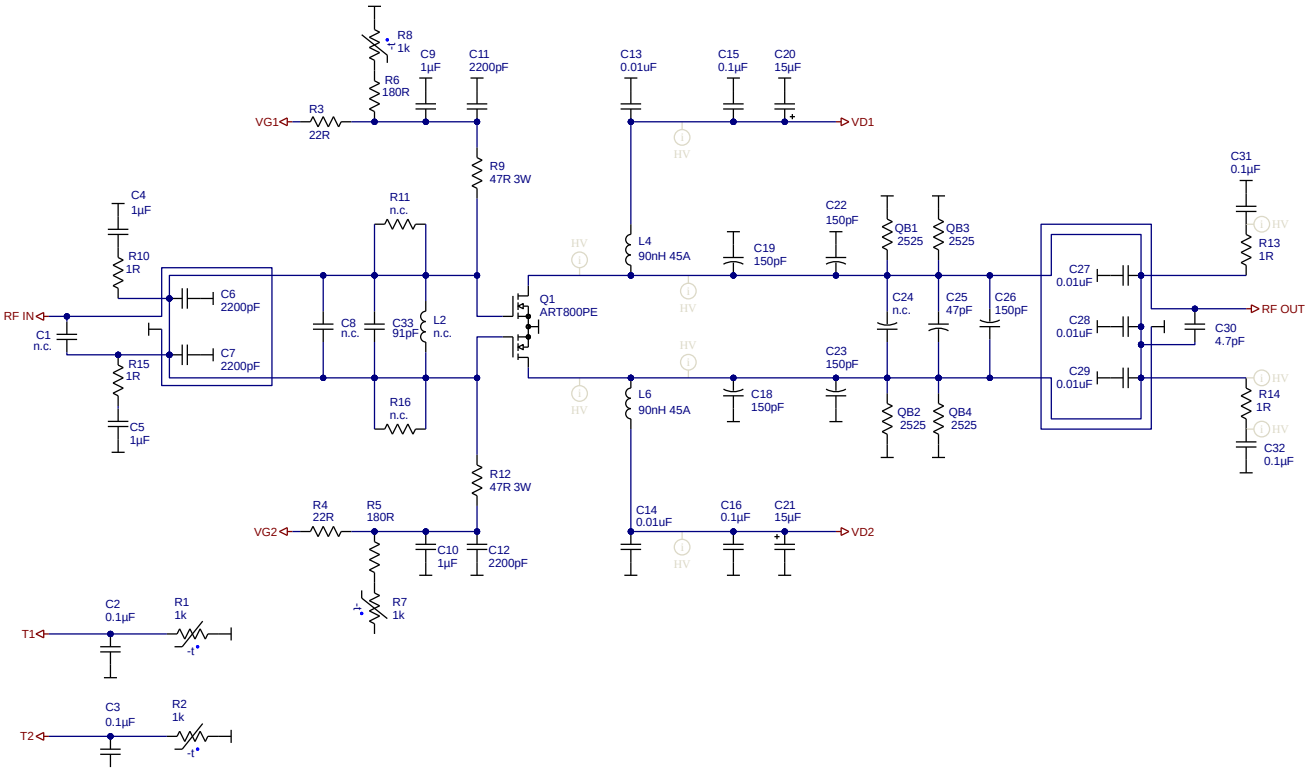

Figure 1 Schematic diagram of the amplifier

Figure 2 Demo board mounted on copper baseplate with water colling channel

5.3 Design recommendations

C4, C5, C31, C32, R10, R15, R13, R14 are for stability reasons. The values may need to be changed in each particular application.

Check ripple current and power dissipation in C15, C16, C20, C21, R13, R14 when operating in pulsed mode. Additional off-board electrolytic capacitors are mandatory.

Electrical characteristics

5.4 General characteristics

Test Conditions: CW pulsed operation: 100us pulse width 10% duty cycle; 50R load; IDq_total = 50mA; RF power measured after LPF; Tbaseplate = 25°C;

Table 2: Electrical characteristics

Symbol	Parameter	Unit	Min	Typ	Max
F	Frequency range of output matching	MHz	57	-	63
P_{1dB}	Output power at 1dB compression	W	-	680	-
η_D	Drain efficiency at 1dB compression	%	-	75	-
V_{DD}	Drain voltage	V	-	-	55
I_{DD_PEAK}	Peak current consumption	A	-	18	-
IRL	Input return loss	dB	-	10	-

5.5 Power sweep in CW pulsed operation

Test Conditions: CW pulsed operation: 100us pulse width 10% duty cycle; 50R load; Idq_total = 50mA; RF power measured after LPF; T_baseplate = 25°C;

Table 3: Output power and efficiency at different frequencies and compression levels

F, MHz	G_{MAX}, dB	P_{1dB}, W [1]	P_{2dB}, W	P_{3dB}, W	$\eta_{D\ P1dB}$, % [2]	$\eta_{D\ P2dB}$, %	$\eta_{D\ P3dB}$, %
57	29.2	704	760	785	75.7	78.0	78.8
60	29.1	680	734	770	75.6	77.6	78.6
63	28.9	683	745	770	76.5	79.1	80.2

[1] P_{1dB}, P_{2dB}, P_{3dB} - output power at 1, 2 and 3dB compression

[2] η_{D_P1dB}, η_{D_P2dB}, η_{D_P3dB} - drain efficiency at 1, 2 and 3dB compression

5.6 Power sweep in CW operation

Test Conditions: CW operation; 50R load; Idq_total = 50mA; RF power measured after LPF; T_baseplate = 25°C;

Table 4: Output power and efficiency at different frequencies and compression levels

F, MHz	G_{MAX}, dB	P_{1dB}, W [1]	P_{2dB}, W	P_{3dB}, W	η_{D_P1dB}, % [2]	η_{D_P2dB}, %	η_{D_P3dB}, %
57	28.6	655	711	740	74.0	76.5	77.5
60	28.5	635	690	725	74.2	76.4	77.6
63	28.4	635	700	730	75.1	78.0	79.3

[1] P_{1dB}, P_{2dB}, P_{3dB} - output power at 1, 2 and 3dB compression

[2] η_{D_P1dB}, η_{D_P2dB}, η_{D_P3dB} - drain efficiency at 1, 2 and 3dB compression

5.7 Sweep Graphs – CW Pulsed operation

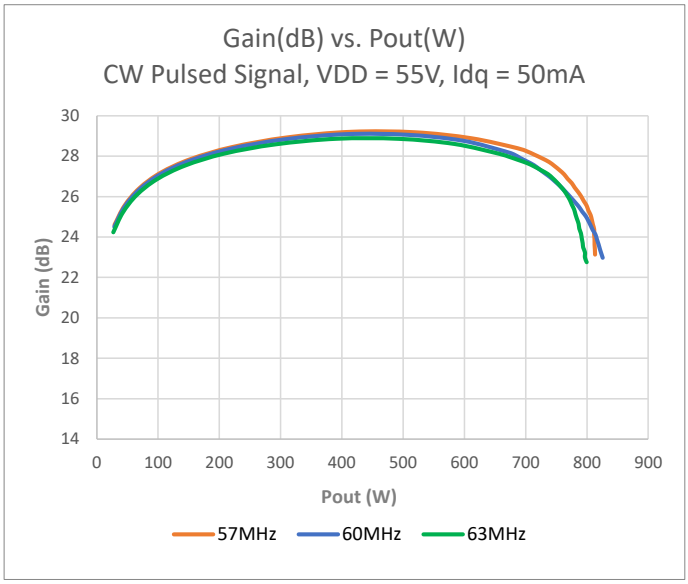

Figure 3 Gain(dB) over output power (W), CW pulsed signal, VDD = 55V, Idq = 50mA, PW = 100µsec, δ = 10%

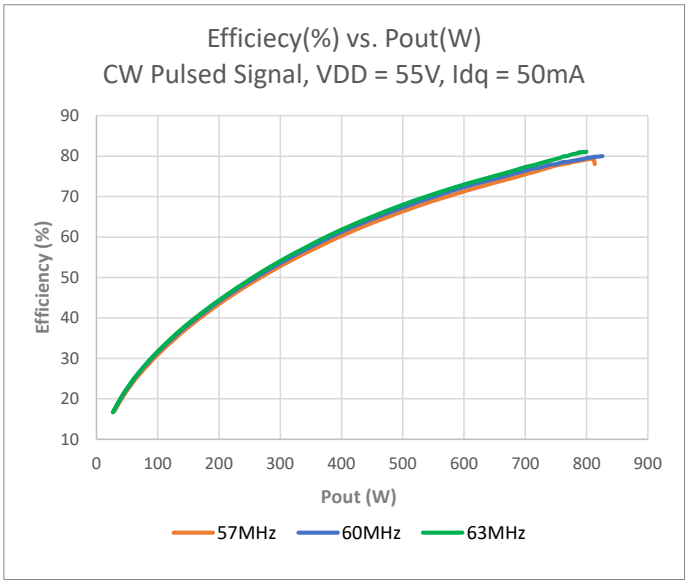

Figure 4 Efficiency (%) over output power (W), CW pulsed signal, VDD = 55V, Idq = 50mA, PW = 100µsec, δ = 10%

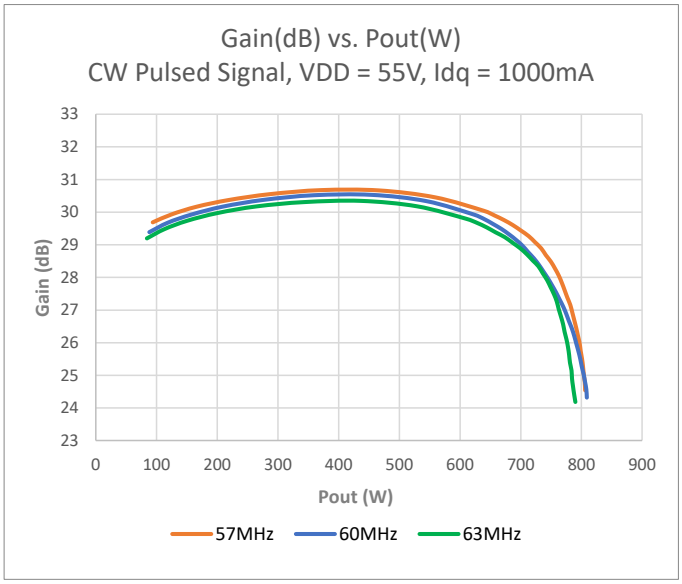

Figure 5 Gain(dB) over output power (W), CW pulsed signal, VDD = 55V, Idq = 1000mA, PW = 100µsec, δ = 10%

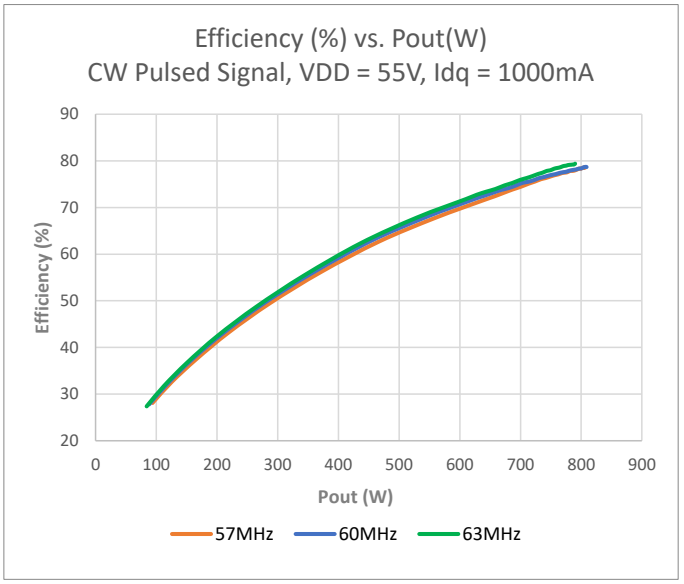

Figure 6 Efficiency (%) over output power (W), CW pulsed signal, VDD = 55V, Idq = 1000mA, PW = 100µsec, δ = 10%

5.8 Sweep Graphs – CW operation

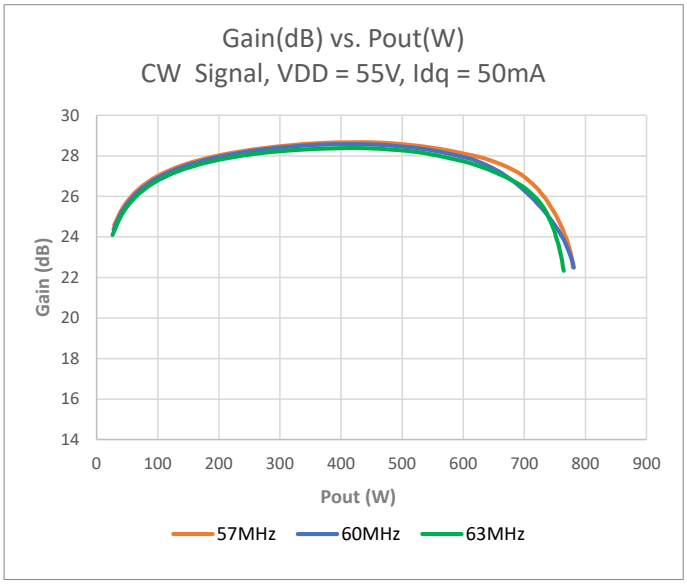

Figure 7 Gain(dB) over output power (W), CW signal, VDD = 55V, Idq = 50mA

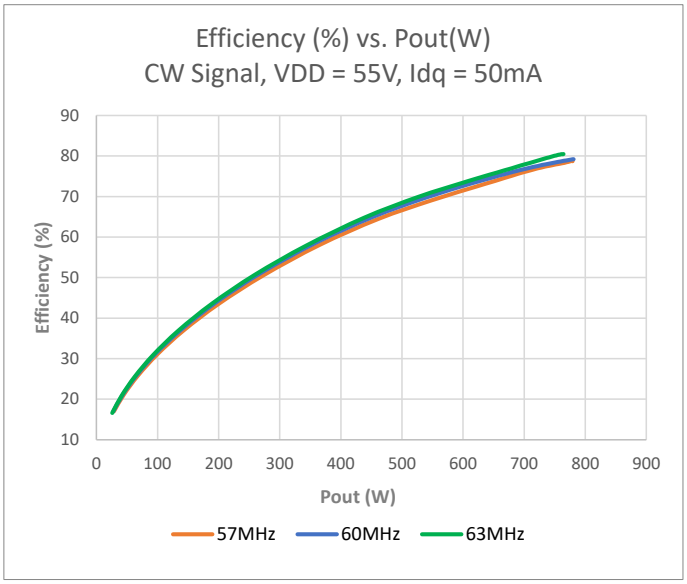

Figure 8 Efficiency (%) over output power (W), CW signal, VDD = 55V, Idq = 50mA

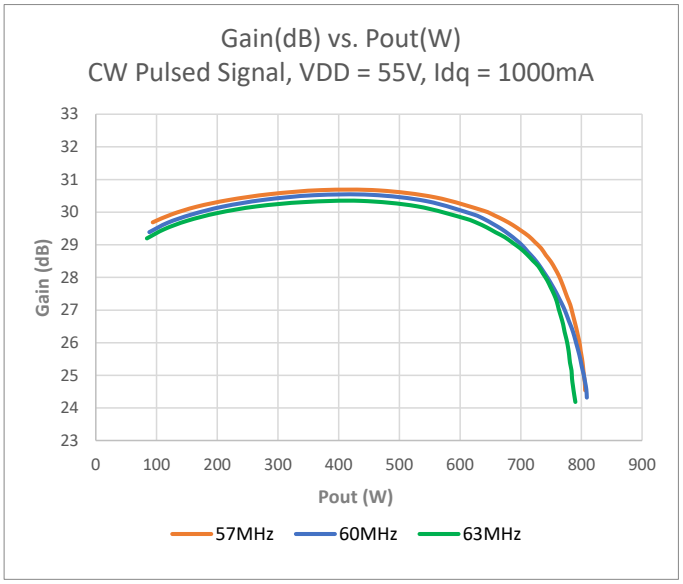

Figure 9 Gain(dB) over output power (W), CW signal, VDD = 55V, Idq = 1000mA

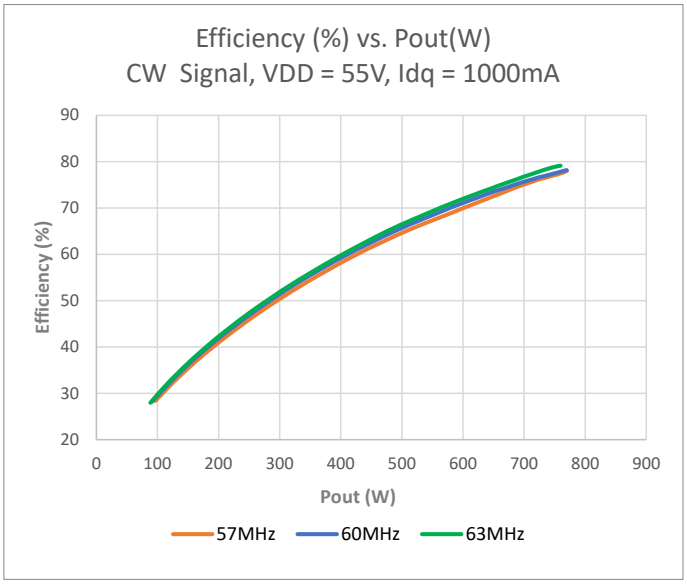

Figure 10 Efficiency (%) over output power (W), CW signal, VDD = 55V, Idq = 1000mA

6. Hardware

6.1 Board specifications

Table 5: Board specifications

Parameter	Value
Manufacturer	Rogers
Type	Multilayer RO4835 + RO4450
Dk	3.48 @ 10GHz
Df	0.0037 @ 10GHz
Total PCB thickness	4.9mm
Layers	10
Board specifics	Transistor Q1 is mounted on a U-shaped copper insert (coin)
Board dimensions	152 x 60mm

6.2 Demo markings

Table 6: Device specifics

Parameter	Value
Manufacturer	Ampleon
Device	ART800PE
PCB marking	BPP0120E9X1600

7. Thermal characteristics

Figure 8 illustrates the IR image of the demo after reaching thermal equilibrium with water cooling.

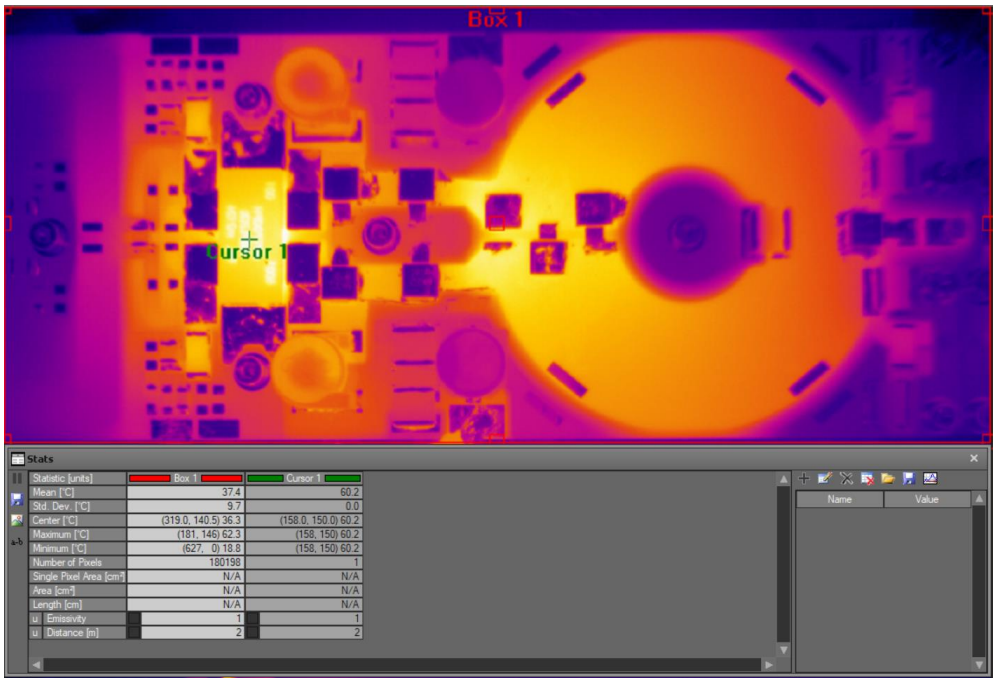

Figure 11 IR image of the demo operating at P3dB, V_{DD} = 55V, water cooling, Twater = 25°C

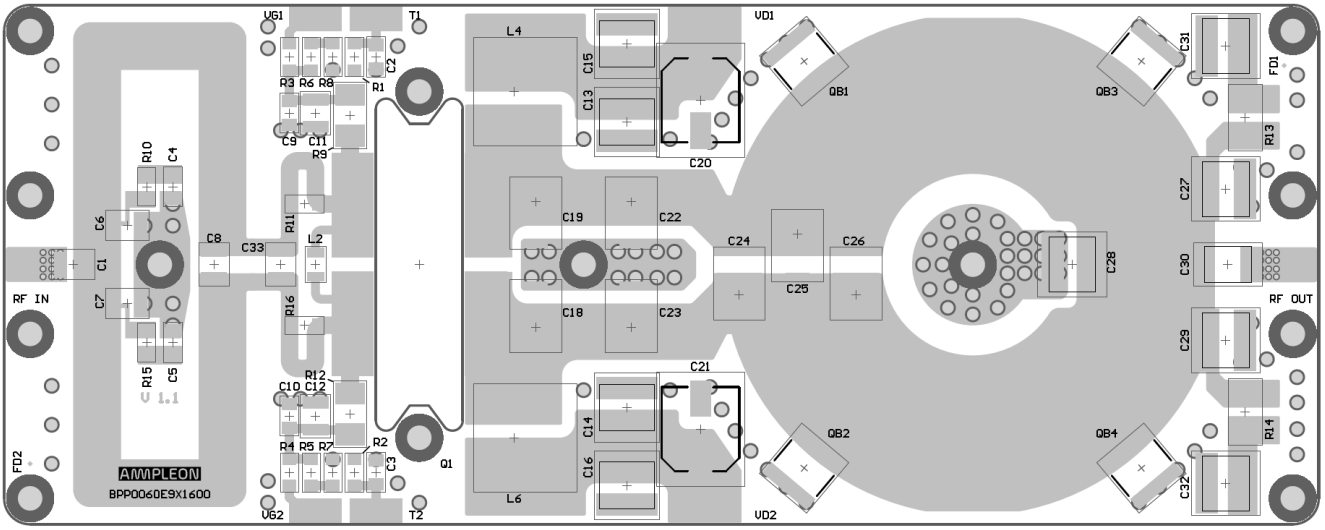

Figure 12 PCB and component layout

7.1 Bill of materials

Table 7: Bill of Materials

Designator	Group	Value	Tolerance	Name	Manufacturer	Quantity
C1, C8	Capacitor	n.c.				3
C33	Capacitor	91pF	±5%	800B910JT500XT1K	ATC	1
C2, C3	Capacitor	0.1µF	±5%	CL31C104JAHNNWE	Samsung	2
C4, C5, C9, C10	Capacitor	1µF	±10%	VJ1206Y105KXXTW1BC	Vishay	4
C6, C7, C11, C12	Capacitor	2200pF	±2%	111121000222GQTAF9LM	Knowles Syfer	4
C13, C14, C27, C28, C29	Capacitor	0.01uF	±5%	222522000103JQTAF9LM	Knowles Syfer	5
C15, C16, C31, C32	Capacitor	0.1µF	±10%	VJ2225Y104KXGAT	Vishay	4
C17	Capacitor	10pF	±5%	MIN02-002CC100J-F	Cornell Dubilier	1
C18, C19	Capacitor	150pF	±5%	MIN02-002EC151J-F	Cornell Dubilier	2
C20, C21	Capacitor	15µF	±20%	100SXV15M	Panasonic	2
C22, C23	Capacitor	150pF	±5%	MIN02-002EC151J-F	Cornell Dubilier	4
C24	Capacitor	n.c.				1
C25	Capacitor	47pF	±5%	MIN02-002EC470J-F	Cornell Dubilier	1
C26	Capacitor	150pF	±5%	MIN02-002EC151J-F	Cornell Dubilier	1
C30	Capacitor	4.7pF	±5%	MIN02-002EC4R7J-F	Cornell Dubilier	1
C125, C126	Capacitor	n.c.			Cornell Dubilier	2
L2	Inductor	330nH	±5%	1206CS-331XJE	Coilcraft	1
L4, L6	Inductor	90nH 45A	±10%	1212VS-90NME_	Coilcraft	2
Q1	Transistor			ART800PE	Ampleon	1
QB1, QB2, QB3, QB4	Q Bridge	2525		QB2525A60WSTB	ATC	4

R1, R2, R7, R8	NTC Thermistor	1k	±5%	B57621C5102J062	TDK	4
R3, R4	Resistor	22R	±1%	CRGP1206F22R	TE Connectivity	2
R5, R6	Resistor	180R	±1%	CRGCQ1206F180R	TE Connectivity	2
R9, R12	Resistor	47R 3W	±1%	352247RFT	TE Connectivity	2
R10, R15	Resistor	1R	±5%	CRGS1206J1R0	TE Connectivity	2
R11, R16	Resistor	n.c.				2
R13, R14	Resistor	1R	±5%	35221R0JT	TE Connectivity	2

7. Abbreviations

Table 8: Abbreviations

Parameter	Description
F	Frequency
CW	Continuous Wave
Gmax	Maximum Gain
P1dB	1 dB Compression Point of the Gain
V_{DD}	Drain Voltage
VGS	Gate Voltage
η_{DRAIN}	Drain Efficiency
VSWR	Voltage Standing Wave Ratio
δ	Duty Cycle
t_p	Pulse Width
RF	Radio Frequency
P_L	Power Delivered to 50Ω Load at RF OUT Connector
S21	Small Signal Gain (S-parameter measurement in 50Ω System)
Pin	Input Power to the Amplifier at RF IN Connector
Pout	Output Power of Amplifier at RF OUT Connector
LPF	Low Pass Filter

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