AR211147

ART150PEG, 6.78MHz

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AMPLEON

Application Report

Document information	
Status	General Publication
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Abstract	Measurement results of a 6.78MHz Class EF2 Generator with the ART150PEG

1. Revision History

Table 1: Report revisions

Revision	Date	Description	Author
1.0	2021.11.08	Initial document	Yevhen Tymofieiev

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5. Description

5.1 General description

This report presents the measurement results of the Class EF2 Generator demo AR211147. The device used is ART150PEG, Advanced Rugged Technology (ART) LDMOS power transistor. The demo is operating at 6.78MHz.

Class EF2 (Class E with shorted 2nd harmonic) brings the best power utilization ratio in combination with high efficiency, low cost and exceptional harmonic suppression.

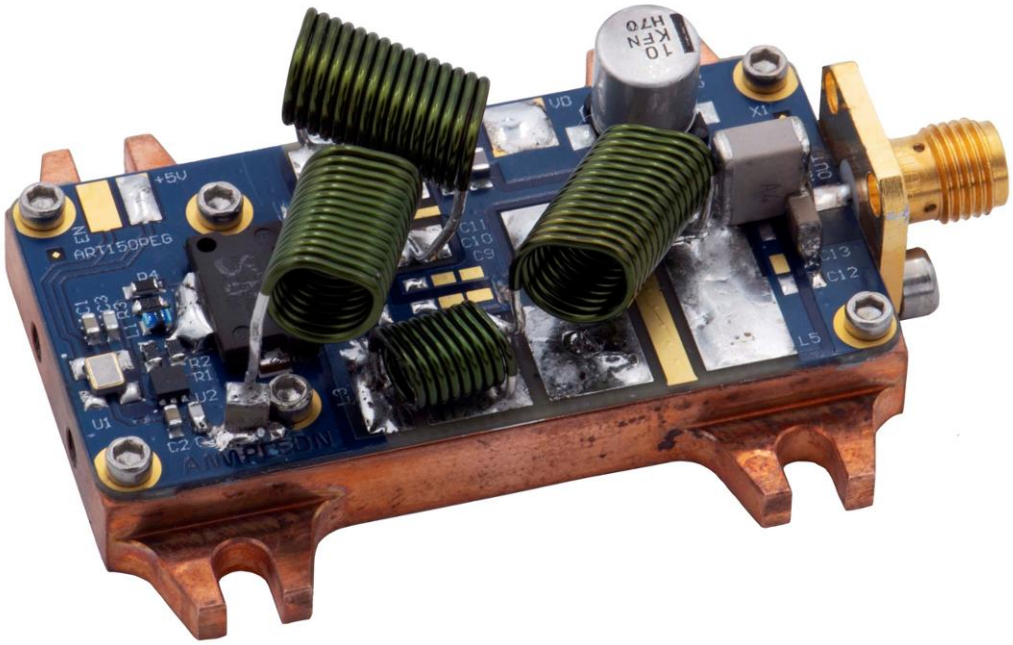

Figure 1 Side view

5.2 Theory of operation

The demo lineup consists of a 6.78MHz clock U1, gate driver U2, pre-distortion network, LDMOS transistor Q1 and the output matching (*Figure 1*).

6.78MHz clock U1 is the crystal oscillator with digital CMOS output. It provides the signal to Schmitt trigger at the non-inverting input of the gate driver U2. The output stage of the driver U2 is connected to the gate of Q1 via current limiting resistor R1 and pre-distortion network (L1, C6). The pre-distortion network is boosting the rise and fall times of the pulse on the capacitive gate of Q1 and therefore reduces the losses in transistor Q1 during the switching between low (0V) and high (4-5V) states. The output matching network provides a proper transformation ratio and helps to reduce the level of harmonics.

Output RF power at the connector X1 can be regulated with variable V_{DD} coming from the switching mode power supply (SMPS) in the range of 5 to 150W.

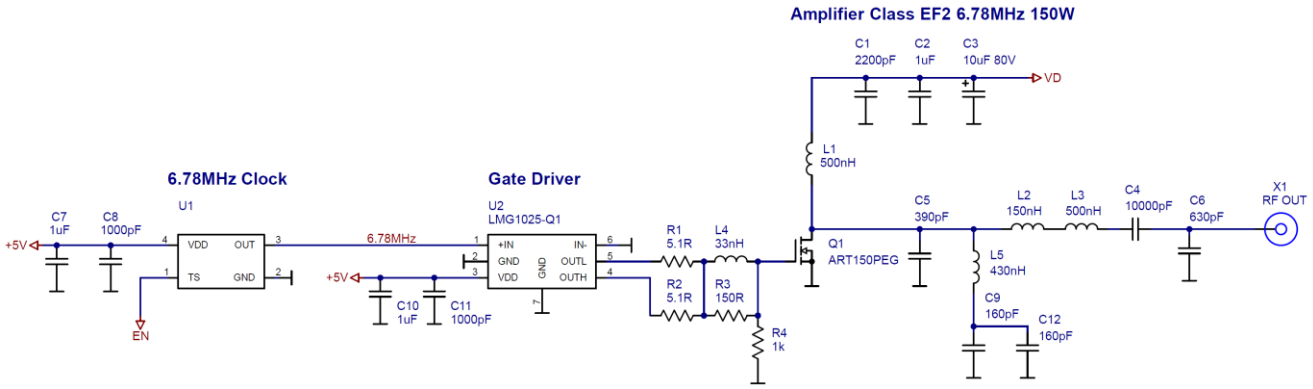

Figure 2 Schematic

5.3 Design recommendations

The frequency of operation is set by the clock U1 and can be adjusted by the IC supplier on request. The output matching supports the 6.5-7MHz frequency range.

Demo works in high-efficiency mode Class EF2. For long-term reliability at high output power or in certain mismatch conditions check peak voltages on the drain lead of Q1.

The nominal output power is 150W at 50 Ohm load. For long-term operation at higher output power or in certain mismatch conditions check the junction temperature and MTF in “RF Power Lifetime Calculator” at https://www.ampleon.com/.

Because of the high impedance of the interface between U1 and U2, the line on PCB is kept as short as possible. Local SMD shield covering U1, U2 and all the peripheral components might help to reduce coupling from the output matching.

The pre-distortion network might create positive and negative voltage spikes outside of the safe operating region of the gate driver U2. It is important to dump those spikes using R1, R2 and R3.

The gate driver U2 could be driven directly from the microcontroller to enable output power adjustment via pulse-width modulation (PWM).

It is possible to run the demo in pulsed mode by applying the modulation/enable signal to pin1 of U1. When operating in this mode, it might be necessary to check the ripple current in capacitor C3).

6. Electrical characteristics

6.1 General characteristics

Table 2: Electrical characteristics

CW operation; 50R load; RF power measured after LPF; Tbaseplate = 40°C

Symbol	Parameter	Unit	Min	Typ	Max
F	Frequency range of output matching[1]	MHz	6.5	6.78	7
V_{DD}	Drain voltage of LDMOS section	V	10	-	65
I_{DD}	Current consumption of LDMOS section	A	-	3.2	-
V_{DRIVER}	Voltage supply of driver section	V	4	4.7	5
P_{OUT}	Output power[2]	W	-	150	-
η_{DRAIN}	Drain efficiency	%	-	86.5	-
η_{LINEUP}	Lineup efficiency	%	-	86.3	-
P_{DISS}	Dissipated power	W	-	25	-
H_2	Level of 2nd harmonic	dBc	-	-38	-
H_3	Level of 3rd Harmonic	dBc	-	-25	-

[1] The exact frequency of operation is set by the clock U1

[2] Typical output power of 150W is achieved with V_{DD} = 63V

6.2 Power sweep

Table 3: Output power and efficiency as a function of drain voltage

F = 6.78MHz; CW operation; 50R load; V_{DRIVER} = 4.7V ; RF power measured after LPF; Tbaseplate = 40°C

V_{DD}, V	I_{DD}, A	P_{OUT}, W	η_{DRAIN}, %	η_{LINEUP}, %	P_{DISS}[2], W
10	0.5	3.88	82.4	78.2	0.8
20	0.9	15.5	84.3	83.2	2.9
30	1.4	35.4	86.4	85.9	5.6
40	1.8	62.4	86.4	86.1	9.8
50	2.2	97.1	86.7	86.5	14.9
60	2.7	138	86.5	86.3	21.6
65[1]	2.9	161	86.4	86.3	25.2

[1] *Long-term operation at V_{DD} > 63V is not recommended*

[2] *Power dissipated in transistor Q1 and output matching*

Board specifications

Table 4: Board specifications

Parameter	Value
Manufacturer	EMC
Type	EM-827BI (Lead free FR4)
Dk	4.8 @ 1MHz 4.2 @ 1GHz
Df	0.018 @ 1MHz 0.019 @ 1GHz
Laminate thickness	0.5mm / 1 oz.
Layers	2, top/bottom. Bottom all copper
Board specifics	Transistor Q1 is mounted on an I-shaped copper insert (coin)
Board dimensions	50 x 25mm

6.3 Demo markings

Table 5: Device specifics

Parameter	Value
Manufacturer	Ampleon
Device	ART150PEG
PCB marking	ART150PEG GEN

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