AR211125

ART150PEG, 40MHz

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AMPLEON

Application Report

Document information	
Status	General Publication
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Abstract	Measurement results of a 40MHz generator with the ART150PEG

1. Revision History

Table 1: Report revisions

Revision	Date	Description	Author
1.0	2021.09.02	Initial document	Yevhen Tymofieiev

2. Contents

3. List of figures

4. List of tables

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5. Description

5.1 General description

This report presents the measurement results of the generator demo AR211125. The device used is ART150PEG, Advanced Rugged Technology (ART) LDMOS power transistor. The presented demo is operating at 40MHz.

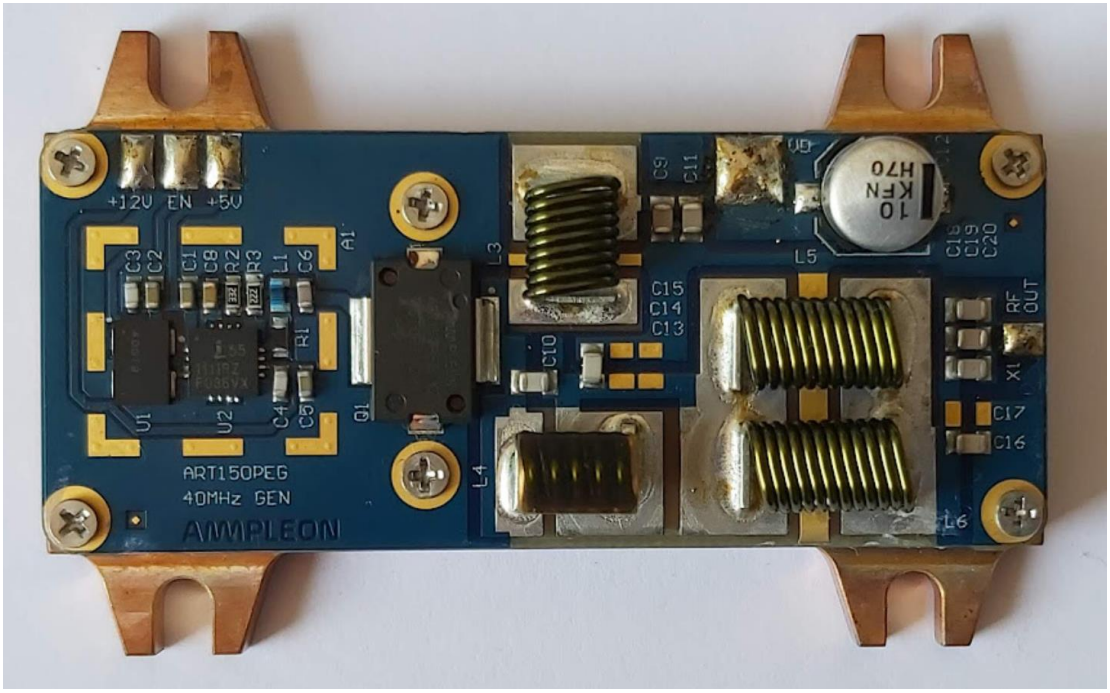

Figure 1 Demo front view

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5.2 Theory of operation

The demo lineup consists of a 40MHz clock U1, gate driver U2, pre-distortion network, LDMOS transistor Q1 and the output matching (*Figure 1*).

40MHz clock U1 is the crystal oscillator with digital CMOS output. It provides the signal to Schmitt trigger at the non-inverting input of the gate driver U2. The output stage of the driver U2 is connected to the gate of Q1 via current limiting resistor R1 and pre-distortion network (L1, C6). The pre-distortion network is boosting the rise and fall times of the pulse on the capacitive gate of Q1 and therefore reduces the losses in transistor Q1 during the switching between low (0V) and high (7-11V) states. The output matching network provides a proper transformation ratio and helps to reduce the level of harmonics.

Output RF power at the connector X1 can be regulated with variable V_{DD} coming from the switching mode power supply (SMPS) in the range of 5 to 150W.

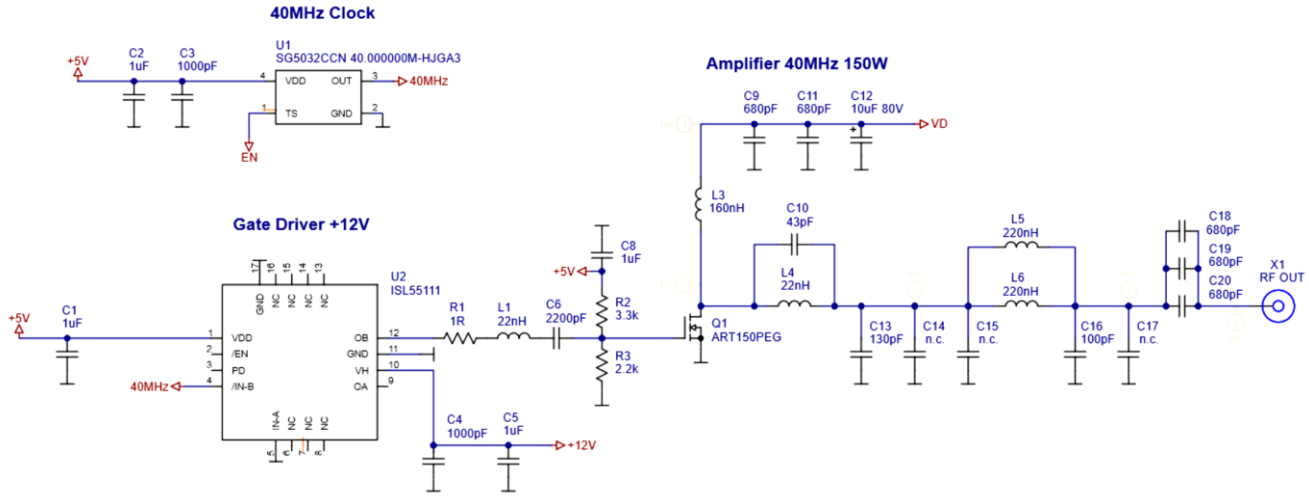

Figure 2 Schematic

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5.3 Design recommendations

The frequency of operation is set by the clock U1 and can be adjusted by the IC supplier on request. The output matching supports the 40-42MHz frequency range.

The nominal output power is 150W at 50 Ohm load. For long-term operation at higher output power or in certain mismatch conditions check the junction temperature and MTF in “RF Power Lifetime Calculator” at https://www.ampleon.com/.

Demo works in high-efficiency mode close to class E. Long-term operation with V_{DD} > 60V is not recommended because of possible voltage overshoot at the drain of Q1.

Because of the high impedance of the interface between U1 and U2, the line on PCB is kept as short as possible. Local SMD shield covering U1, U2 and all the peripheral components might help to reduce coupling from the output matching.

The pre-distortion network might create positive and negative voltage spikes outside of the safe operating region of the gate driver U2. It is important to dump those spikes using R1.

The gate driver U2 could be driven directly from the microcontroller to enable output power adjustment via pulse-width modulation (PWM).

It is possible to run the demo in pulsed mode by applying the modulation/enable signal to pin1 of U1. When operating in this mode, it might be necessary to check the ripple current in capacitor C12.

C10, C13, C16 can be replaced with 1111 capacitors for a slight improvement in electrical characteristics. Several 0805 capacitors can be used in parallel in order to reduce equivalent series resistance (ESR).

As explained in chapter 7, two inductors 2222SQ-221GE (L4, L5) connected in parallel can be replaced with one inductor 1010VS-111ME.

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6. Electrical characteristics

6.1 General characteristics

Table 2: Electrical characteristics

CW operation; 50R load; RF power measured after LPF; Tbaseplate = 40°C

Symbol	Parameter	Unit	Min	Typ	Max
F	Frequency range of output matching[1]	MHz	40	-	42
V_{DD}	Drain voltage of LDMOS section	V	10	-	60
I_{DD}	Current consumption of LDMOS section	A	-	3.2	-
V_{DRIVER}	Voltage supply of driver section	V	5	9	12
I_{DRIVER}	Current consumption of driver section	mA	-	80	-
P_{OUT}	Output power[2]	W	-	150	-
η_{DRAIN}	Drain efficiency[3]	%	-	86.3	-
η_{LINEUP}	Lineup efficiency[3]	%	-	86.0	-
P_{DISS}	Dissipated power	W	-	25	-
H_2	Level of 2nd harmonic	dBc	-	-18	-
H_3	Level of 3rd Harmonic	dBc	-	-35	-

[1] The exact frequency of operation is set by the clock U1

[2] Typical output power of 150W is achieved with V_{DD} = 56V

[3] Measured at 40MHz

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6.2 Power sweep

Table 3: Output power and efficiency as a function of drain voltage

F = 40MHz; CW operation; 50R load; V_{DRIVER} = 9V ; RF power measured after LPF; Tbaseplate = 40°C

V_{DD}, V	I_{DD}, A	P_{OUT}, W	η_{DRAIN}, %	η_{LINEUP}, %	P_{DISS}[2], W
10	0.689	5.2	75.5	68.5	1.7
15	0.973	11.6	79.5	75.8	3.0
20	1.25	20.4	81.6	79.4	4.6
25	1.52	31.6	83.2	81.6	6.4
30	1.78	45	84.3	83.2	8.4
35	2.03	60.8	85.6	84.7	10.3
40	2.3	79	85.9	85.2	13.0
45	2.55	99.1	86.4	85.8	15.7
50	2.8	121	86.4	86.0	19.0
55	3.05	145	86.4	86.1	22.8
60	3.29	170	86.1	85.8	27.4
65[1]	3.5	191	85.3	85.0	33.0

[1] *Long-term operation at V_{DD} > 60V is not recommended*

[2] *Power dissipated in transistor Q1 and output matching*

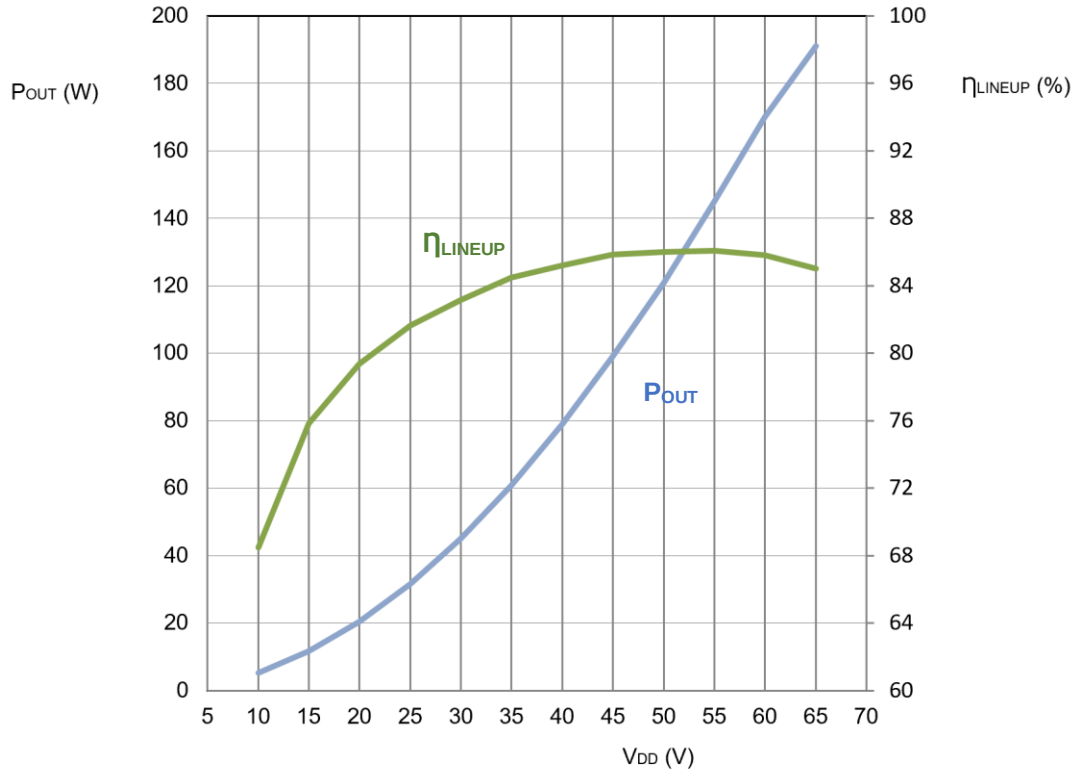

Figure 3 Output power and lineup efficiency as a function of drain voltage

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6.3 Optimal voltage supply of driver section

Driver IC ISL55111 (U2) has separate supply pins for the logic section and half-bridge drivers. The best demo lineup efficiency is achieved with a 9V supply at the half-bridge driver section of U2.

Table 4: Output power and efficiency as a function of voltage supply of driver section

F = 40MHz; CW operation; 50R load; RF power measured after LPF; $T_{BASEPLATE}$ = 40°C

V_{DD}, V	V_{DRIVER}, V	I_{DRIVER}, mA	P_{OUT}, W	η_{DRAIN}, %	η_{LINEUP}, %
50	5	40	104	80.0	79.9
50	7	58	120	86.0	85.8
50	9	78	121	86.4	86.0
50	11	94	121	86.4	85.8
60	5	40	113	69.5	69.4
60	7	58	167	85.4	85.2
60	9	78	170	86.1	85.8
60	11	94	170	86.1	85.7

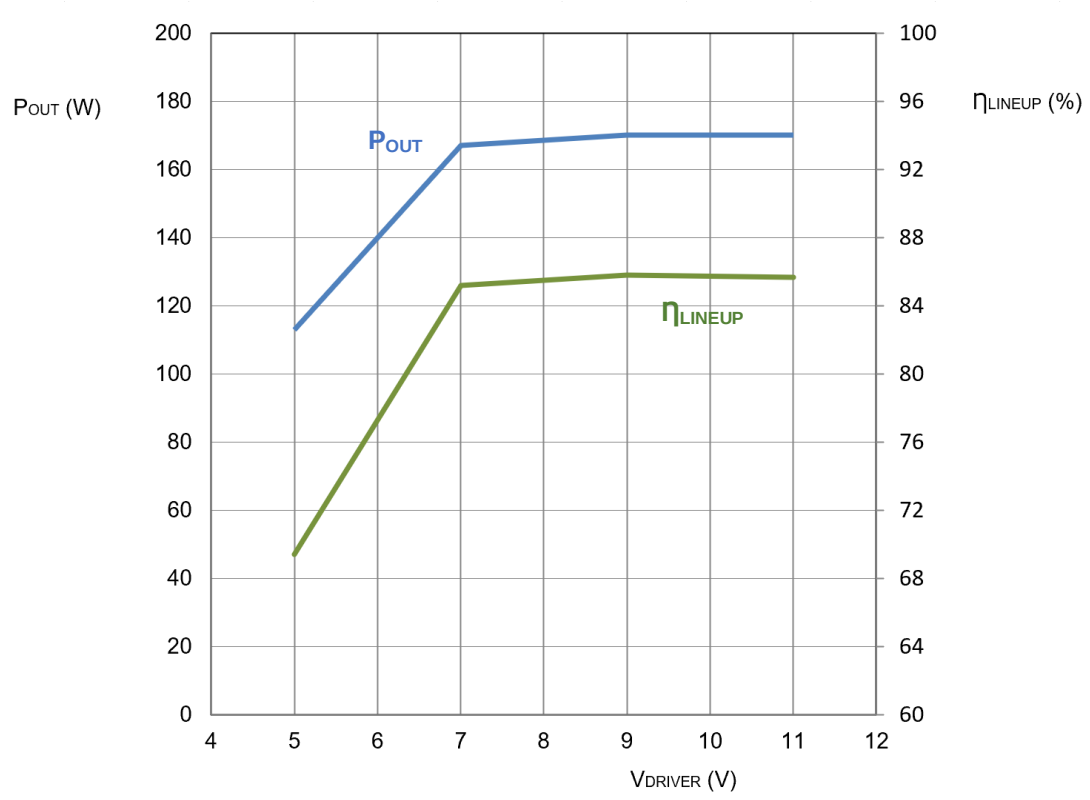

Figure 4 Output power and lineup efficiency as a function of voltage supply of driver section; F = 40MHz; V_{DD} = 60V

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7. Thermal characteristics

The board has been measured during RF operation with an IR camera to detect hotspots.

Test conditions:

F = 40MHz; V_{DD} = 56V; V_{DRIVER} = 9V;

P_{OUT} = 150W CW, 50R load, RF power measured after LPF;

$T_{BASEPLATE}$ = 40°C

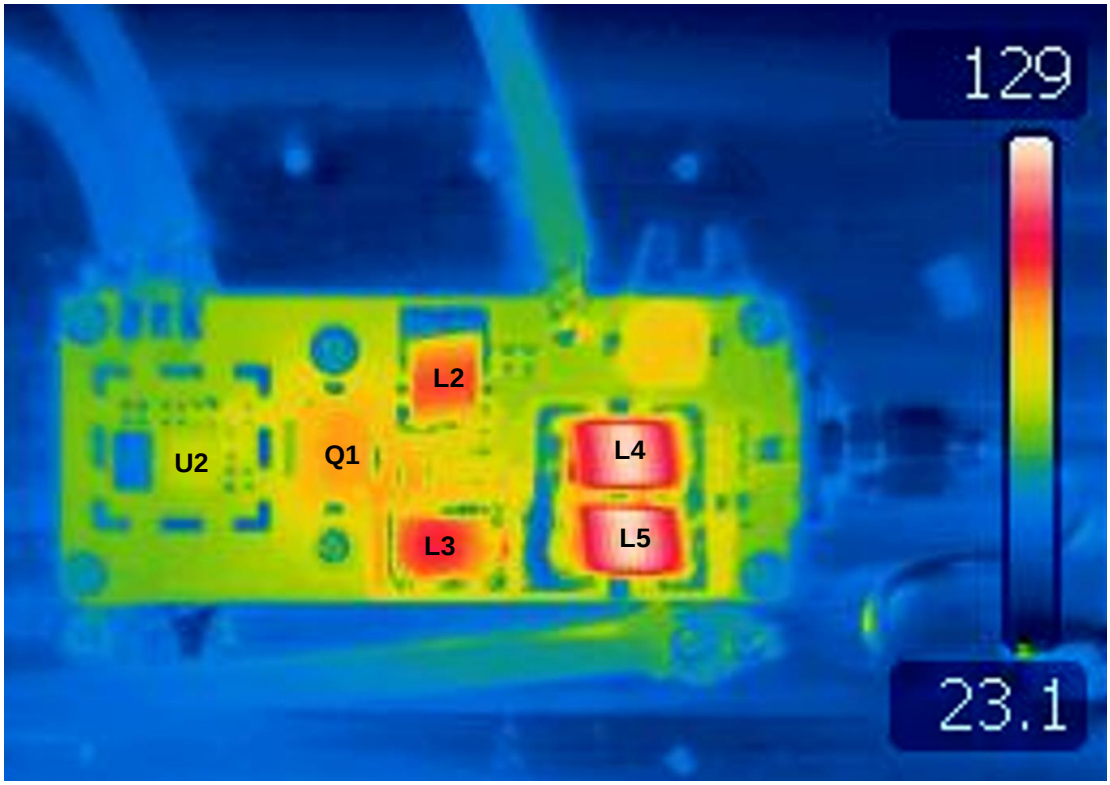

Figure 5 IR picture

The board has two hotspots – L4, L5. Both get a temperature rise of 90°C.

Those two 220nH 5A inductors 2222SQ-221GE connected in parallel were used in the demo design because of the tight ±2% tolerance. It is possible to replace L4 and L5 just with one 111nH 22A inductor 1010VS-111ME. It is up to the customer to decide if ±20% tolerance of 1010VS-111ME can provide sufficient yield in mass production.

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8. Hardware

8.1 Bill of materials

Table 5: Bill of Materials

Designator	Group	Value	Tolerance	Name	Manufacturer	Quantity
A1	Shield			2118706-2	TE	1
C1, C2, C5, C8	Capacitor	1uF	±10%	0603YC105KAT2A	AVX	4
C3, C4	Capacitor	1000pF	±5%	06035A102JAT2A	AVX	2
C6	Capacitor	2200pF	±5%	06035A222JAT2A	AVX	1
C9, C11, C18, C19, C20	Capacitor	680pF	±5%	VJ0805D681KXBAJ	Vishay	5
C10	Capacitor	43pF	±5%[1]	08051U430JAT2A	AVX	1
C12	Capacitor	10uF 80V	±20%	EEE-FN1K100XL	Panasonic	1
C13	Capacitor	130pF	±5%[1]	08052U131JAT2A	AVX	1
C16	Capacitor	100pF	±5%[1]	08052U101JAT2A	AVX	1
L1	Inductor	22nH	±5%	LQW18AN22NJ00D	Murata	1
L3	Inductor	160nH	±2%[1]	2222SQ-161GE	Coilcraft	1
L4	Inductor	22nH	±5%[1]	WA3096-AL	Coilcraft	1
L5, L6	Inductor	220nH	±2%[1]	2222SQ-221GE	Coilcraft	2
Q1	Transistor			ART150PEG	Ampleon	1
R1	Resistor	1R	±1%	ERJ-PA3J1R0V	Panasonic	1
R2	Resistor	3.3k	±0.5%	ERA-3AED332V	Panasonic	1
R3	Resistor	2.2k	±0.5%	ERA-3AED222V	Panasonic	1
U1	IC	40MHz		SG5032CCN 40.000000M-HJGA3	Epson	1
U2	IC			ISL55111	Renesas	1

[1] Tolerance is critical for the assembly yield. Use 1% or 2% tolerance for the best results.

[2] Could be replaced with 1111 capacitors for a slight improvement in electrical characteristics. Several 0805 capacitors can be used in parallel (C14, C15, C17) in order to reduce equivalent series resistance.

[3] Square wave oscillator. When changing the frequency, adjust C10, C13, C16, L3-L5

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8.2 Component mapping

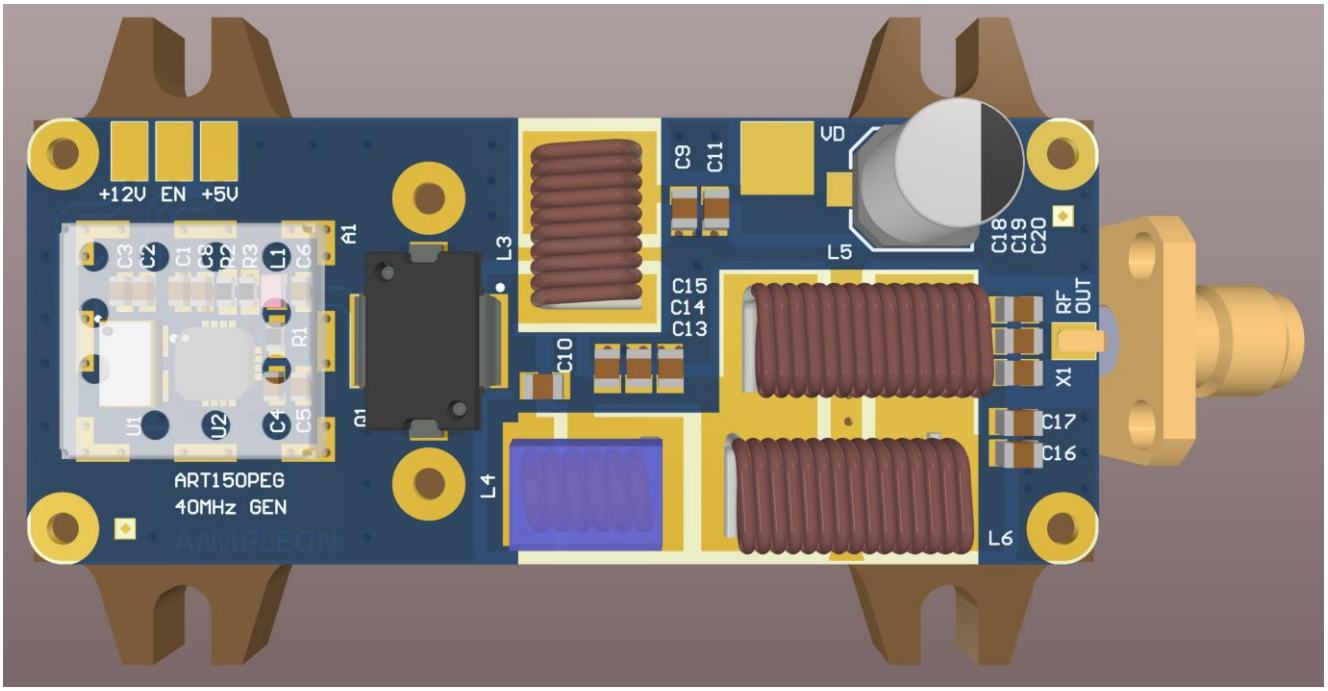

Figure 6 Component mapping

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Board specifications

Table 6: Board specifications

Parameter	Value
Manufacturer	EMC
Type	EM-827BI (Lead free FR4)
Dk	4.8 @ 1MHz 4.2 @ 1GHz
Df	0.018 @ 1MHz 0.019 @ 1GHz
Laminate thickness	0.5mm / 1 oz.
Layers	2, top/bottom. Bottom all copper
Board specifics	Transistor Q1 is mounted on an I-shaped copper insert (coin)
Board dimensions	60 x 25mm

8.3 Demo markings

Table 7: Device specifics

Parameter	Value
Manufacturer	Ampleon
Device	ART150PEG
PCB marking	ART150PEG 40MHz GEN

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