AR211103

ART150PEG, 40MHz

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AMPLEON

Application Report

Document information	
Status	General Publication
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Abstract	Measurement results of a class E generator design for the 40MHz band with the ART150PEG

1. Revision History

Table 1: Report revisions

Revision	Date	Description	Author
1.0	2021.04.02	Initial document	Yevhen Tymofieiev

2. Contents

3. List of figures

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5. Description

5.1 General description

This report presents the measurement results of the Class E generator demo AR211065. The device used is ART150PEG, Advanced Rugged Technology (ART) LDMOS power transistor. The presented demo is operating at 40MHz.

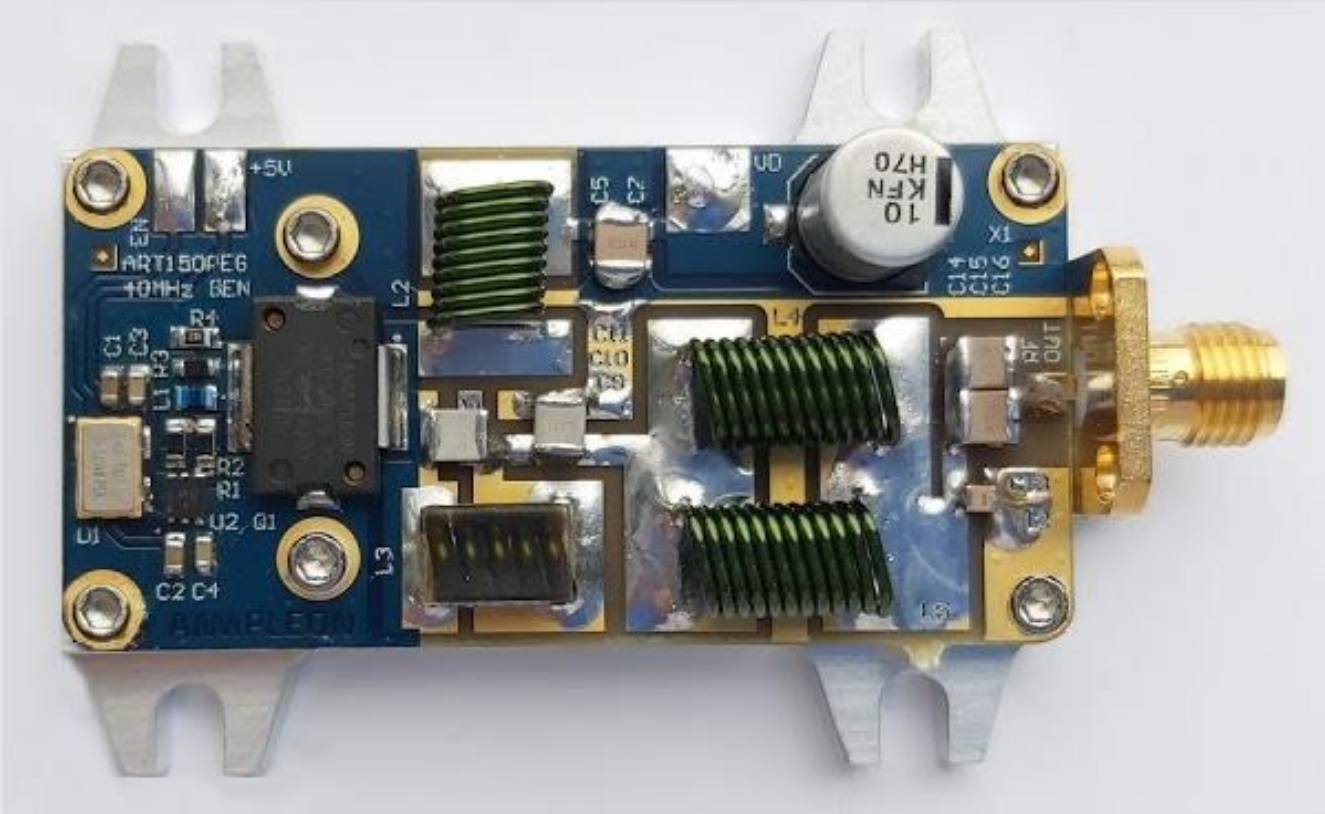

Figure 1 Demo front view

5.2 Theory of operation

The demo lineup consists of a 40MHz clock U1, gate driver U2, pre-distortion network, LDMOS transistor Q1 and the output matching (*Figure 1*).

40MHz clock U1 is the crystal oscillator with digital CMOS output. It provides the signal to Schmitt trigger at the non-inverting input of the gate driver U2. The output stage of the driver U2 is connected to the gate of Q1 via current limiting resistors (R1, R2) and pre-distortion network (L1, R3). The pre-distortion network is boosting the rise and fall times of the pulse on the capacitive gate of Q1 and therefore reduces the losses in transistor Q1 during the switching between 0V and 5V. The output matching network provides a proper transformation ratio and helps to reduce the level of harmonics.

Output RF power at the connector X1 can be regulated with variable V_{DD} coming from the switching mode power supply (SMPS) in the range of 5 to 135W.

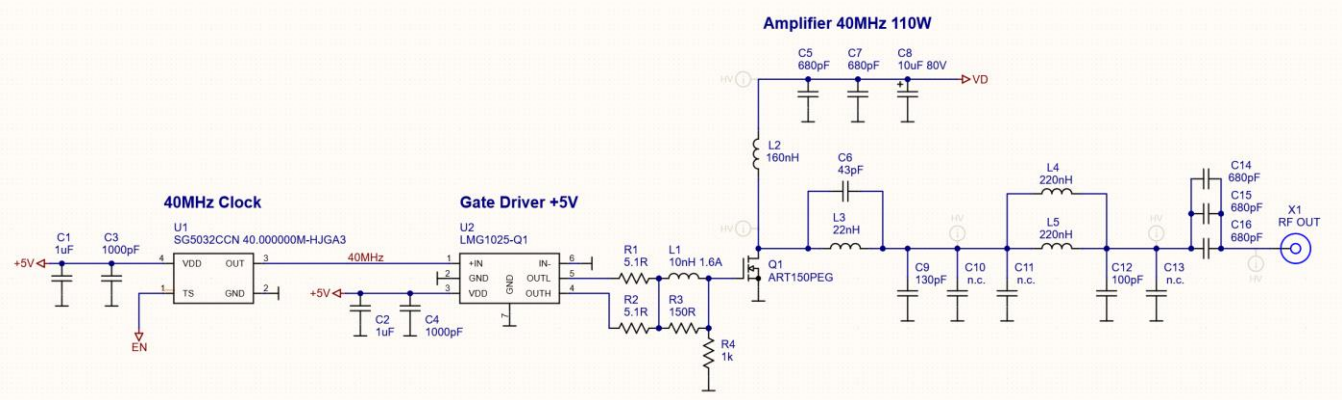

Figure 2 Schematic

5.3 Design recommendations

The frequency of operation is set by the clock U1 and can be adjusted by the IC supplier on request. The output matching supports the 40-42MHz frequency range.

In class E amplifier, peak voltage on the physical drain of transistor can reach approximately 3.5 times V_{DD}. Long-term operation at V_{DD} > 55V is not recommended.

Because of the high impedance of the interface between U1 and U2, the line on PCB is kept as short as possible. Local SMD shield covering U1, U2 and all the peripheral components might help to reduce coupling from the output matching.

The pre-distortion network might create positive and negative voltage spikes outside of the safe operating region of the gate driver U2. It is important to dump those spikes using R1-R3.

The gate driver U2 could be driven directly from the microcontroller to enable output power adjustment via pulse-width modulation (PWM).

It is possible to run the demo in pulsed mode by applying the modulation/enable signal to pin1 of U1. When operating in this mode, it might be necessary to check the ripple current in capacitor C8.

1111 capacitors C5, C6, C7, C9, C12, C14, C15, C16 shown in *Figure 1* have been replaced with cheaper 0805 capacitors (shown in the bill of materials) without any significant change in electrical or thermal characteristics.

As explained in chapter 7, two inductors 2222SQ-221GE (L4, L5) connected in parallel can be replaced with one inductor 1010VS-111ME.

6. Electrical characteristics

6.1 General characteristics

Table 2: Electrical characteristics

CW operation; 50R load; RF power measured after LPF; Tbaseplate =40°C

Symbol	Parameter	Unit	Min	Typ	Max
F	Frequency range of output matching	MHz	40	40[1]	42
V_{DD}	Drain voltage of LDMOS section	V	10	50	55
I_{DD}	Current consumption of LDMOS section	A	-	2.7	-
V_{DRIVER}	Voltage supply of driver section	V	4.75	5	5.25
I_{DRIVER}	Current consumption of driver section	mA	-	73	-
P_{OUT}	Output power	W	5.1	115	134
η_{DRAIN}	Drain efficiency	%	-	86	-
η_{LINEUP}	Lineup efficiency		-	85.5	-
P_{DISS}	Dissipated power	W	1.8	19	25
H_2	Level of 2nd harmonic	dBc	-	-18	-
H_3	Level of 3rd Harmonic	dBc	-	-35	-

[1] *Frequency of operation is set by the clock U1*

6.2 Power sweep

Table 1: Output power and efficiency as a function of drain voltage

CW operation; 50R load; RF power measured after LPF; Tbaseplate =40°C

V_{DD}, V	I_{DD}, A	P_{OUT}, W	η_{DRAIN}, %	η_{LINEUP}, %	P_{DISS}[2], W
10	0.65	5.1	78.5	74.3	1.8
15	0.92	11.1	80.4	78.4	2.7
20	1.19	19.6	82.4	81.1	4.2
25	1.45	30.4	83.9	83.0	5.9
30	1.71	43.4	84.6	84.0	7.9
35	1.96	58.5	85.3	84.8	10.1
40	2.21	76	86.0	85.6	12.4
45	2.45	95	86.2	85.9	15.3
50	2.68	115	85.8	85.6	19.0
55	2.89	134	84.3	84.1	25.0
60[1]	3.03	148	81.4	81.2	33.8
65[1]	3.08	153	76.4	76.3	47.2

[1] *Long-term operation at V_{DD} > 55V is not recommended*

[2] *Power dissipated in transistor Q1*

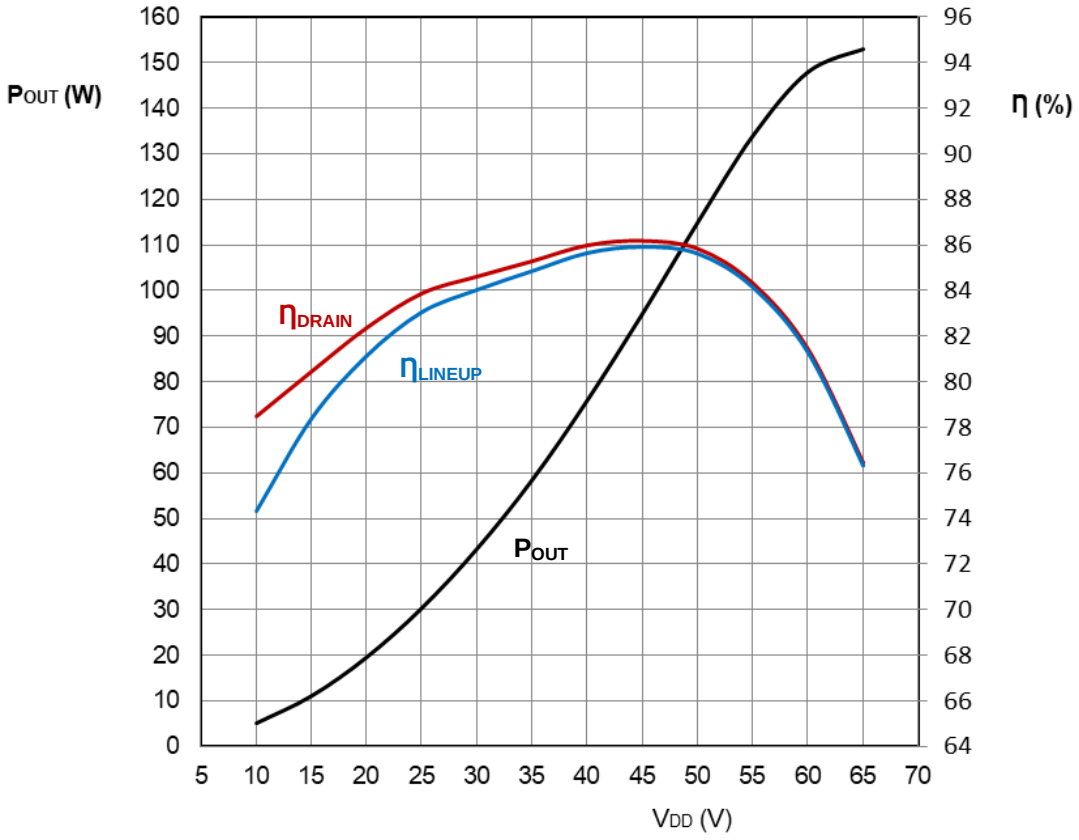

Figure 3 Output power and efficiency as a function of drain voltage

7. Thermal characteristics

The board has been measured during RF operation with IR camera to detect hotspots.

Test conditions:

V_{DD} = 50V;

P_{OUT} = 110W CW, 50R load, RF power measured after LPF;

Tbaseplate =40°C

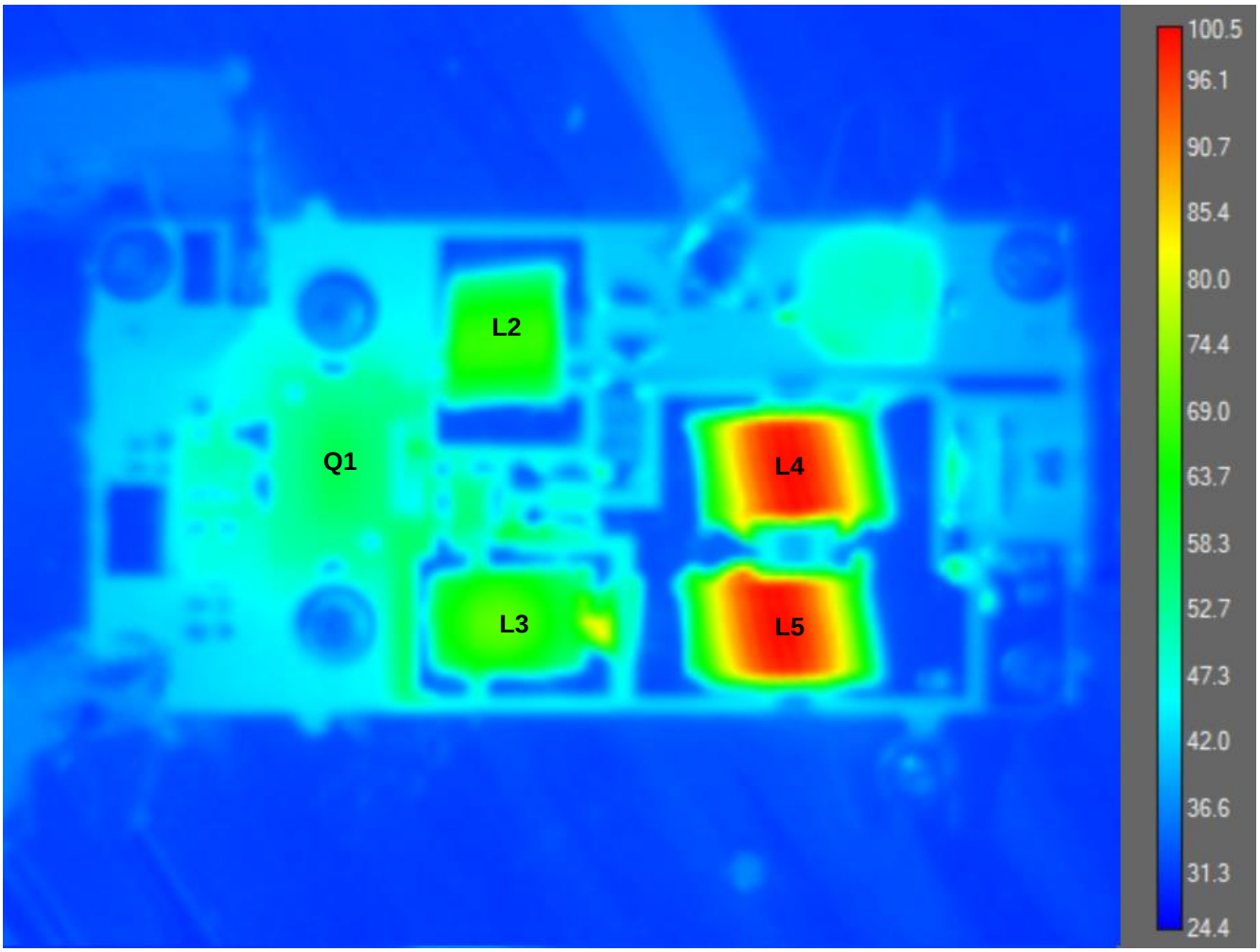

Figure 4 IR picture

The board has two hotspots – L4, L5. Both get a temperature rise of 60°C.

Those two 220nH 5A inductors 2222SQ-221GE connected in parallel were used in the demo design because of the tight ±2% tolerance. It is possible to replace L4 and L5 just with one 111nH 22A inductor 1010VS-111ME. It is up to customer to decide if ±20% tolerance of 1010VS-111ME can provide sufficient yield in mass production.

8. Hardware

8.1 Bill of materials

Table 2: Bill of Materials

Designator	Group	Value	Tolerance	Name	Manufacturer	Quantity
C1, C2	Capacitor	1uF	±10%	06036D106MAT4A	AVX	2
C3, C4	Capacitor	1000pF	±5%	06035A102JAT2A	AVX	2
C5, C7, C14, C15, C16	Capacitor	680pF	±5%	VJ0805D681KXBAJ	Vishay	5
C6	Capacitor	43pF	±5%	08051U430JAT2A	AVX	1
C8	Capacitor	10uF 80V	±20%	EEE-FN1K100XL	Panasonic	1
C9	Capacitor	130pF	±5%	08052U131JAT2A	AVX	1
C12	Capacitor	100pF	±5%	08052U101JAT2A	AVX	1
L1	Inductor	10nH 1.6A	±2%	LQW18AN10NG8ZD	Murata	1
L2	Inductor	160nH	±2%	2222SQ-161GE	Coilcraft	1
L3	Inductor	22nH	±5%	WA3097-AL	Coilcraft	1
L4, L5	Inductor	220nH	±2%	2222SQ-221GE	Coilcraft	2
Q1	Transistor			ART150PEG	Ampleon	1
R1, R2	Resistor	5.1R	±5%	ERJ-PA3J5R1V	Panasonic	2
R3	Resistor	150R	±1%	ERJ-PA3F1500V	Panasonic	1
R4	Resistor	1k	±1%	ERJ-PA3F1001V	Panasonic	1
U1	IC	40MHz		SG5032CCN 40.000000M-HJGA3	Epson	1
U2	IC			LMG1025-Q1	Texas Instruments	1

8.2 Component mapping

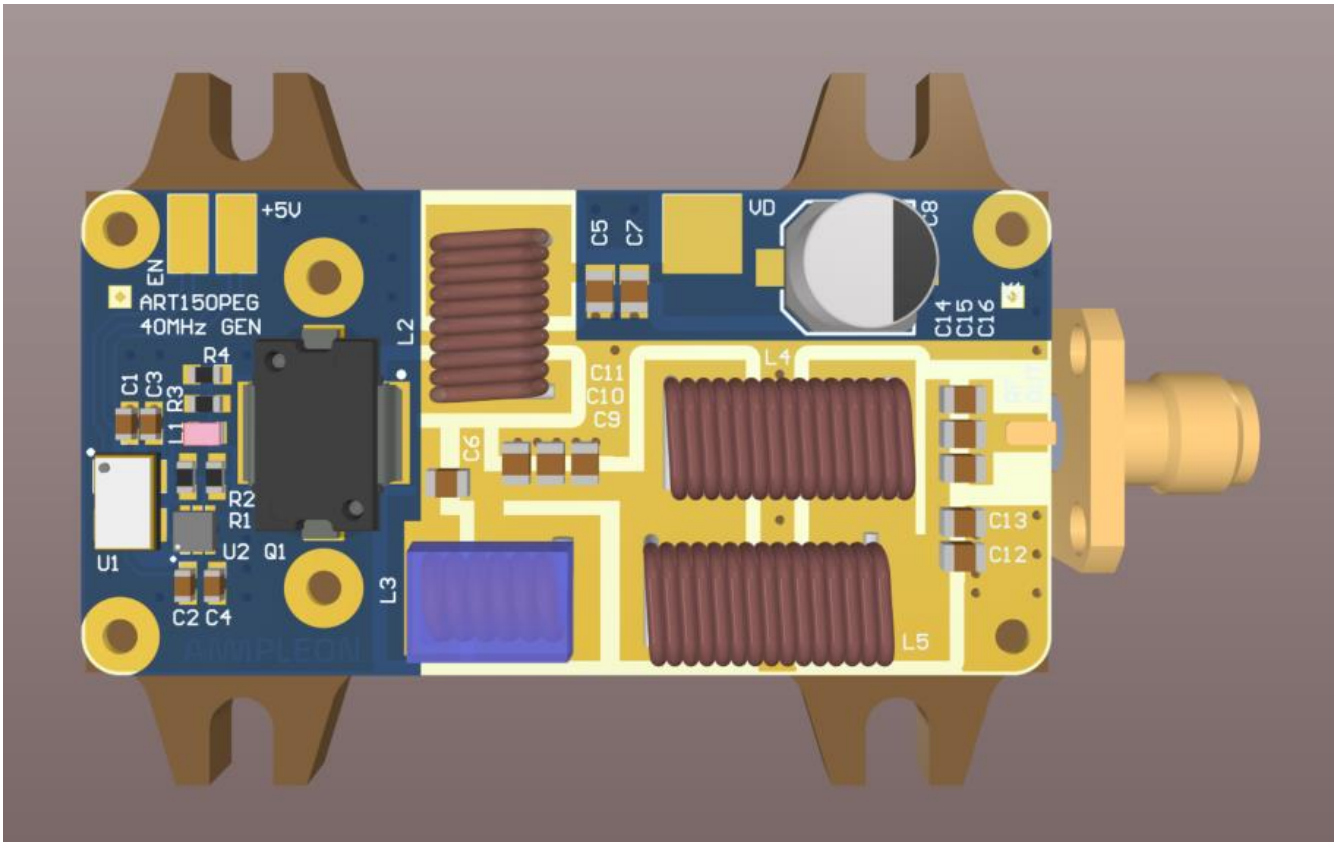

Figure 5 Component mapping

Board specifications

Table 3: Board specifications

Parameter	Value
Manufacturer	EMC
Type	EM-827BI (Lead free FR4)
Dk	4.8 @ 1MHz 4.2 @ 1GHz
Df	0.018 @ 1MHz 0.019 @ 1GHz
Laminate thickness	0.5mm / 1 oz.
Layers	2, top/bottom. Bottom all copper
Board specifics	Transistor Q1 is mounted on an I-shaped copper insert (coin)
Board dimensions	50 x 25mm

8.3 Demo markings

Table 4: Device specifics

Parameter	Value
Manufacturer	Ampleon
Device	ART150PEG
PCB marking	ART150PEG 40MHz GEN

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