

AR211072

BLF978P, 644-650 MHz

v1.0 – April 19, 2021

AMPLEON

Application Report

Document information

Status v1.0

Abstract Measurement results of a class AB design for the BLF978P in a demo optimized for 644-650 MHz.

1. Revision History

Table 1 – Report revisions

Revision	Date	Description	Author
1.0	2021.04.19	Initial document	

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5. General description

This report presents the measurement results of the demoboard designed for the 644-650 MHz frequency band using the BLF978P. During the assembly the transistor has been soldered and the leads have been bent upward to ensure proper soldering, while the PCB has been screwed down without soldering it.

The demo-circuit is matched to 50 Ω at input and output.

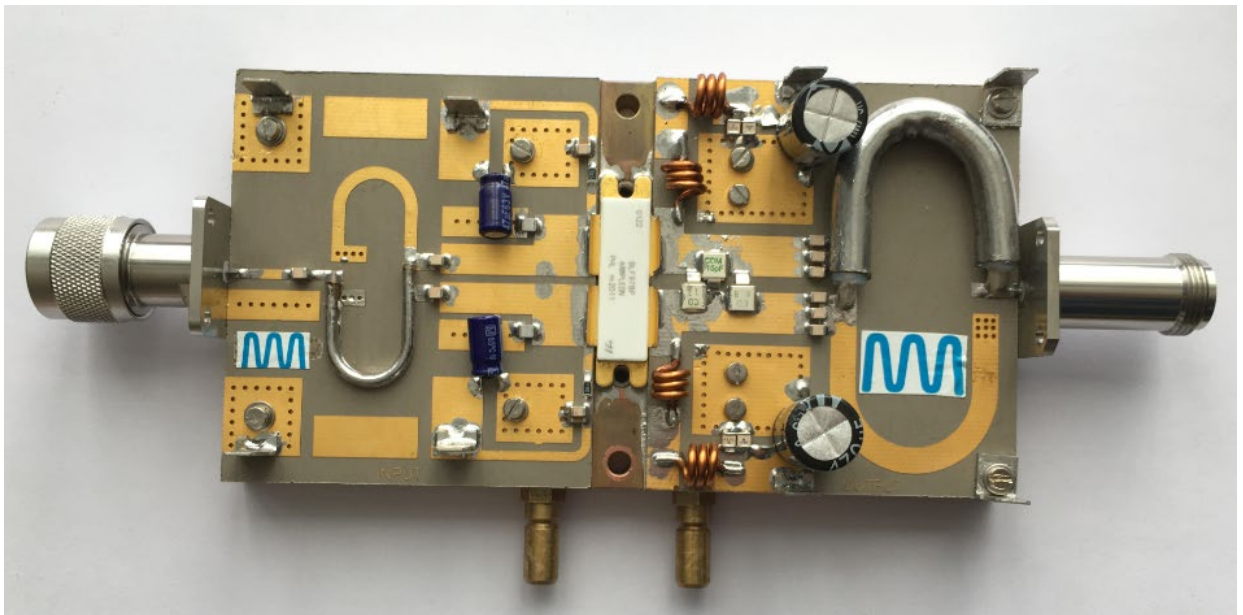


Figure 1 – Demo front view

Table 2 – Test circuit information

Parameter	Description	Unit
Input Laminate Type	Taconic RF35	
Output Laminate Type	Taconic RF35	
Laminate thickness	0.762	mm
Overall dimensions	152.3 x 80	mm
Cooling type	Indirect water cooling	
Device Package	SOT539	

6. CW RF characteristics

Table 3 – Performance indication

Test signal: CW; RF performance at $V_{DS}=50V$; Total $I_{Dq}=20mA$; $T_{amb}=21^{\circ}C$; $T_{cooling\ water}=25^{\circ}C$

Symbol	Parameter	Conditions	Typical	Unit
f	Frequency		644-650	MHz
V_{DS}	Drain-source voltage		50	V
V_{GS}	Gate-source voltage	$I_{Dq} = 10mA \times \text{section}$	1.67	V
G_p	Power gain	$P_{1dBcp} = 1047.4W$	20.1	dB
η_D	Drain efficiency	$P_{1dBcp} = 1047.4W$	70.8	%

7. CW Performance Details

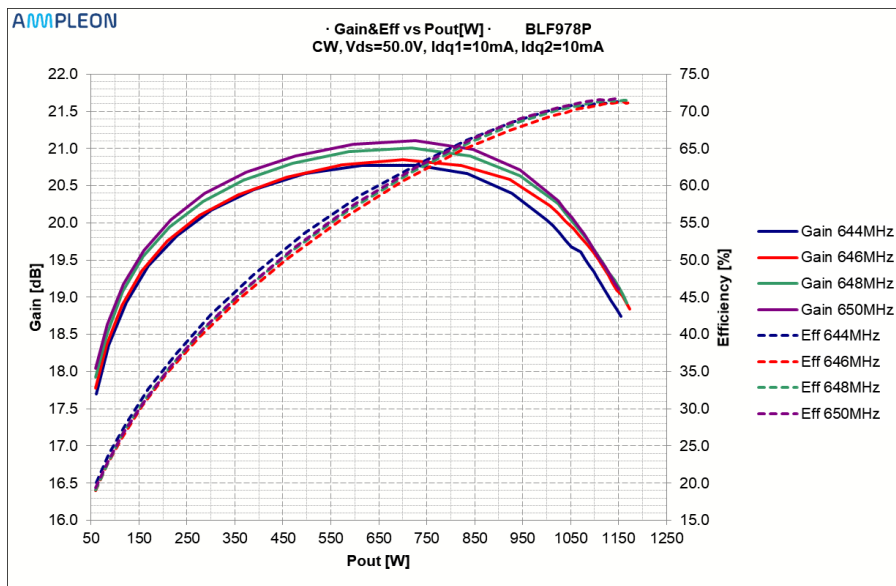


Figure 2 – CW performance

Table 4 – RF Performance overview

Freq [MHz]	Gmax [dB]	Pout@Gmax [W]	P1dB [W]	P2dB [W]	Effmax [%]	Pout@Effmax [W]	Eff P1dB [%]	Eff P2dB [%]
644	20.77	613.43	1038.80	1151.80	71.36	1155.20	70.60	71.32
646	20.85	700.69	1066.40	1173.10	71.37	1157.80	70.31	71.15
648	21.01	717.97	1055.90	1161.30	71.51	1168.10	70.65	71.50
650	21.11	726.48	1047.40	1150.10	71.74	1150.40	70.83	71.74

8. User Guide

8.1 Biasing

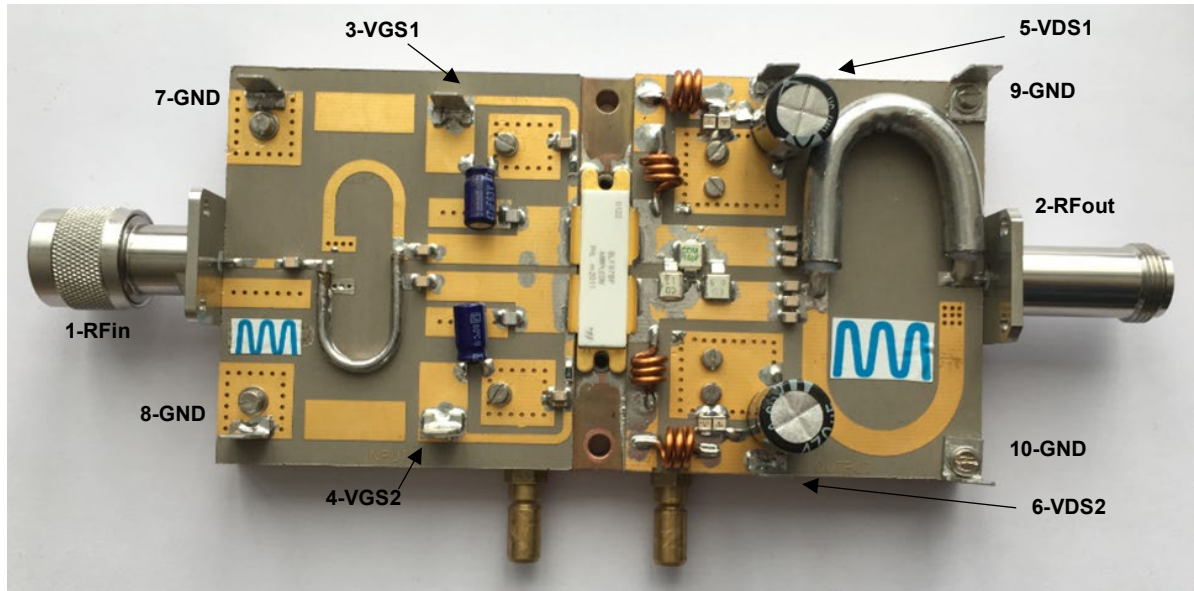


Figure 3 –Board pin configuration

Table 5 – Pin description

Symbol	Pin	Description
RF _{IN}	1	RF input
RF _{OUT}	2	RF output
V _{GS1}	3	Gate-source voltage – Section A
V _{GS2}	4	Gate-source voltage – Section B
V _{DS1}	5	Drain-source voltage – Section A
V _{DS2}	6	Drain-source voltage – Section B
V _{DS}	4	Drain-source voltage
GND	7, 8	Negative supply terminal for V _{GS}
GND	9, 10	Negative supply terminal for V _{DS}

8.2 Bill of Materials

Table 6 – Bill of Materials

Part	Description	Value	Part number /Remark
C1,C8,C9	Multilayer ceramic chip capacitor	100pF	ATC100B soldered on the side
C2,C3	Multilayer ceramic chip capacitor	75 pF	ATC100B soldered on the side
C4, C26	Multilayer ceramic chip capacitor	27 pF	ATC800B
C5,C6	Electrolytic Capacitor	47 uF, 63V	
C7,C10	Multilayer ceramic chip capacitor	100nF	Murata X7R
C11,C14	Multilayer ceramic chip capacitor	100pF	ATC100B
C12,C15	Multilayer ceramic chip capacitor	1nF	ATC100B
C13,C16	Electrolytic Capacitor	470uF, 63V	
C17	SMT Clad RF Capacitors	12pF	CDE MIN02 *To be assembled close to C18 for the highest performance
C18	SMT Clad RF Capacitors	15pF	CDE MIN02
C19	SMT Clad RF Capacitors	6.8pF	CDE MIN02
C20,C21,C22,C23,C24,C25	Multilayer ceramic chip capacitor	15pF	ATC100B soldered on the side
L1,L2	Inductor	3 turns, 1.7mm, 4mm diameter, close wound	
L3,L4	Inductor	3 turns, 1.7mm, 5mm diameter, close wound	
R1,R2	Chip Resistor	47Ω	SMD 1206
Balun B1	Semirigid Zc=25	UT-090C-25	
Balun B2	Semirigid Zc=25	UT-300C-25	
T1	LD MOS transistor	BLF978P	
Input PCB	Taconic RF35	H=0.762mm, Cu=2x35um	Er=3.48
Output PCB	Taconic RF35	H=0.762mm, Cu=2x70um	Er=3.48

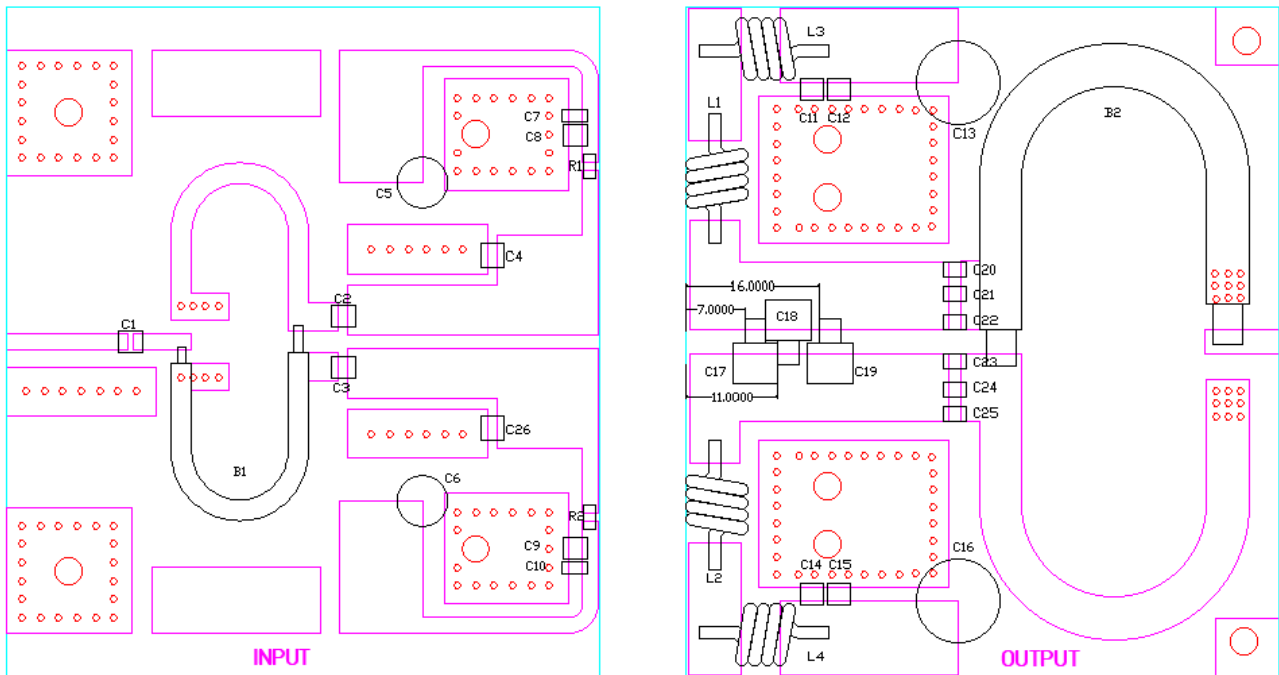


Figure 4 – Component mapping

8.3 Temperature behavior

For operation of this demo board water cooling should be applied. Water temperature should be kept at 25 degC.

8.4 Device markings

Table 7 – Module specifics

Parameter	Value
Manufacturer	Ampleon
Device	BLF978P
Comments	Engineering sample

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