AR201213

ART35FE, 60-130 MHz

v1.0 – September 29, 2020

AMPLEON

Application Report

Document information	
Status	v1.0
Abstract	Measurement results of a wideband demoboard design with the ART35FE in the 60-130 MHz bandwidth

1. Revision History

Table 1 – Report revisions

Revision	Date	Description	Author
1.0	2020.09.29	Initial document	

2. Contents

3. List of figures

4. List of tables

5. General description

This report presents the measurement results of the demoboard designed for 60-130 MHz frequency band using the ART35FE transistor based on 65V ART technology. During assembly, the PCB has been screwed down without soldering it and the connection of the transistor has been made with a pressing block.

The dedicated demo-circuit is matched to 50 Ω at input and output.

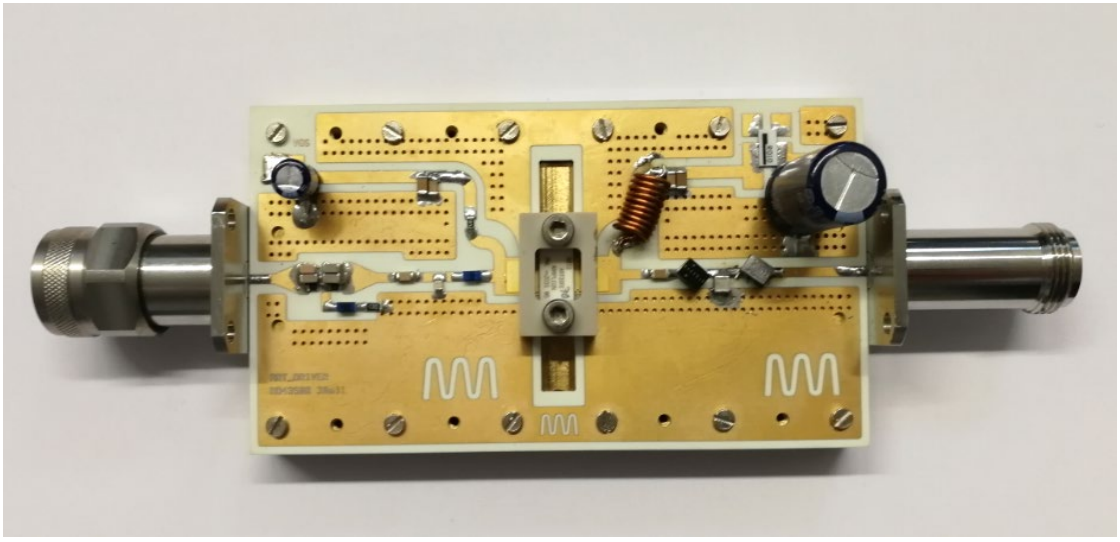


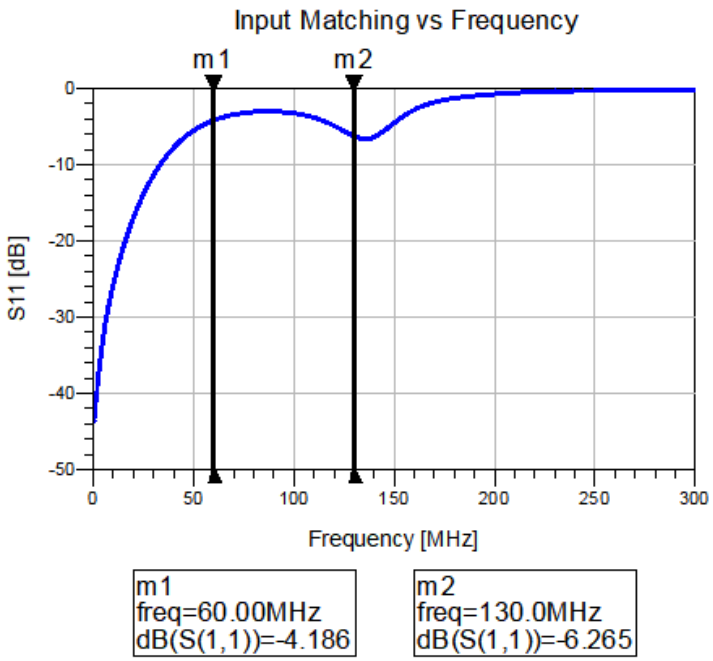
Figure 1 – Demo front view

Table 2 – Test circuit information

Parameter	Description	Unit
Laminate Type	Rogers 4350B	
Dk	3.48	
Df	0.0037 @10 GHz	
Laminate thickness	0.762	mm
Copper thickness	1 oz top/bottom	
Overall dimensions	106 x 60	mm
Cooling type	Indirect water cooling	
Device Package	SOT467	

6. Measured S-Parameters

Measurement conditions: V_{DS}=65V; I_{Dq}=100mA; $T_{cooling\ water}$ =25°C



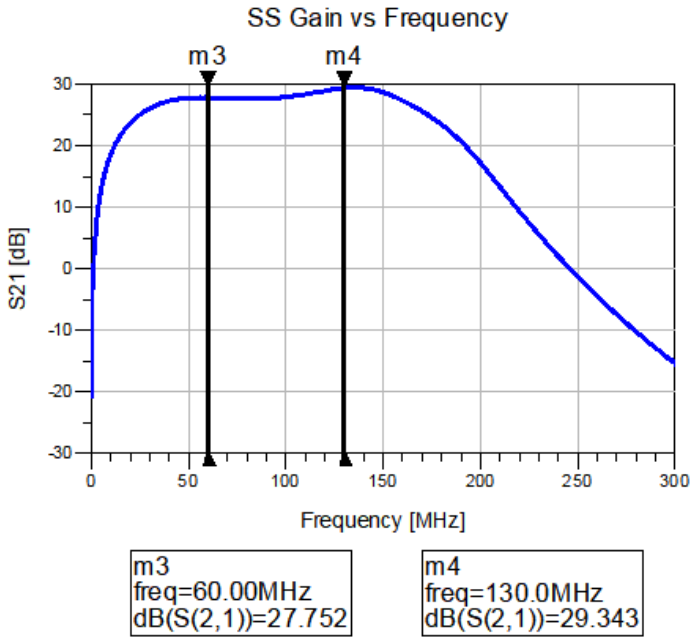


Figure 2 – Measured S parameters: Input Matching (top), Gain (bottom)

7. CW RF characteristics

Table 3 – Performance indication

Test signal: CW; RF performance at V_{DS}=65V; I_{Dq}=10mA; $T_{cooling\ water}$=25°C

Symbol	Parameter	Conditions	Typical	Unit
f	Frequency		130	MHz
V_{DS}	Drain-source voltage		65	V
V_{GS}	Gate-source voltage	I_{Dq} = 10mA	2.05	V
Gp	Power Gain	P_{1dBcp}=38.9 W	27.4	dB
η_D	Drain Efficiency	P_{1dBcp}=38.9 W	79.1	%

8. CW Performance Details

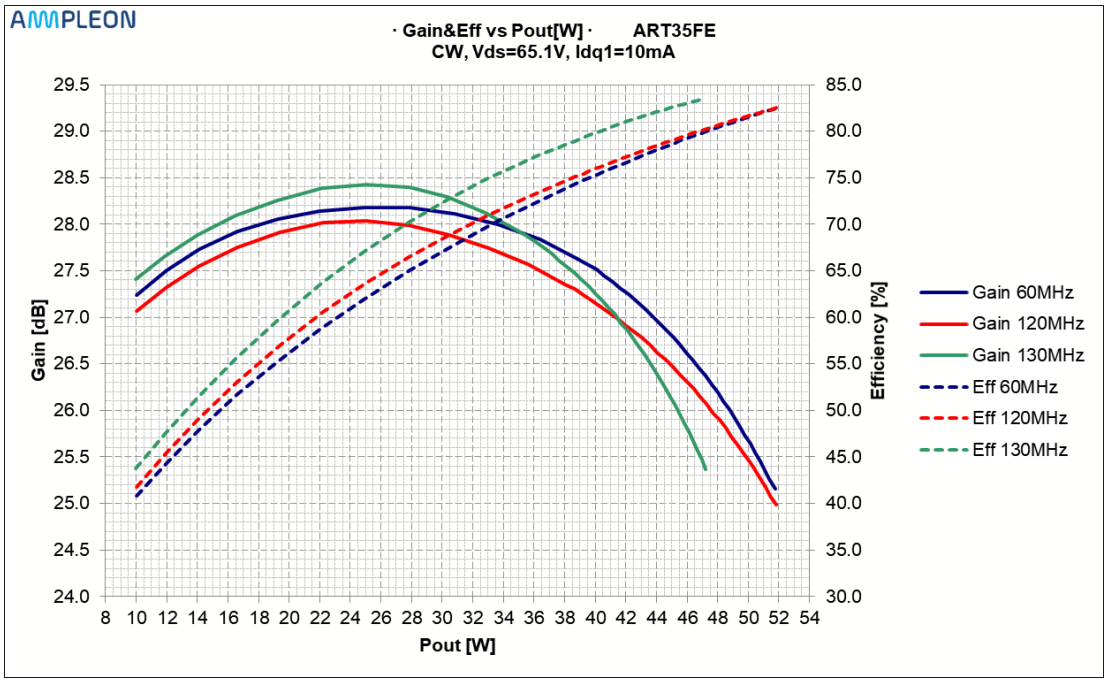


Figure 3 – Demo board CW performance

Table 4 – RF Performance overview

Freq [MHz]	Gmax [dB]	Pout@ Gmax [W]	P1dB [W]	P2dB [W]	P3dB [W]	Effmax [%]	Pout@ Effmax [W]	Eff P1dB [%]	Eff P2dB [%]	Eff P3dB [%]
60	28.18	24.86	42.65	48.05	51.66	82.46	51.74	77.08	80.46	82.41
120	28.03	25.02	41.04	47.44	51.62	82.52	51.80	76.63	80.35	82.41
130	28.43	25.05	38.92	43.87	47.07	83.55	47.23	79.15	82.00	83.49

9. User Guide

9.1 Biasing

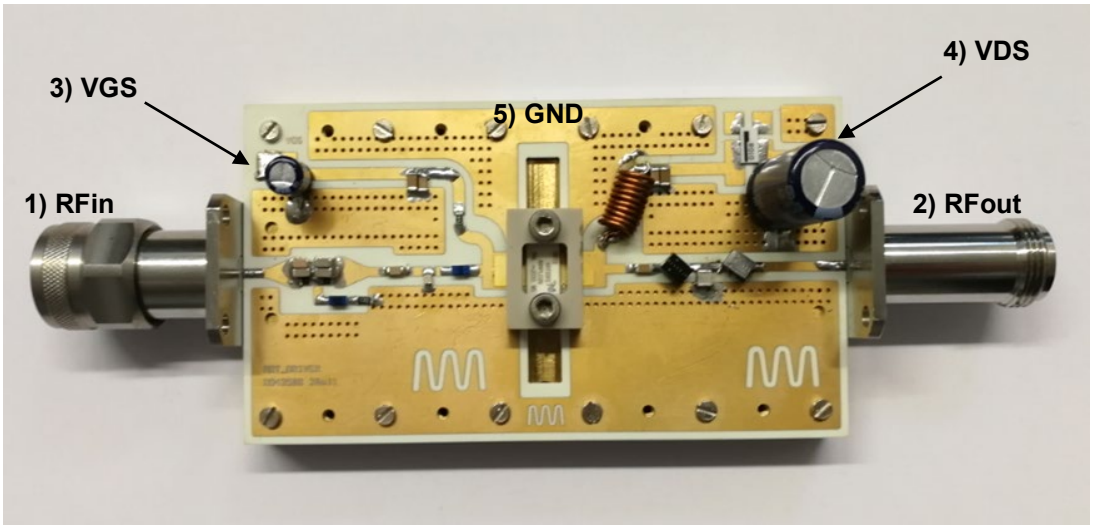


Figure 4 – Application board pin configuration

Table 5 – Pin description

Symbol	Pin	Description
RF_{IN}	1	RF input
RF_{OUT}	2	RF output
V_{GS}	3	Gate-source voltage
V_{DS}	4	Drain-source voltage
GND	5	Negative supply terminal for V_{DS} and V_{GS}

9.2 Bill of Materials

Table 6 – Bill of Materials

Part	Description	Value	Remark
C1	Multilayer ceramic chip capacitor	2x910 pF	ATC800B
C2	Multilayer ceramic chip capacitor	2x620 pF	ATC800B
C3	Electrolytic capacitor	47uF	
C10	Electrolytic capacitor	220 uF	100V
C4, C9	Multilayer ceramic chip capacitor	4.7uF	100V
C5, C6, C8, C11	Multilayer ceramic chip capacitor	100 nF	100V
C7	Multilayer ceramic chip capacitor	30 pF	ATC800A
C12	Multilayer ceramic chip capacitor	24 pF	ATC800B
R1, R2	Chip Resistor	2.4 Ohm	1206
R3	Chip Resistor	43 Ohm	1206
R4	Chip Resistor	5.1 kOhm	1206
L1	Chip Inductor	270 nH	1206CS
L2	Chip Inductor	68nH	1206CS
L3	Air core Inductor	10 turns, D=5mm WireD=0.8mm	
L4	Air core Inductor	68 nH	1812SMS
L5	Air core Inductor	22 nH	1812SMS

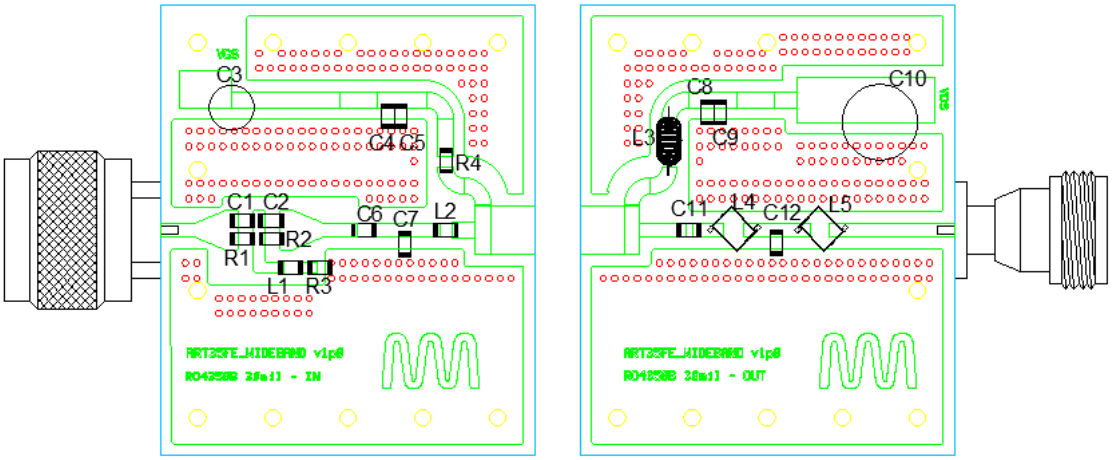


Figure 5 – Component mapping

9.3 Device markings

Table 7 – Module specifics

Parameter	Value
Manufacturer	Ampleon
Device	ART35FE
Comments	Engineering sample: PHL m2035 W5

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