

AR201165

BLF978P, 352 MHz

v1.0 – October 30, 2020

AMPLEON

Application Report

Document information

Status v1.0

Abstract Measurement results of a demoboard design with the BLF978P optimized for 352 MHz

1. Revision History

Table 1 – Report revisions

Revision	Date	Description	Author
1.0	2020.10.30	Initial document	

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5. General description

This report presents the measurement results of the demoboard designed for 352 MHz frequency using the BLF978P transistor. During assembly, the PCB has been screwed down without soldering it and the transistor has been soldered.

The dedicated demo-circuit is matched to 50 Ω at input and output.

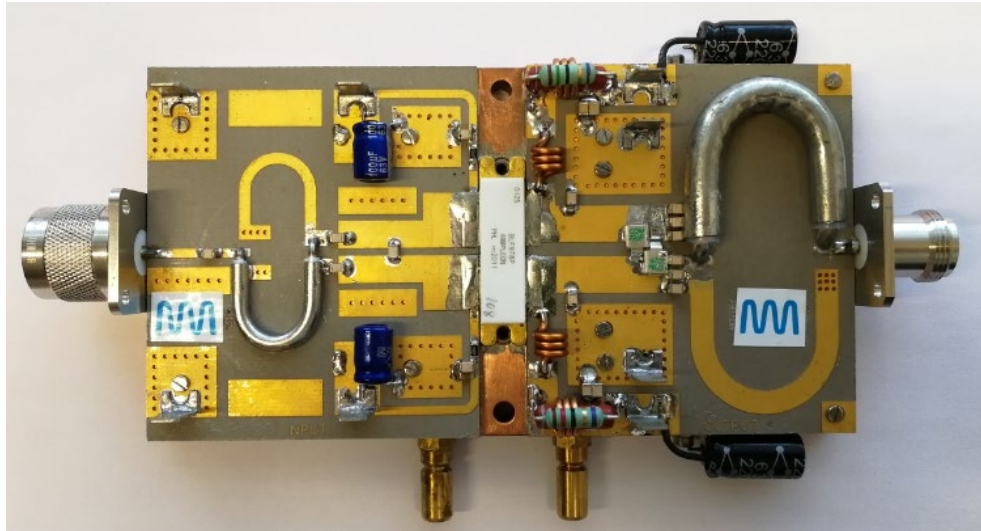


Figure 1 – Demo front view

Table 2 – Test circuit information

Parameter	Description	Unit
Input Laminate Type	Taconic RF35	
Output Laminate Type	Taconic RF35	
Df	0.0018 @ 1.9 GHz	
Dk	3.5	
Laminate thickness	0.762	mm
Copper thickness Input PCB	1 oz	
Copper thickness Output PCB	2 oz	
Overall dimensions	152.3 x 80.2	mm
Cooling type	Indirect water cooling	
Device Package	SOT539	

6. CW RF characteristics

Table 3 – Performance indication

Test signal: CW; RF performance at $V_{DS}=50V$; Total $I_{Dq}=20mA$; $T_{cooling\ water}=25^{\circ}C$

Symbol	Parameter	Conditions	Typical	Unit
f	Frequency		352	MHz
V_{DS}	Drain-source voltage		50	V
V_{GS}	Gate-source voltage	$I_{Dq} = 10mA$ x section	1.6	V
Gp	Power Gain	$P_{1dBcp}=1166.1\ W$	23.46	dB
η_D	Drain Efficiency	$P_{1dBcp}=1166.1\ W$	77.37	%

7. CW Performance Details

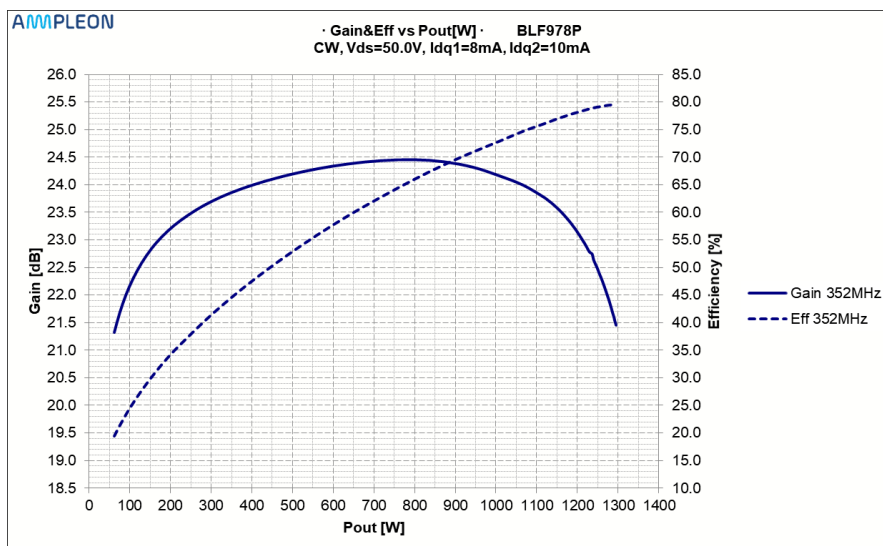


Figure 2 – Demo board CW performance

Table 4 – RF Performance overview

Freq [MHz]	Gmax [dB]	Pout@Gmax [W]	P1dB [W]	P2dB [W]	P3dB [W]	Effmax [%]	Pout@Effmax [W]	Eff P1dB [%]	Eff P2dB [%]	Eff P3dB [%]
352	24.46	797.26	1166.10	1250.10	1294.70	79.58	1294.80	77.37	79.12	79.57

8. User Guide

8.1 Biasing

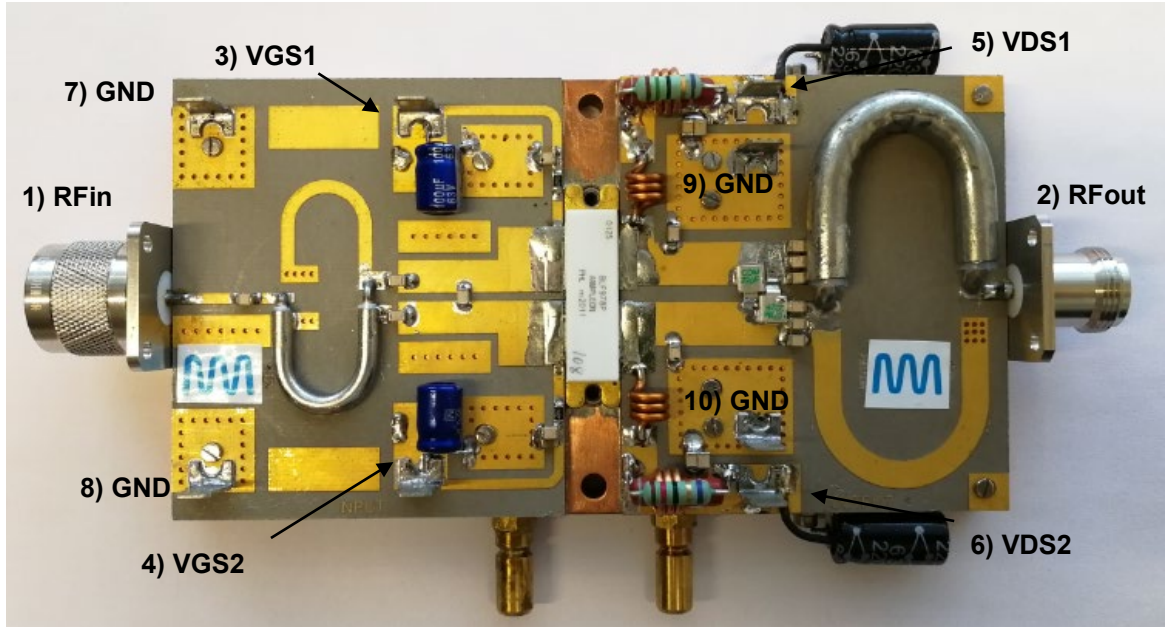


Figure 3 – Application board pin configuration

Table 5 – Pin description

Symbol	Pin	Description
RF _{IN}	1	RF input
RF _{OUT}	2	RF output
V _{GS1}	3	Gate-source voltage – Section 1
V _{GS2}	4	Gate-source voltage – Section 2
V _{DS1}	5	Drain-source voltage – Section 1
V _{DS2}	6	Drain-source voltage – Section 2
GND	7, 8	Negative supply terminal for V _{GS}
GND	9, 10	Negative supply terminal for V _{DS}

8.2 Bill of Materials

Table 6 – Bill of Materials

Part	Description	Value	Part number /Remark
C1,C8,C9	Multilayer ceramic chip capacitor	100pF	ATC100B soldered on the side
C2,C3	Multilayer ceramic chip capacitor	56pF	ATC100B soldered on the side
C4	Multilayer ceramic chip capacitor	75pF	ATC100B
C5,C6	Electrolytic Capacitor	100uF 63V	
C7,C10	Multilayer ceramic chip capacitor	100nF	Murata X7R
C11,C14	Multilayer ceramic chip capacitor	100pF	ATC100B soldered on the side
C12,C15	Multilayer ceramic chip capacitor	1nF	ATC100B soldered on the side
C13,C16	Electrolytic Capacitor	220uF 63V	
C17,C18	SMT Clad RF Capacitors	22pF	CDE MIN02
C19,C20,C21, C22,C23,C24	Multilayer ceramic chip capacitor	47pF	
C25,C26	Multilayer ceramic chip capacitor	15 pF	ATC100B soldered on the side
L1,L4		3 turns, 1.7mm, 5mm diameter, close wound, parallel to R4 and R5	
L2,L3		3 turns, 1.7mm, 4mm diameter, close wound	
R1,R2	Chip Resistor	47Ω	SMD 1206
R3,R6	Chip Resistor	15Ω	3W
R4,R5	Chip Resistor	8.2Ω	3W
Balun B1	Semirigid Zc=25	UT-090C-25	
Balun B2	Semirigid Zc=25	UT-300C-25	
T1	LDMOS transistor	BLF978P	

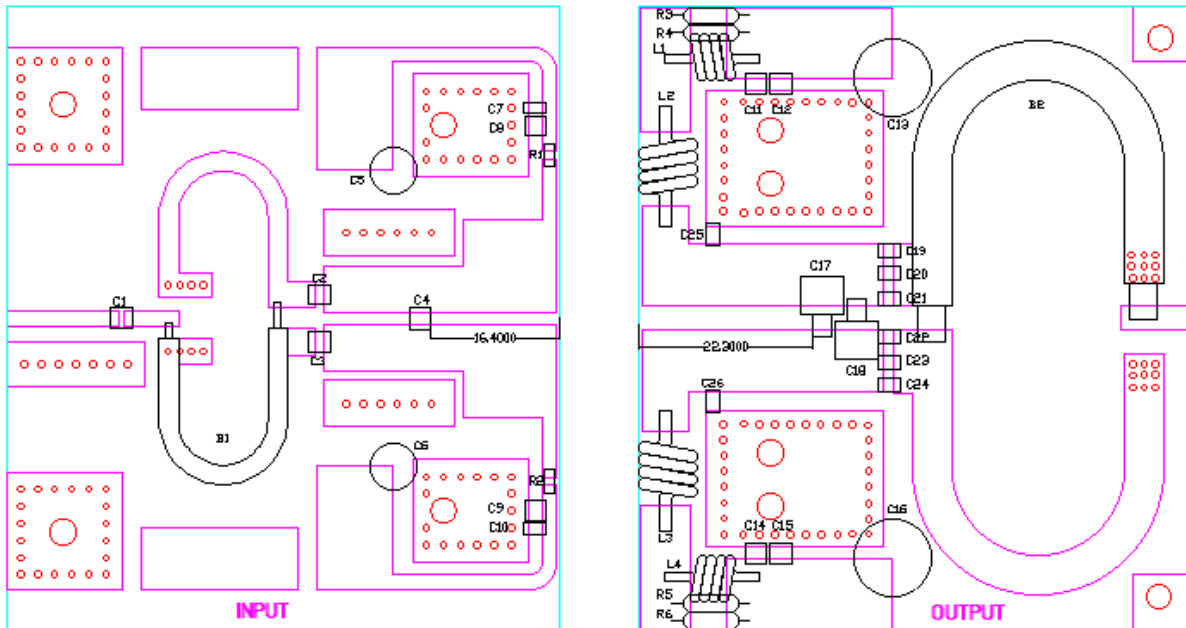


Figure 4 – Component mapping

8.3 Demoboard cooling

For operation of this demo board water cooling should be applied. Water temperature should be kept at 25 degC.

8.4 Device markings

Table 7 – Module specifics

Parameter	Value
Manufacturer	Ampleon
Device	BLF978P
Comments	Engineering sample

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