AR201138

ART2K0FE demo for 352 MHz 1500 W CW power amplifier

Rev. 2 — 26 October 2020

Application report

Document information

Info	Content
Keywords	ART2K0FE, 352 MHz, Coplanar balun, 65 V LDMOS
Abstract	This application report describes the design and performance of a 1500 W 352 MHz CW power amplifier using the LDMOS ART2K0FE power transistor and PCB integrated coplanar baluns.

Revision history

Rev	Date	Description
1	20201014	Initial version
2	20201026	Correct thermal calculation. Include Rth from cooling water to heatsink. CDE capacitors type corrected.

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1. Introduction

This application report describes the results of an ART2K0FE demo board at 352 MHz producing 1500 watt CW with an efficiency of more than 74 %.

This amplifier design can be used in synchrotron particle accelerators but can also be used for other applications at this frequency.

The demo board has been tested at VDD = 50 V, 60 V and 65 V, with a quiescent drain current (IDq) of 100 mA, 200 mA and 500 mA for the total device. Gain and efficiency were measured CW at 352 MHz. IDq is adjusted by connecting a voltage supply to the respective connections on the input circuit. The procedure to adjust the IDq is to start with a low voltage of approximately 0.5 V and increase the voltage slowly until the IDq reaches the wanted value. The gate bias voltage (VGG) value needed is approximately 1.73 V for 100 mA, 1.93 V for 200 mA and 2.01 V for 500 mA.

Results of the measurements are shown in section 2.2.

A picture of the amplifier is shown below in figure 1. The size of the demo board is 80 mm x 150 mm, excluding the N-connectors.

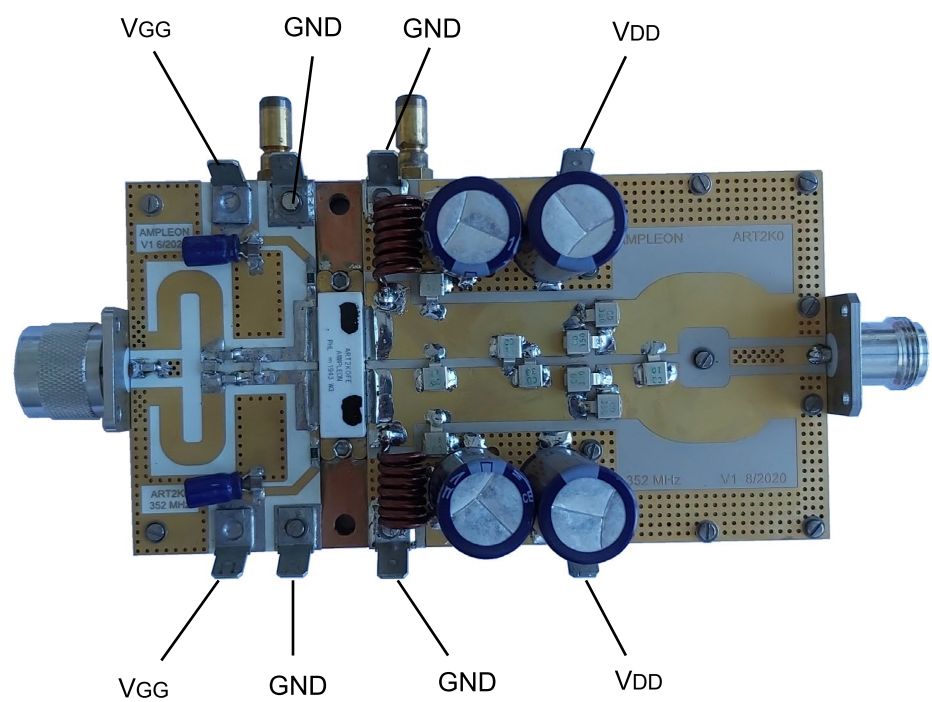


Fig 1. ART2K0FE amplifier demo board

2. Test circuit

The test circuit has the following features:

- 352 MHz operating frequency
- 1500 W power output at 74 % efficiency
- RF and thermally stable
- Demo board size 80 mm x 150 mm
- Coplanar balun at the input and output circuit
- Water cooled

2.1 Schematic diagram

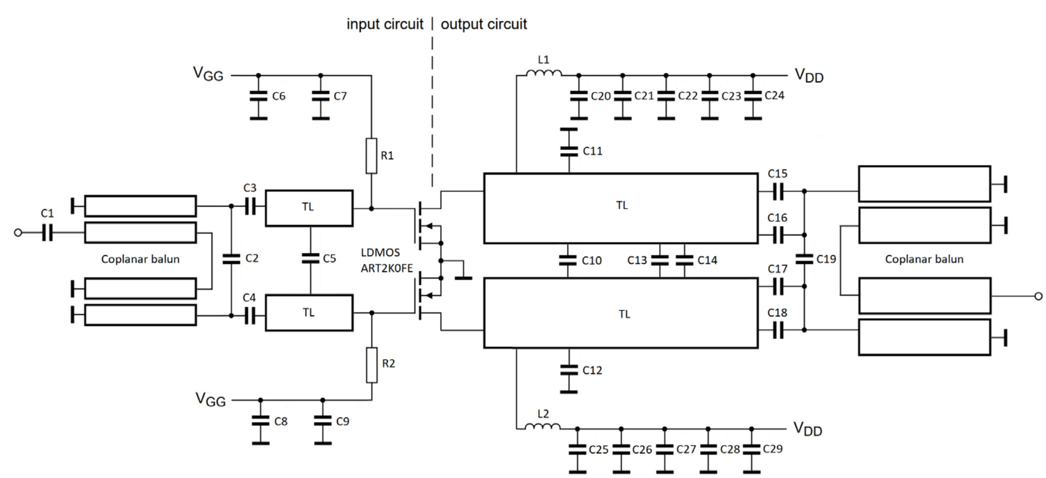


Fig 2. ART2K0FE amplifier circuit

The demo board was built with double sided RT/duroid 6035HTC substrate material with ε_r = 3.5. The substrate material has a height of 0.762 mm and the final copper thickness is 70 µm. Both input and output circuit use the same substrate material.

Cooling is provided by connecting a 25 °C water supply to the baseplate cooling tubes.

Both input and output circuit make use of a coplanar balun that are more production friendly because it omits the use of thick coaxial balun cables that are difficult to handle and give assembly variations. The coplanar balun is designed to have the balanced side on the top metal layer, while the single ended side is using the bottom metal layer. To reduce the baseplate ground effect on the single ended side, a 5 mm deep cavity is present underneath the baluns inside the baseplate.

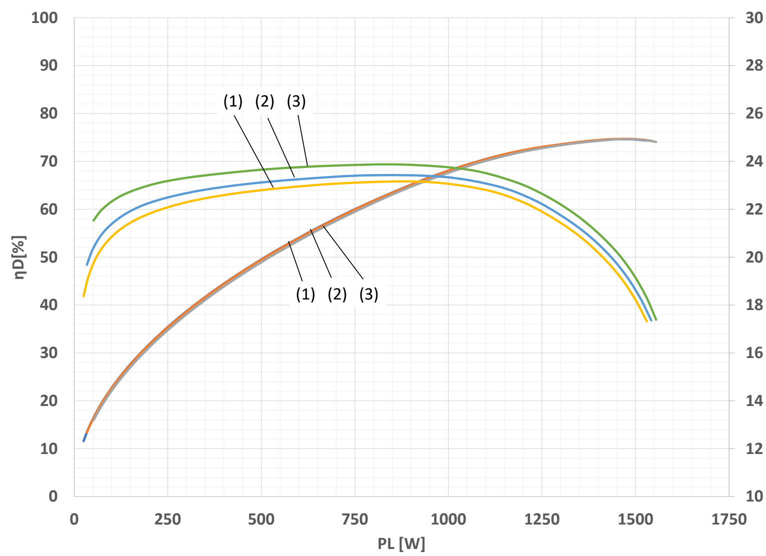
At the input circuit the power levels are low enough that no excess heating occurs, and an air cavity is sufficient for the input balun. The output balun must handle high power levels and extra cooling is required to avoid overheating. To give extra cooling to the output balun the output cavity is filled with *Thermipad TP22626* thermal gap filler material. The output balun is designed according to the ε_r of the Thermipad material. In the middle of the balun cavity a small pedestal is available on which the coplanar balun can be pulled down with a small screw this to make sure the coplanar balun makes tight contact with the Thermal Gap filler material.

To reduce losses and heat generation in the output circuit high quality Cornell Dubilier mica capacitors need to be used.

The circuit can be slightly tuned for different combinations of maximum output power and efficiency by varying the value and position of C10, C11 and C12 in the output circuit.

At the input circuit the S11 and amplifier gain can be optimized by changing the value and position of capacitor C5.

2.2 Measurement data

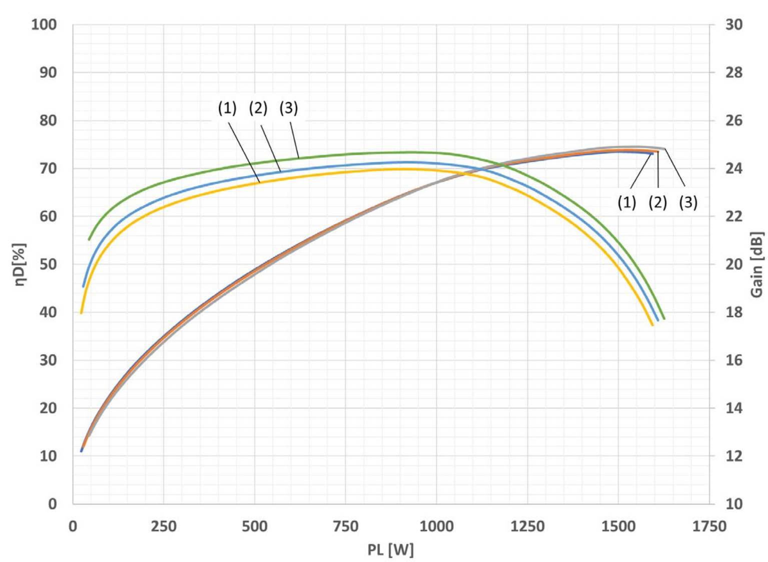


(1) I_{Dq} = 100 mA

(2) I_{Dq} = 200 mA

(3) I_{Dq} = 500 mA

Fig 3. Gain and drain efficiency as function of output power; VDS = 65 V; CW

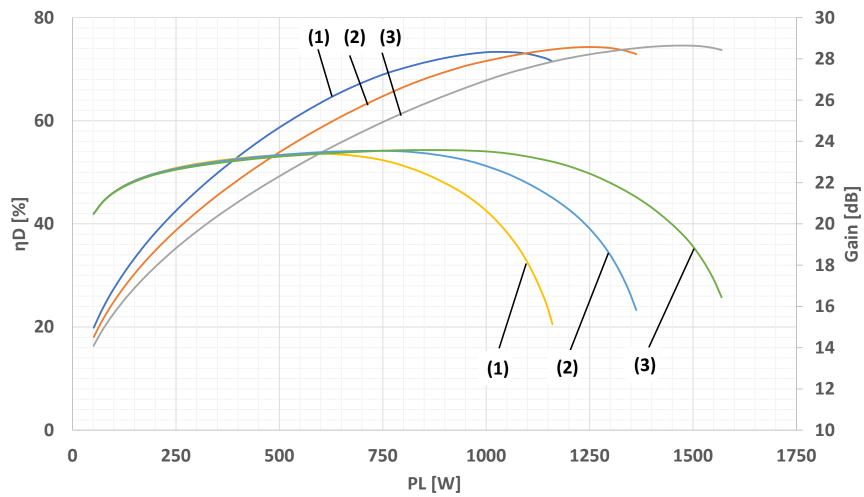


(1) I_{Dq} = 100 mA

(2) I_{Dq} = 200 mA

(3) I_{Dq} = 500 mA

Fig 4. Gain and drain efficiency as function of output power; VDS = 65 V; δ = 10 %



(1) V_{DS} = 55 V

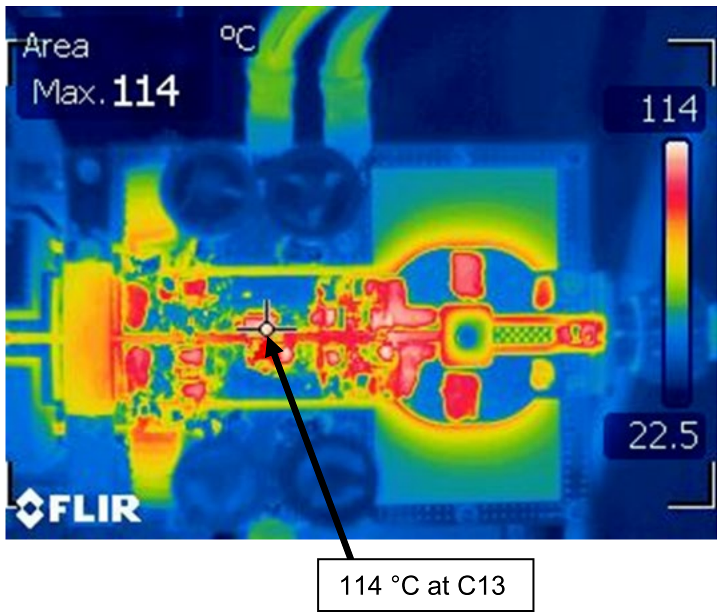
(2) V_{DS} = 60 V

(3) V_{DS} = 65 V

Fig 5. Gain and drain efficiency as function of output power and V_{DS}; CW

2.3 Thermal behavior of the output circuit

The highest temperature measured at 1550 W CW is 114 °C at the matching capacitor C13 in the output circuit.



Vds = 65 V, IDq = 200 mA, PL = 1550 W

Fig 6. Output circuit infrared thermal measurement

The junction temperature of the LDMOS die was estimated from infrared thermal test data that is available and shown in figure 6. It is estimated by calculation that the power dissipation (Pdiss) is approximately 542 W (at PL = 1550 W and η_D = 74.1 %). When the device is well soldered to the heatsink the total Rth from die to heatsink will be around 0.12 K/W. The Rth from heatsink to the cooling water is 0.08 K/W, giving a total die to water Rth of 0.2 K/W. This will give a die temperature of 134 °C when the cooling water temperature is 25 °C.

2.4 Layout and components

2.4.1 Output circuit

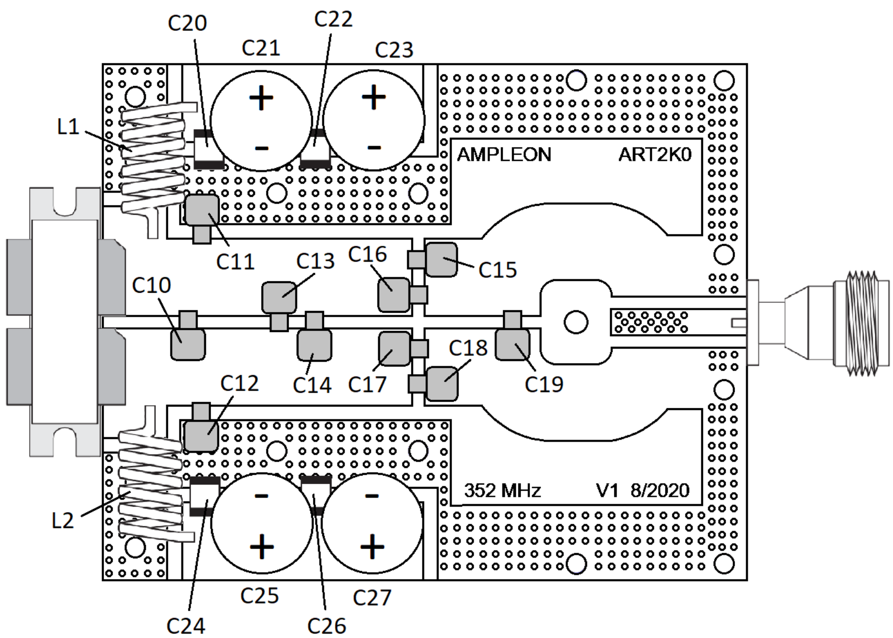


Fig 7. Output circuit

For demo purposes the output circuit makes use of a female N-connector for easy handling. It is however highly recommended to use a connector type that can handle higher power levels in a final application, like a 7/16 type connector.

Table 1. Output circuit bill of materials

Circuit reference	Description	Type / manufacturer
PCB	RT/duroid 6035HTC, 0.762 mm height, 70 µm CU thickness	Rogers
L1, L2	6 turns, 2.0 mm wire, 6 mm diameter, close wound	Enamel copper wire
C10	47 pF	Cornell Dubilier MIN02-002
C11, C12	91 pF	Cornell Dubilier MIN02-002
C13	33 pF	Cornell Dubilier MIN02-002
C14	36 pF	Cornell Dubilier MIN02-002
C15, C16, C17 C18	350 pF	Cornell Dubilier MIN02-002
C19	18 pF	Cornell Dubilier MIN02-002
C20, C24	1 nF	ATC800B
C21, C23, C25 C27	1000 µF / 100 V	Electrolytic
C22, C26	10 uF / 100 V	X7R ceramic
N connector	Female, 50 Ω	Suhner
LDMOS	ART2K0FE	Ampleon

2.4.2 Input circuit

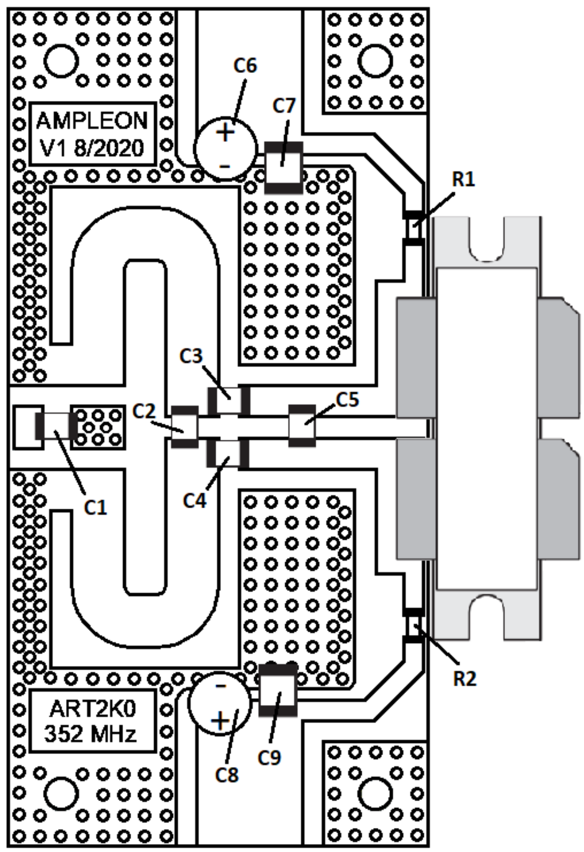


Fig 8. Input circuit

Table 2. Input circuit bill of materials

Circuit reference	Description	Type / manufacturer
PCB	RT/duroid 6035HTC, 0.762 mm height, 70 μm CU thickness	Rogers
R1, R2	47 Ω	1206 SMD
C1	110 pF	ATC800B
C2	18 pF	ATC800B
C3, C4	33 pF	ATC800B
C5	47 pF	ATC800B
C6, C8	47 μF / 63V	Electrolytic
C7, C9	1 nF	ATC800B
N connector	Male, 50 Ω	Suhner

3. Abbreviations

Table 3. Abbreviations

Acronym	Description
CW	Continuous Wave
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PCB	Printed-Circuit Board

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5. Contents

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