

AR191199

BLC2425M10LS500P,
2400-2500 MHz

v1.0 – December 16, 2019

AMPLEON

Application Report

Document information

Status	v1.0
Abstract	Measurement results of a 2400-2500 MHz demo with BLC2425M10LS500P.
Demo number	AR191199

1. Revision History

Table 1 – Report revisions

Revision	Date	Description	Author
1.0	2019.12.16	Initial document	

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5. General description

This report presents the measurement results of the high efficiency 500W GEN10 LDMOS demo using the BLC2425M10LS500P transistor in the frequency range from 2400MHz to 2500MHz. The demo is matched to 50 Ω at input and output.

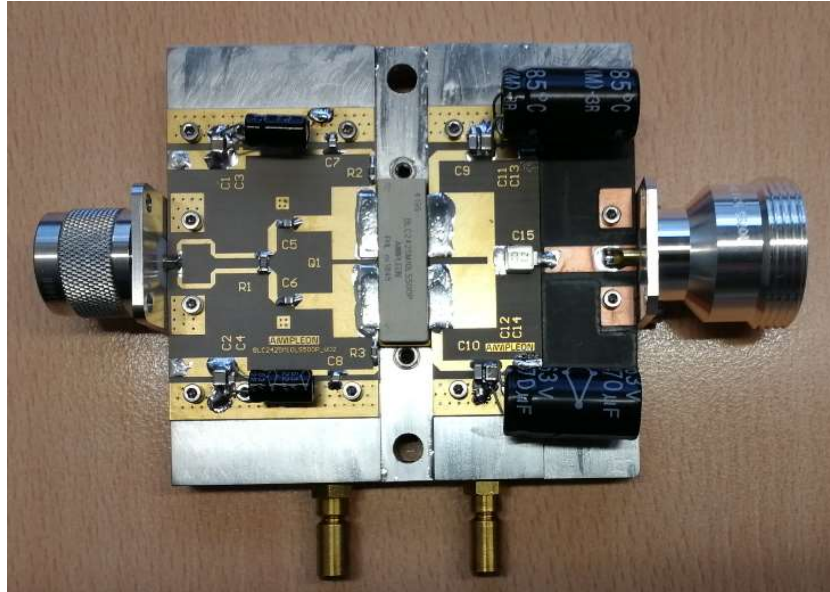


Figure 1 – Demo view of the BLC2425M10LS500P

Table 2 – Demo circuit information

Parameter	Description	Unit
Input Laminate Type	TC350, 30 mils	
Output Laminate1 Type	TC350, 30 mils	
Output Laminate2 Type	RT/Duroid 5880, 62 mils	
Overall dimensions	90.3 x 85	mm
IN PCB dimensions	40 x 60	mm
OUT PCB dimensions	40 x 60	mm
Cooling type	Indirect water cooling	
Device Package	SOT1250-1	

6. RF characteristics

Table 3 – RF characteristics

Test signal: CW; RF performance at $V_{DS}=32V$; Total $I_{Dq}=20mA$; $T_{amb}=25^{\circ}C$; $T_{cooling\ water}=25^{\circ}C$

Symbol	Parameter	Conditions	Typical	Unit
f	Frequency		2400–2500	MHz
V_{DS}	Drain-source voltage		32	V
V_{GS1}	Gate-source voltage		1.7	V
V_{GS2}	Gate-source voltage		1.7	V
G_p	Power gain	$P_{1dBcp} = 515W$	14.9	dB
η_D	Drain efficiency	$P_{1dBcp} = 515W$	68.8	%

7. Performance Details

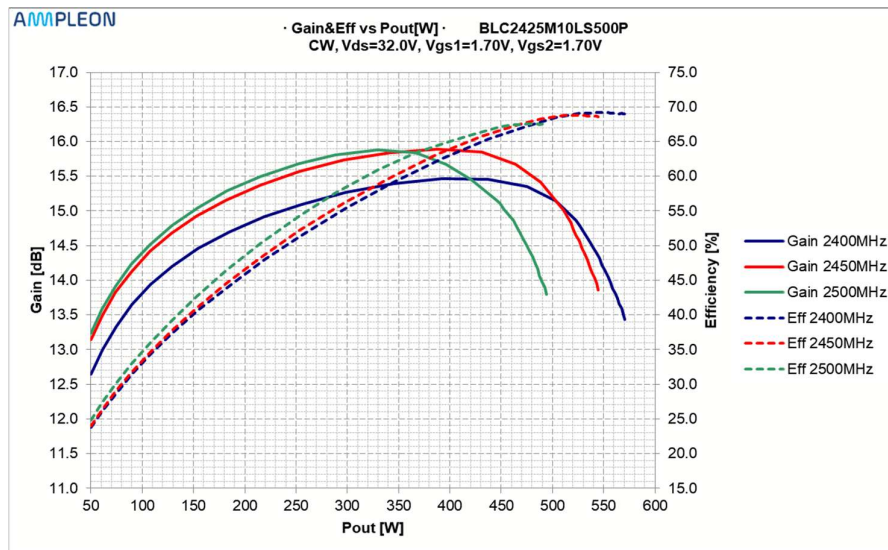


Figure 2 – BLC2425M10LS500P demo board performance

Table 4 – RF Performance overview

Freq [MHz]	Gmax [dB]	Pout@Gmax [W]	P1dB [W]	P2dB [W]	Effmax [%]	Pout@Effmax [W]	Eff P1dB [%]	Eff P2dB [%]
2400	15.5	392.5	539.9	569.9	69.2	546.1	69.2	69
2450	15.9	388	515	544.1	68.8	517.7	68.8	68.6
2500	15.9	329.7	461.1	492.8	67.6	486	67.4	67.5

8. User Guide

8.1 Biasing

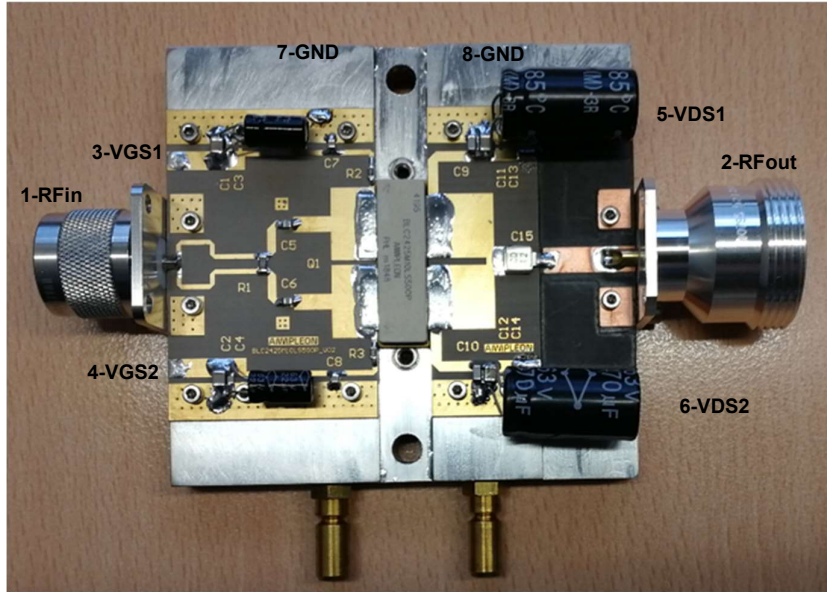


Figure 3 – BLC2425M10LS500P demo board pin configuration

Table 5 – Pin description

Symbol	Pin	Description
RF _{IN}	1	RF input
RF _{OUT}	2	RF output
V _{GS1}	3	Gate-source voltage
V _{GS2}	4	Gate-source voltage
V _{DS1}	5	Drain-source voltage
V _{DS2}	6	Drain-source voltage
GND	7, 8	Negative supply terminal for V _{GS} and V _{DS} respectively

8.2 Bill of Materials

Table 6 – Bill of Materials

Part	Description	Part number	Value/Remark
<i>C1, C2</i>	<i>Multilayer ceramic chip capacitor</i>	<i>GRM32RR71H105KA01L</i>	<i>1µF/50V</i>
<i>C3, C4, C11, C12</i>	<i>Multilayer ceramic chip capacitor</i>	<i>08051A102JAT2A</i>	<i>1nF, 100V</i>
<i>C5, C6, C7, C8</i>	<i>Multilayer ceramic chip capacitor</i>	<i>ATC800A</i>	<i>22pF</i>
<i>C9, C10</i>	<i>Multilayer ceramic chip capacitor</i>	<i>ATC800B</i>	<i>22pF</i>
<i>C13, C14</i>	<i>Multilayer ceramic chip capacitor</i>	<i>C1210</i>	<i>4.7µF/50V</i>
<i>C15</i>	<i>Mica capacitor</i>	<i>MIN02</i>	<i>12pF</i>
<i>R1</i>	<i>Chip resistor</i>	<i>R1206</i>	<i>100R</i>
<i>R2, R3</i>	<i>Chip resistor</i>	<i>R0603</i>	<i>10R</i>
<i>ELCO1, ELCO2</i>	<i>Input Electrolytic capacitors</i>		<i>22uF/63V</i>
<i>ELCO3, ELCO4</i>	<i>Output Electrolytic capacitors</i>		<i>470uF/63V</i>
<i>T1</i>	<i>LDMOS transistor</i>	<i>BLC2425M10LS500P</i>	<i>Ampleon</i>
<i>Input PCB</i>	<i>Rogers TC350</i>		<i>30 mil thickness</i>
<i>Output PCB</i>	<i>Rogers TC350</i>		<i>30 mil thickness</i>
<i>Final Output PCB</i>	<i>RT/Duroid 5880</i>		<i>62 mil thickness</i>

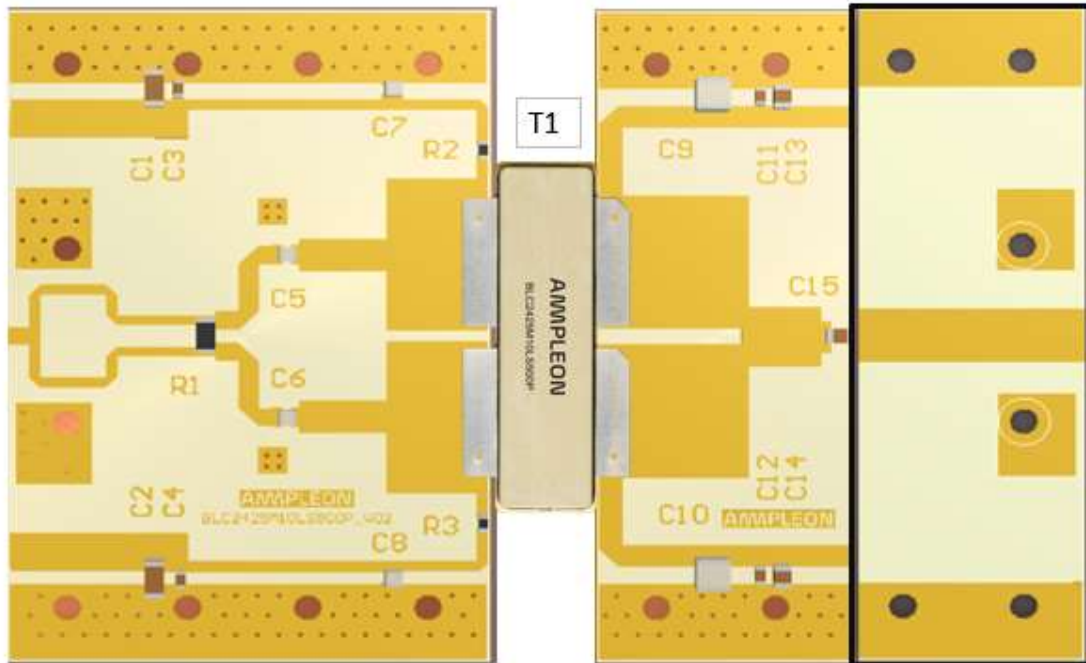


Figure 4 – BLC2425M10LS500P demo board component description

8.3 Temperature behavior

For operation of this demo board water cooling should be applied. Water temperature should not exceed 45 °C.

8.4 Device markings

Table 7 – Module specifics

Parameter	Value
Manufacturer	Ampleon
Device	BLC2425M10LS500P
Comments	Engineering sample

9. Legal information

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