

# AR191188

BLF974P, 230-236 MHz

v1.0 – December 6, 2019

AMPLEON

Application Report

## Document information

**Status** v1.0

**Abstract** Measurement results of a BLF974P demo design optimized for 230-236 MHz.

## 1. Revision History

Table 1 – Report revisions

| Revision | Date       | Description      | Author |
|----------|------------|------------------|--------|
| 1.0      | 2019.12.06 | Initial document |        |

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5. General description

This report presents the measurement results of the BLF974P in a demoboard optimized for 230-236 MHz, with transistor pressed down.

Measurements have been performed on a dedicated demo-circuit, matched to 50 Ω at input and output.

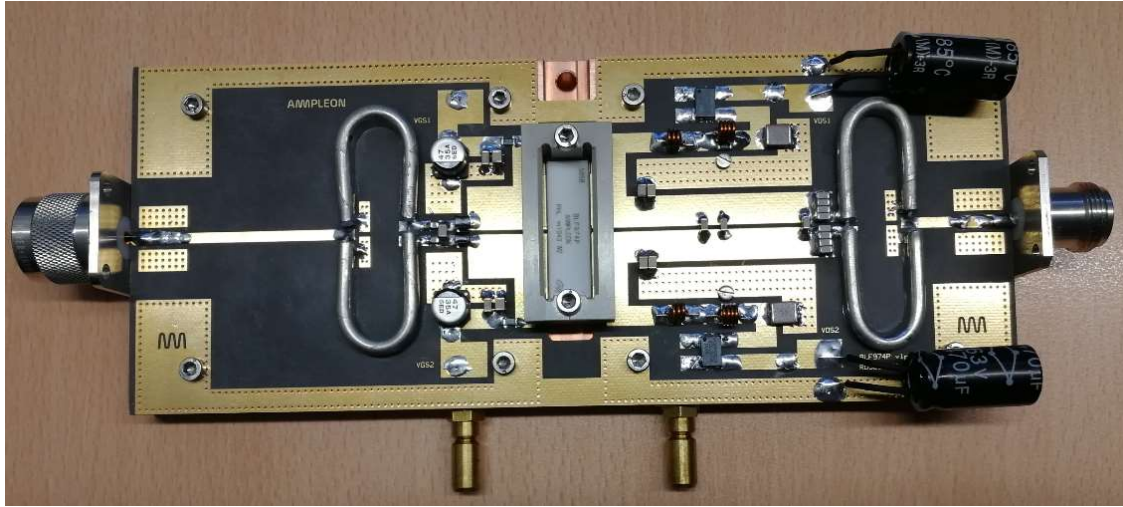


Figure 1 – Demo view of the BLF974P

Table 2 – Test circuit information

| Parameter            | Description   | Unit |
|----------------------|---|------|
| Input Laminate Type  | RT/duroid 5880  |      |
| Output Laminate Type | RT/duroid 5880  |      |
| Laminate thickness   | 0.79  | mm   |
| Overall dimensions   | 200.3 x 80  | mm   |
| IN PCB dimensions    | 95 x 80 (removing extended input 50 Ohm line: 50 x 80 mm) | mm   |
| OUT PCB dimensions   | 95 x 80   | mm   |
| Cooling type         | Indirect water cooling                                    |      |
| Device Package       | SOT539  |      |

## 6. RF characteristics

Table 3 – RF characteristics

Test signal: CW-Pulsed, PW=500uS, DC=25% ; RF performance at  $V_{DS}=50V$ ; Total  $I_{Dq}=1.3A$ ;  
 $T_{amb}=21^{\circ}C$ ;  $T_{cooling\ water}=25^{\circ}C$

| Symbol   | Parameter            | Conditions                             | Typical | Unit |
|----------|----------------------|--|---------|------|
| f        | Frequency            |  | 230-236 | MHz  |
| $V_{DS}$ | Drain-source voltage |  | 50      | V    |
| $V_{GS}$ | Gate-source voltage  | $I_{Dq} = 750mA \times \text{section}$ | 2       | V    |
| $G_p$    | Power gain           | $P_{1dBcp} = 649.8W$                   | 26.4    | dB   |
| $\eta_D$ | Drain efficiency     | $P_{1dBcp} = 649.8W$                   | 76.7    | %    |

## 7. Performance Details

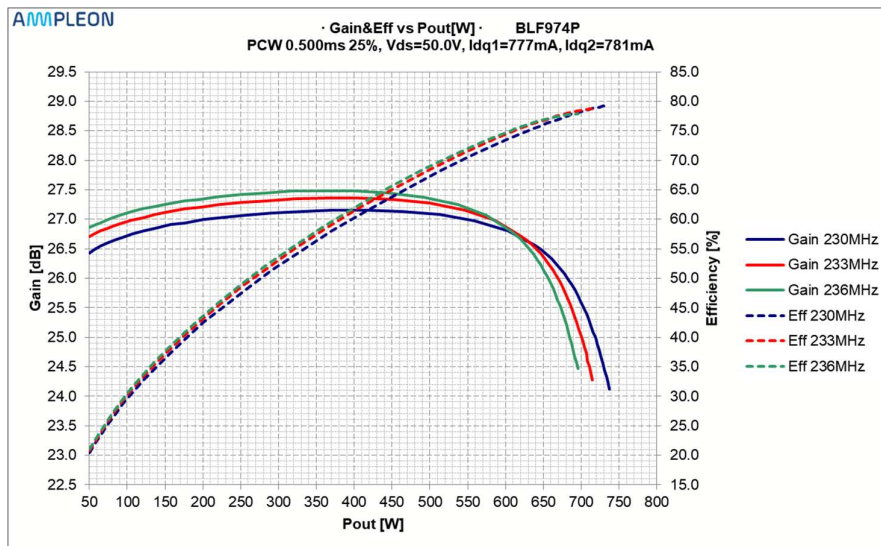


Figure 2 – BLF974P demo board performance

Table 4 – RF Performance overview

| Freq [MHz] | Gmax [dB] | Pout@Gmax [W] | P1dB [W] | P2dB [W] | P3dB [W] | Effmax [%] | Pout@Effmax [W] | Eff P1dB [%] | Eff P2dB [%] | Eff P3dB [%] |
|------------|-----------|---------------|----------|----------|----------|------------|-----------------|--------------|--------------|--------------|
| 230        | 27.2      | 416           | 673.1    | 714.2    | 736.5    | 79.3       | 737.2           | 77.1         | 78.7         | 79.3         |
| 233        | 27.4      | 406.1         | 649.8    | 691.1    | 713.5    | 78.7       | 714.9           | 76.7         | 78.3         | 78.7         |
| 236        | 27.5      | 358.3         | 632.5    | 673.2    | 695.1    | 77.8       | 695.5           | 76.2         | 77.5         | 77.8         |

8. Transistor Lumped Element equivalent model

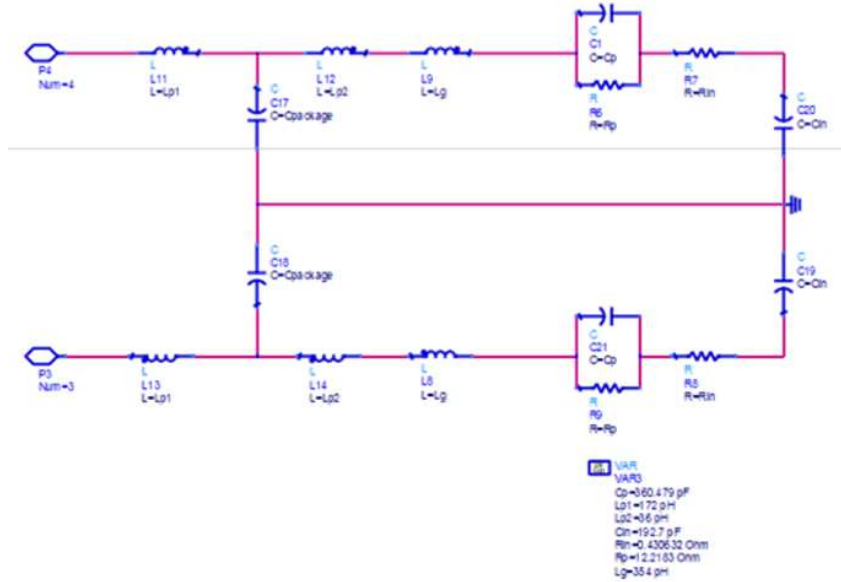


Figure 3 – Transistor Lumped Element Equivalent: Input

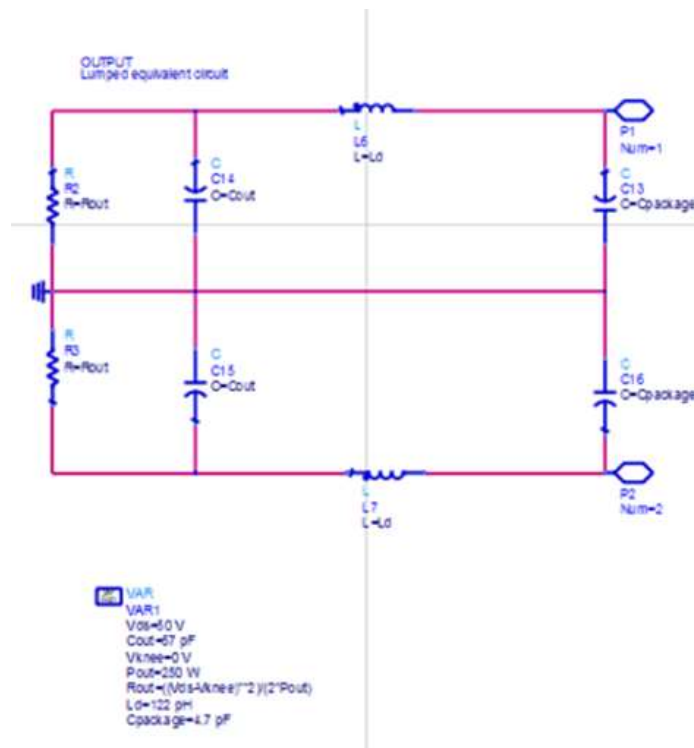


Figure 4 – Transistor Lumped Element Equivalent: Output

9. User Guide

9.1 Biasing

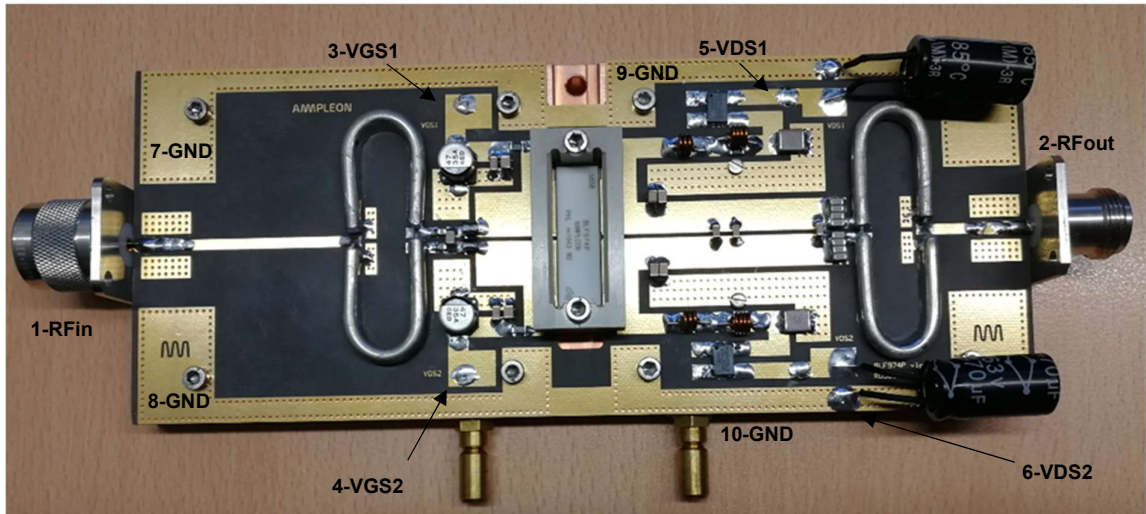


Figure 5 – BLF974P demo board pin configuration

Table 5 – Pin description

| Symbol     | Pin   | Description                           |
|------------|-------|---------------------------------------|
| $RF_{IN}$  | 1     | RF input                              |
| $RF_{OUT}$ | 2     | RF output                             |
| $V_{GS1}$  | 3     | Gate-source voltage – Section A       |
| $V_{GS2}$  | 4     | Gate-source voltage – Section B       |
| $V_{DS1}$  | 5     | Drain-source voltage – Section A      |
| $V_{DS2}$  | 6     | Drain-source voltage – Section B      |
| GND        | 7, 8  | Negative supply terminal for $V_{GS}$ |
| GND        | 9, 10 | Negative supply terminal for $V_{DS}$ |

9.2 Bill of Materials

Table 6 – Bill of Materials

| Part                         | Description                       | Value                | Part number /Remark           |
|------------------------------|-----------------------------------|----------------------|-------------------------------|
| C1, C2                       | Multilayer ceramic chip capacitor | 47pF                 | ATC600F                       |
| C3                           | Multilayer ceramic chip capacitor | 62 pF                | ATC100B soldered on the side  |
| C4, C5                       | Multilayer ceramic chip capacitor | 1 nF                 | ATC100B                       |
| C6, C7                       | Multilayer ceramic chip capacitor | 4.7 uF               | GRM31CC72A475KE11L Murata     |
| C8                           | Multilayer ceramic chip capacitor | 15 pF                | ATC800B soldered on the side  |
| C9                           | Multilayer ceramic chip capacitor | 20 pF                | ATC800B soldered on the side  |
| C10                          | Multilayer ceramic chip capacitor | 4.7 pF               | ATC800B soldered on the side  |
| C11, C12, C13, C16, C17, C18 | Multilayer ceramic chip capacitor | 10 pF                | ATC800B soldered on the side  |
| C14, C15                     | Multilayer ceramic chip capacitor | 20 pF                | ATC800B soldered on the side  |
| C19, C20                     | Multilayer ceramic chip capacitor | 51 pF                | ATC100B soldered on the side  |
| C21, C22                     | Multilayer ceramic chip capacitor | 1.2 pF               | ATC100B soldered on the side  |
| C23, C24                     | Multilayer ceramic chip capacitor | 4.7uF / 100V         | C3225X7S2A475K200AE           |
| C25, C26                     |                                   | 470 uF / 63V         | Electrolytic capacitor        |
| C28, C29                     |                                   | 47 uF, 63V           | Electrolytic capacitor        |
| L1, L2                       | Chip inductor                     | 2.5 nH               | A01TKLB Coilcraft             |
| L3, L4                       | 3 turn 1 mm copper wire           | D=3mm, length=3.3 mm |                               |
| L5, L6                       | 4 turn 1 mm copper wire           | D=3mm, length=4 mm   |                               |
| TL                           | Soldered Microstrip line          |                      |                               |
| R1, R2                       | Chip Resistor                     | 20Ω                  | 0.6W SMD 1206                 |
| R3, R4                       | Chip Resistor                     | 2x3.6Ω               | 0.6W SMD 1206                 |
| R5, R6                       | Shunt Resistor                    | 0.01Ω                | Ohmite/FC4L110R010FER         |
| Balun B1, B2, B3, B4         | Coaxial Line Zc=50, 58 mm         |                      | HUBER+SUHNER EZ-141-AL-TP-M17 |
| T1                           | LD MOS transistor                 | BLF974P              |                               |
| Input PCB                    | RT/duroid 5880                    | H=0.79mm, Cu=35um    | Er=2.2                        |
| Output PCB                   | RT/duroid 5880                    | H=0.79mm, Cu=35um    | Er=2.2                        |



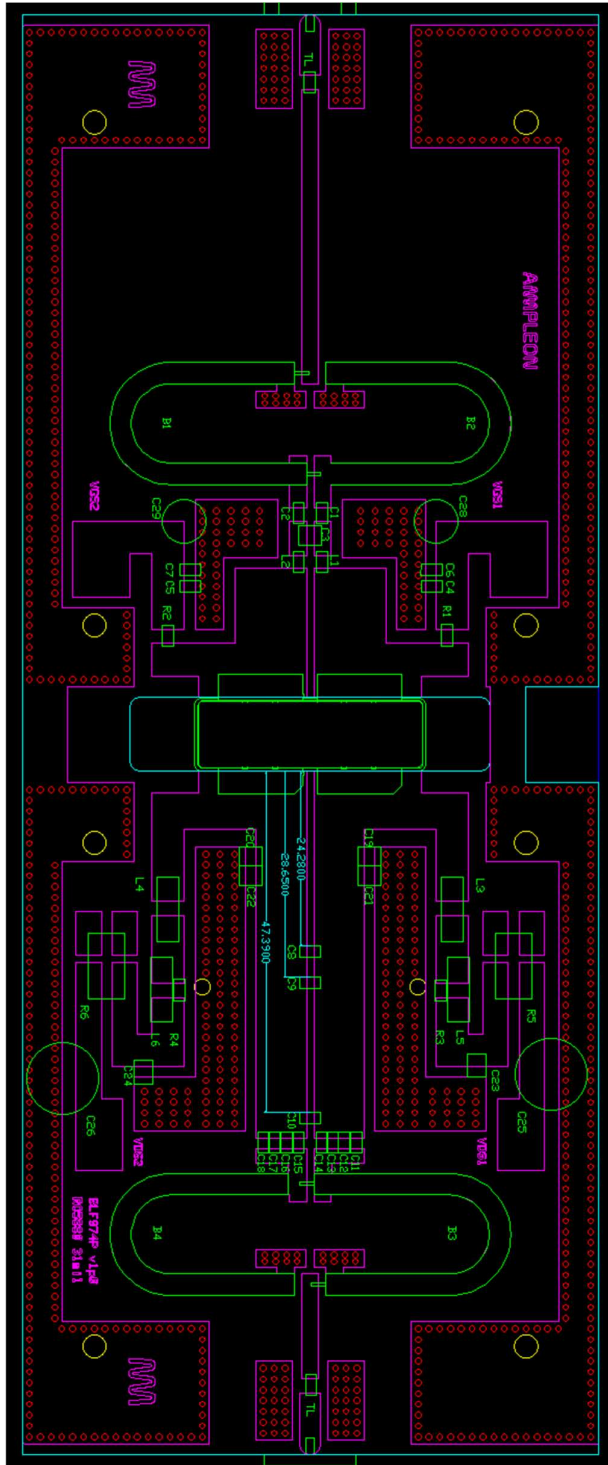


Figure 6 – BLF974P application board component description and position

### 9.3 Temperature behavior

For operation of this demo board water cooling should be applied.

### 9.4 Device markings

*Table 7 – Module specifics*

| Parameter    | Value              |
|--------------|--------------------|
| Manufacturer | Ampleon            |
| Device       | BLF974P            |
| Comments     | Engineering sample |

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### 10.1 Definitions

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