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Thermal characteristics of ART LDMOS power transistors

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Application note

Document information

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Keywords	Thermal Resistance, Thermal Impedance, RC network, LDMOS, ART.
Abstract	This application note presents the thermal characterization and modeling methodology used on Ampleon's ART LDMOS transistors. The accurate, systematic, and consistent methodology for thermal characterization and modeling is essential in predicting the junction temperature and evaluating the transistor's lifetime.

Revision history

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1. Introduction

The laterally diffused metal oxide semiconductor (LDMOS) power device offers exceptional RF performance while increasing the efficiency and reliability of power amplifiers. Ampleon introduced the first family of LDMOS devices based upon Advanced Rugged Technology (ART), built to handle the toughest conditions in industrial, scientific, and medical applications. The ART LDMOS offers higher efficiency and lower power dissipation compared to other LDMOS transistors, but still operates at high power with high heat dissipation. To ensure safe operation, a thorough thermal characterization and model are necessary. In targeted applications, thermal design is crucial for improving system reliability and delivering cost-efficient, energy-saving RF performance. This document focuses on the thermal characterization of ART LDMOS.

2. Methodology for thermal evaluation

Ampleon's methodology for thermal evaluation and product datasheet of ART LDMOS follows the process shown in Figure 1. The process begins with finite element thermal modeling during the design phase and thermal characterization in the production phase. Using a calibrated customized thermal model, device design parameters are predicted and optimized within the thermal budget. After sample fabrication, the maximum surface temperature of the die is measured using infrared (IR) thermography and $Rth_{(j-c)}$ is calculated based on MIL-STD-833 [1]. Transient thermal measurement, as per JESD 51-14 [2], is used to extract thermal impedance during pulse operation. The fitted thermal RC network from the transient response is incorporated into device modeling and system-level thermal modeling. The wear out reliability of LDMOS devices is dominated by electromigration and can be calculated using the MTF tool as a function of junction temperature. The constant failure rate (FIT) is calculated using the average junction temperature of the active die(s).

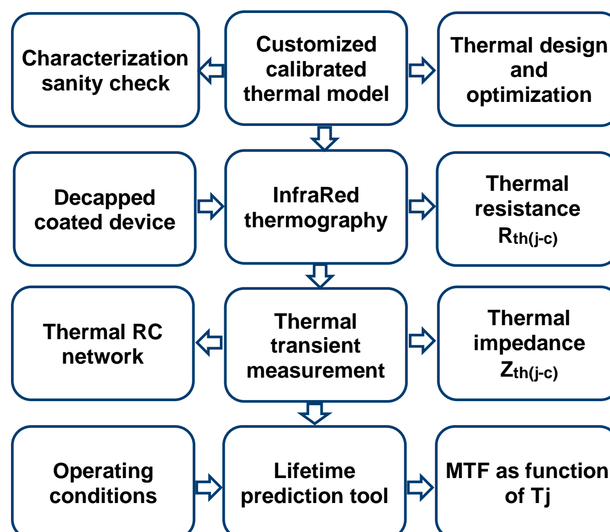

Figure 1. Methodology for ART LDMOS thermal evaluation

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In addition to the above-shown ART LDMOS thermal evaluation methodology deliverables, Ampleon provides for some transistors access to the internal die temperature by integration of a thermal sensor. This thermal sensor is located near to the maximum physical junction temperature point and converts the die temperature into an equivalent electrical current that is made available to the user by a dedicated package pin.

Due to the availability of the sensed die temperature, this sensor can be used to control and/or monitor the die temperature and enables multiple use cases as for e.g., protection of the transistor from thermal damages, indication of dissipated power, lifetime control by ongoing measurements or degradation of the flange solder joint.
The advantages of an integrated sensor against an external sensor are more accurate, faster response to junction temperature changes, easy interconnection and assembly, and a smaller application footprint.

3. Definition of Rth and Zth

The junction-to-case thermal resistance ($R_{th(j-c)}$) is a measure of the ability of a transistor to dissipate heat from the operating active area to the outside surface of the package (case). The traditional MIL-STD-833 [1] standard requires the determination of the maximum junction temperature (T_j), the case temperature (T_c), and the dissipation power (P_D). The junction-to-case thermal resistance is then calculated using

$$R_{th(j-c)} = \frac{T_j - T_c}{P_D}$$

where the peak dissipation power in the given operating condition is calculated using:

$$P_D = P_{in} + P_{DC} - P_{out}$$

where P_{in} and P_{out} are the RF input and output power and P_{DC} is the DC input power.

The result obtained is referred to as "steady-state $R_{th(j-c)}$", as it is determined under steady-state conditions and is based on the temperature difference along the heat flow path from the junction to the case. Measuring it can be challenging as it requires accurately measuring the package case temperature with a thermocouple while the case surface is in close contact with a heat sink. Additionally, for visible access to the die surface (Tj is close to the surface), samples need to be manually prepared by removing the lid or plastic encapsulant and coating with a uniform high-emissivity paint. This can lead to different measurement set-ups and samples producing deviant values.

The JESD 51-14 standard proposed method is based on transient measurements of the average junction temperature under different cooling conditions at the heat sink case surface. It does not require knowledge of the case temperature and does not involve sample preparation, thus eliminating errors associated with these factors

The thermal impedance or $Z_{th(j-c)}(t)$ of a transistor which is heated with constant power P_D starting at time t = 0 while its case surface is properly attached to the heatsink shall be defined as

$$Z_{th(j-c)} = \frac{T_j(t) - T_j(0)}{P_D}$$

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i.e., the thermal impedance equals the time-dependent change of the junction temperature $T_j(t)$ divided by the heating power. If the cooling condition at the package case is changed, this should have no influence on the thermal impedance until the temperature starts to increase at the package case. A measurement with different contact resistance however changes the total thermal resistance at steady-state and therefore separates the impedance curves of different measurements starting from the point where the external contact resistance contributes, which can be identified as the package case interface.

4. InfraRed thermography for $R_{th(j-c)}$

Infrared thermography is the most commonly used technique to determine the maximum junction temperature of LDMOS power amplifier devices during operation. Ampleon's datasheets for ART LDMOS devices also present $R_{th(j-c)}$ based on MIL standard, to enable customers to apply their own system-level IR measurement data and compare it to thermal data from competitors' datasheets.

An image and schematic of the IR setup are shown in Figure 2. The package is attached to the baseplate with a proper thermal interface to ensure good thermal and electrical contact for the package case and leads. The RF matching boards for input and output are placed on the baseplate. The baseplate is temperature-controlled using a liquid cooling system to accurately set the desired case temperature of the transistor. The case temperature (T_C) of the package is measured by a spring-loaded thermocouple, which is mounted within the baseplate. For visible access to the die surface, the lid or plastic encapsulant is removed before IR imaging. The exposed die is coated with a fixed high emissivity coating. Once the supply voltage and bias are applied to the circuit, the RF signal is switched on and set to the required RF output power level. The IR scan image is captured and data is recorded when all settings are stable, along with all corresponding electrical data.

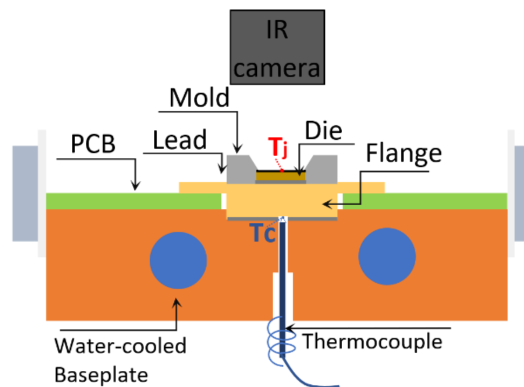

Figure 2. IR measurement setup with measuring the maximum junction and case temperature based on MIL-STD-883E

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5. Thermal transient test for $Z_{th(j-c)}$ and thermal network

Systems that employ power amplifiers often operate in pulse modes rather than continuous wave (CW); thus, it is important to understand the transient response of a device. The thermal impedance can be measured using the Electrical Test Method (ETM) based on the JESD 51-1 standard [3]. The ETM uses a temperature-sensitive parameter (TSP) to sense the change in temperature of the junction operating area when electrical power is applied to the device-under-test (DUT). The most commonly used TSP is the voltage drop across a forward-biased diode. The relationship between the temperature sensing diode forward voltage and junction temperature is determined by performing a calibration. The Transient Dual Interface (TDI) method is used to identify the back of the package without measuring the case temperature. Figure 3 shows a test environment with and without using paste on the back of the package. The DUT is placed on top of a baseplate whose temperature is controlled with a coldplate.

The procedure for measuring is to supply a constant heating current (Ih) to the diode in the DUT to raise the temperature of the die. Once the junction temperature is high and stable, the supply of heating current is stopped, and the measurement is quickly switched to the forward voltage current. Data is recorded until the forward voltage reaches low-temperature steady state, then converted to temperatures based on the calibration curve. The transient cooling curve data is post-processed into usable information like pulse thermal resistance and RC thermal network.

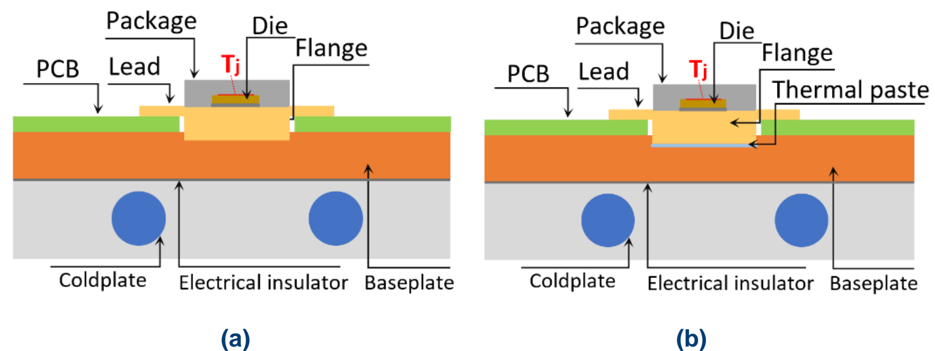

Figure 3. Test stack-up for the TDI method, taking two types of measurements: (a) “Without” and (b) “with” thermal paste between the DUT and the baseplate.

The structure-function expresses the heat transfer path of the device structure as a one-dimensional thermal circuit of thermal resistance and thermal capacitance and enables the thermal structure of the device to be visualized. Figure 3a shows the measurement results of sample ART2K0FE with and without thermal paste converted to structure functions and superimposed. It can be seen that paste reduces the thermal resistance and the branching point represents the interface between the case and the thermal paste, meaning that the thermal resistance from the junction to the branching point is Rth,(j-c) in accordance with JESD51-14. Since this method is based on a temperature-sensitive electrical signal, the response represents the temperature of the whole active area which is lower than the hot-spot temperature. Figure 3b shows the thermal resistance vs. pulse time in a log scale for several duty cycles. The thermal resistance in CW time (t > 1sec) scaled to IR measurement to represent the maximum temperature.

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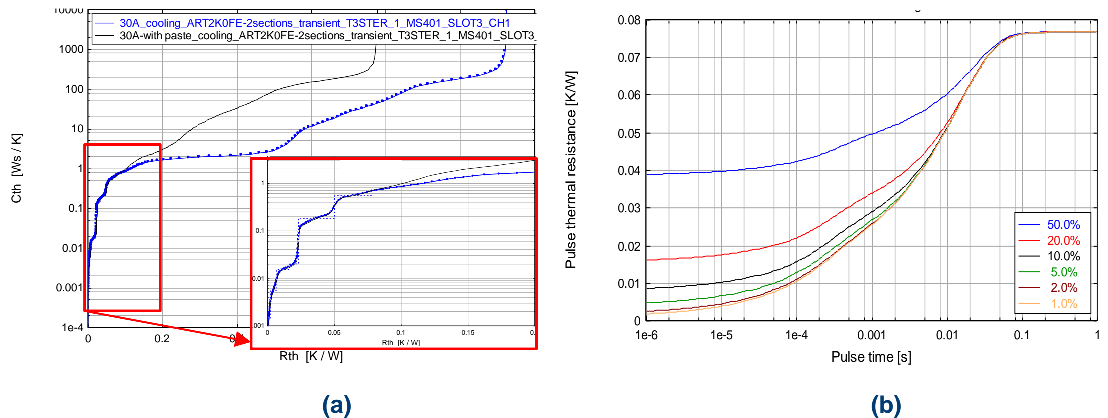
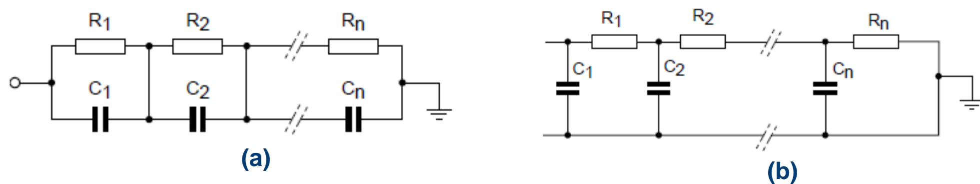


(a) (b)

Figure 4. (a) Structure function with separation point and (b) pulse thermal resistance of ART2K0FE device

The structure function obtained from the transient thermal measurement is represented as a Foster and Cauer RC network, as shown in Figure 5. Foster models are derived by fitting a curve, and the R and C values do not correspond to geometrical locations on the physical device. Therefore, these values cannot be calculated from device material constants and cannot be divided or interconnected, for example, by connecting the RC network of a heat sink. A Cauer model can be derived from a Foster model, and they are equivalent representations of the device thermal performance. The Cauer model also consists of an RC network, but the thermal capacitances are all connected to the thermal ground, i.e., ambient temperature. The nodes in the Cauer model have a physical meaning and allow access to the temperature of the internal layers of the semiconductor structure. Both Foster and Cauer RC thermal models allow application engineers to perform fast calculations of the transient response of a package to complex power profiles.



(a) (b)

Figure 5. (a) Foster and (b) Cauer RC thermal models

6. Thermal model for design and validation

Automated thermal modeling can shorten design time, standardize processes, and provide consistent and reliable results for sanity check of measurements. The 3D FEM thermal model with a customized workflow in Ansys software generates geometry from die layout and package specifications. A refined, independent multi-zone mesh and heat load, with a boundary condition as the constant temperature on the heat sink, are assigned. The steady-state thermal analysis presents the temperature distribution

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(Figure 6) on the device for Rth estimation, and transient thermal analysis is used for Zth extraction.

The thermal model is calibrated on material properties (specifically thin layers) and geometry with accurate IR measurement on various steady heat dissipations, in addition to transient electrical-based measurement. The calibrated model is benchmarked to ensure versatility and range of applicability. Due to the nonlinearity of material properties (temperature-dependent thermal conductivity of Silicon), the thermal resistance slightly depends on heat dissipation and case temperature.

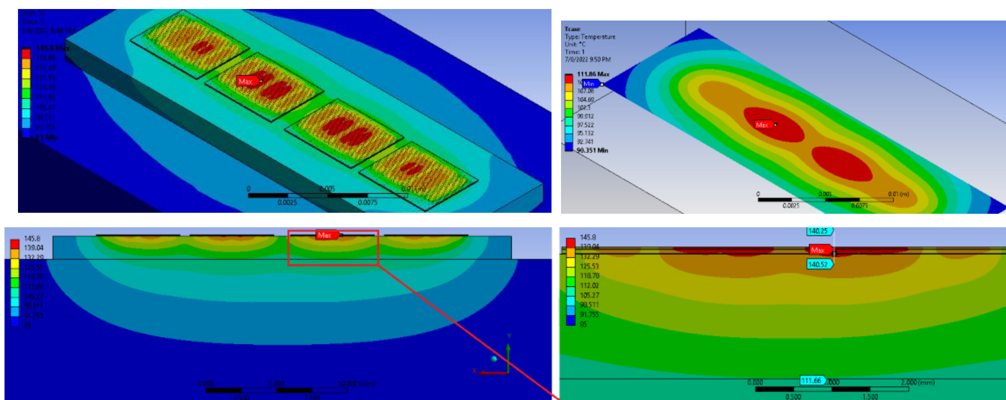

Figure 6. Thermal model of ART2K0FE device

7. Lifetime calculation

Junction temperatures can be used to estimate lifetimes. For LDMOS transistors the MTF (mean time to failure) can be calculated with the online tool. An example in Figure 7 shows the MTF calculation for the ART2K0FE with a power loading of 2000W. The MTF tool uses the estimate of the maximum junction temperature (as determined with IR). The calculated MTF should be above the required application lifetime with margin (rule of thumb factor 4).

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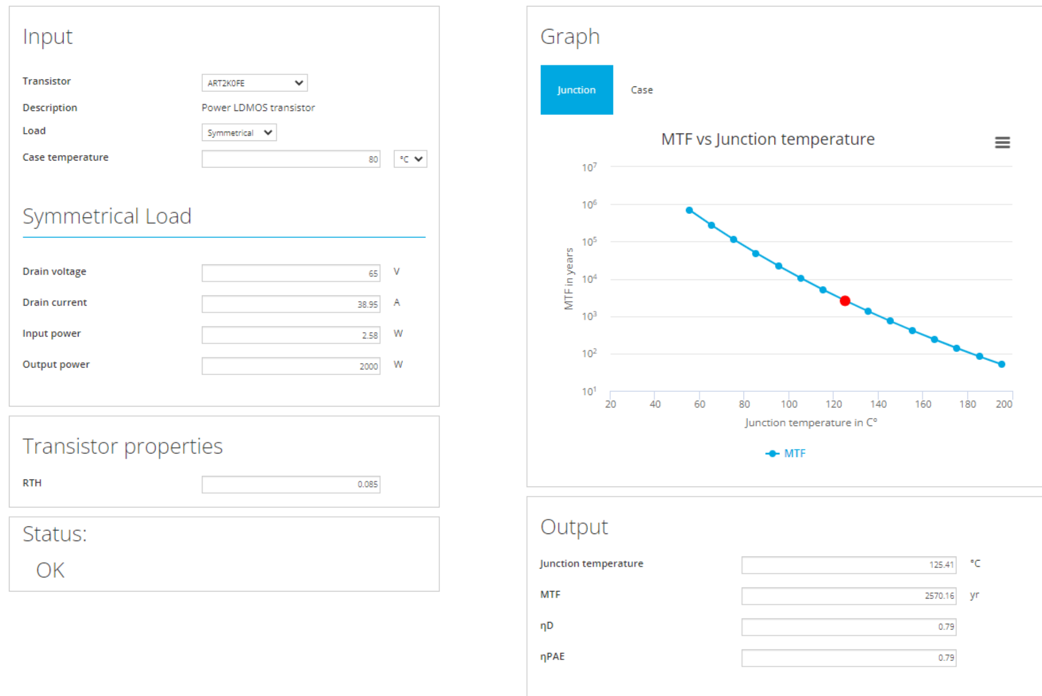

Figure 7. RF Power Lifetime Calculator ART2K0FE available on AMPLEON website

For calculating the failure rate (FIT) of the transistor, the average junction temperature over the active die(s) is used. This can be calculated with the Rthj-c as determined with the JESD51-1 method. Figure 8 shows the failure rate curve for the ART2K0FE transistor consisting of 4 active dies as a function of the junction temperature. With an average junction temperature of 125°C the failure rate is about 4 FIT. The failure rate can be used for calculating the failure rate on module or system level.

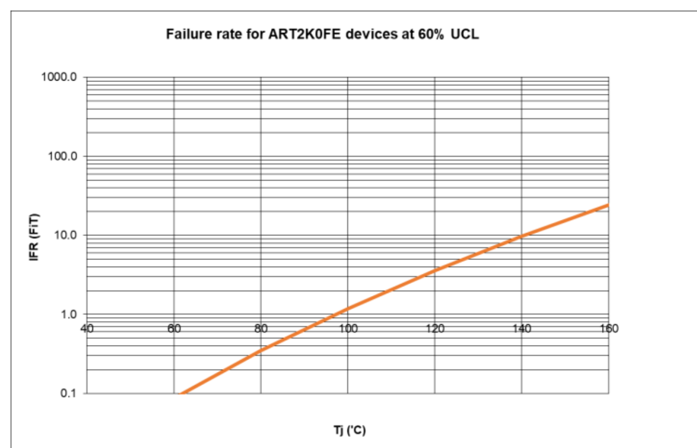

Figure 8. FIT versus junction temperature for the ART2K0FE

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