# AN221012

## Thermal characteristics of GaN power transistors

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Application note

### Document information

| Info | Content |
|---|---|
| **Keywords** | Thermal Resistance, Characterization, Simulation, GaN. |
| **Abstract** | This application note outlines the methodology for thermal evaluation of high-power GaN RF power amplifier devices. Establishing an accurate, systematic, and consistent approach to thermal characterization and modeling is essential for predicting surface and channel temperatures, as well as assessing the transistor’s lifetime. |

## Revision history

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|---|---|---|
| AN221012#1 | 20220310 | Initial version. |
| AN221012#2 | 20240901 | Second version. |

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# 1. Introduction

To meet the increasing demands and requirements of modern radio frequency (RF) power amplifiers (PA), Gallium Nitride on Silicon Carbide (GaN on SiC) has emerged due to its high breakdown voltage, superior power density, high-frequency operation, and excellent thermal properties. With more power concentrated in a small area, RF designers face the growing challenge of maintaining a suitable thermal environment. The performance and reliability of power amplifiers are highly dependent on operating temperature. Therefore, an accurate, systematic, and consistent approach to thermal characterization and modeling is crucial for establishing a reliable system. This document explains the proposed methodology for the thermal evaluation of high-power GaN RF PA devices.

# 2. Thermal Challenge in GaN Devices

Device technology progress for power amplifiers has always focused on increasing power density and gain at higher speeds. The push for higher power density led to the migration from silicon (Si) to gallium arsenide (GaAs), and eventually to gallium nitride (GaN). Table 1 compares LDMOS with GaN technology from a thermal perspective. In GaN devices, with higher power, smaller footprints, and still lower efficiency, the power density is about five times higher than LDMOS. Theoretically, GaN can deliver a power density of more than 20 watts per millimeter (W/mm) at high frequencies, but its usage has been limited to 10 W/mm or less due to the elevated temperatures resulting from dissipating substantial amounts of heat in a compact volume.

Thermal management is the reason silicon carbide (SiC) is the substrate of choice for high-performance RF applications. SiC’s good thermal conductivity and high operating temperature are as important as the GaN semiconductor for delivering high RF power. Due to the intrinsic nature of GaN HEMTs, harsh and localized self-heating in the conducting channel may occur; this effect increases with the device power density and further compromises reliability. On one side, the electrical behavior of the traps is temperature-dependent. On the other side, additional phonon scattering in the channel degrades the 2DEG effective carrier mobility, leading to degraded DC and RF performance. Finally, since the relationship between lifetime and operating temperature is semi-exponential, even a small temperature reduction can significantly impact the lifetime of GaNs with thermally activated degradation mechanisms.

To manage the thermal challenge today, circuit designers spread the heat sources at the semiconductor surface, increasing the distance between device fingers or making those fingers smaller. However, the thermal challenge does not end at the chip level. The packaging engineer also plays a crucial role because the heat flux is higher at the chip-package interface. A good thermal interface between the chip and the package is essential to delivering all the RF power density the GaN device can provide. In conclusion, in GaN technology, thermal design is as important as electrical design.

Table 1. Comparison of LDMOS with GaN power amplifier from a thermal point of view

| Parameters | LDMOS | GaN |
|---|---|---|
| **Power density** | Low (0.5-3 W/mm) | High (4-10 W/mm) |
| **Thermal conductivity of substrate** | Si with low K (1.4 W/cm.K) | SiC with high K (3.5 W/cm.K) |
| **Nonlinearity** | Low T-dependency (conductivity reduction to 30 %) | High T-dependency (conductivity reduction to half) |
| **Operating temperature** | 50 - 125 °C | 125 - 225 °C |
| **Temperature gradient** | Low around heat source and from source to the junction | High around the heat source and from surface to channel |
| **Temperature measurement** | Simpler with less gradient and physics | More challenges with trapping |
| **Packaging** | Low temperature and gradient | Higher thermal stress with the high aspect ratio |
| **System-level cooling** | Bigger with air cooling | Smaller with higher case temperature |

# 3. Techniques for Channel Temperature Estimation

There are several techniques to estimate the channel temperature of GaN device under operating conditions. As presented in Table 2, each approach has its benefits and limitations based on the size and location of the temperature reading area, accuracy, time, and cost. The maximum channel temperature cannot be measured directly since it is optically hidden in most cases. Due to high heat flux in the active area of the device, a thermal gradient appears in the structure and temperature quickly decreases around the gate area. Therefore, the value of thermal resistance can be quite different depending on the method used to estimate the temperature of the device. Figure 1 shows a comparison of temperature values for sample GaN devices obtained using different methods. Depending on the method, the thermal resistance can be underestimated compared to the one corresponding to the peak maximum channel temperature.

Table 2. Benefit and limitations of various techniques for channel temperature estimation

| Technique | Benefits | Limitations |
|---|---|---|
| **InfraRed** | Fast and easy, most popular, and commonly used in industries | Averages the temperature over optical spot size (> 3 µm), Reading temperature on the surface, Needs sample preparation |
| **µRaman** | Measurement volume near to channel, High temporal (10ns) and spatial (> 0.5 µm) resolution | Slow for large devices, expensive, and needs expertise |
| **Temperature-sensitive electrical parameter** | Uses standard test equipment, provides transient response | Measure the average of the active area, TSEP degradation |
| **Thermal modeling** | Easy to use, all device areas accessible, Estimate maximum channel temperature in nanometer mesh size | Uncertainty in material properties, interfaces, and modeling assumption |

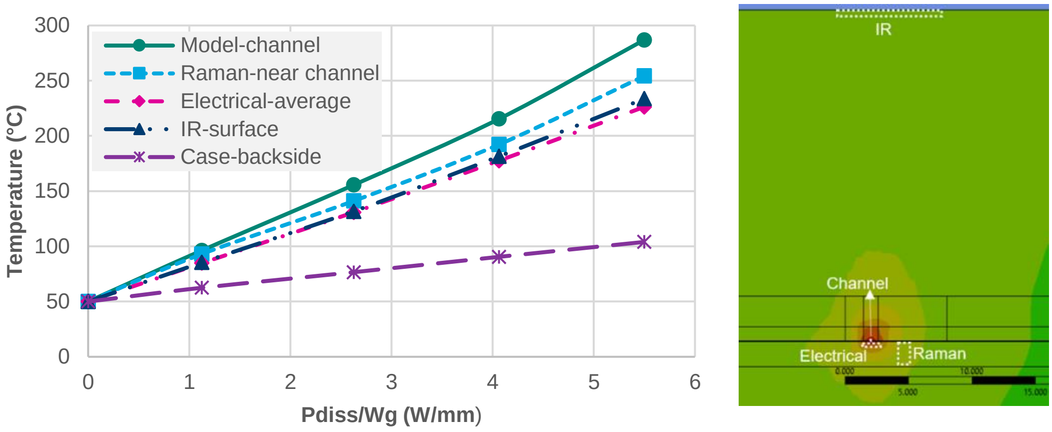


Figure 1. Comparison of various methods on the measurement of sample GaN device

## 4. Methodology for Thermal Evaluation

Ampleon’s methodology for GaN thermal evaluation and product datasheet follows the process illustrated in Figure 2. The methodology relies on a combination of thermal measurements and finite element thermal modelling. A customized thermal model is generated based on assumptions, inputs, and physics-based modelling. For each process technology, the thermal model is calibrated with accurate IR, µRaman, and transient measurements. The calibrated thermal model is then used to predict and optimize device design parameters within the allowed thermal budget.

After sample fabrication, the surface temperature of the die is measured using an IR camera. With a thermocouple on the back of the case, the thermal resistance from the surface to the case can be extracted. By correlating the thermal model with measurements, the channel temperature is calculated to extract the thermal resistance from the channel to the case. Transient thermal modeling and measurement are used for thermal impedance extraction during pulse operation. The fitted RC network from the transient response is incorporated into the thermal node in device modeling. The reliability of each device is calculated based on the operating conditions and the lifetime curve provided on the website. Results are represented by Median-Time-To-Failure as a function of channel temperature.

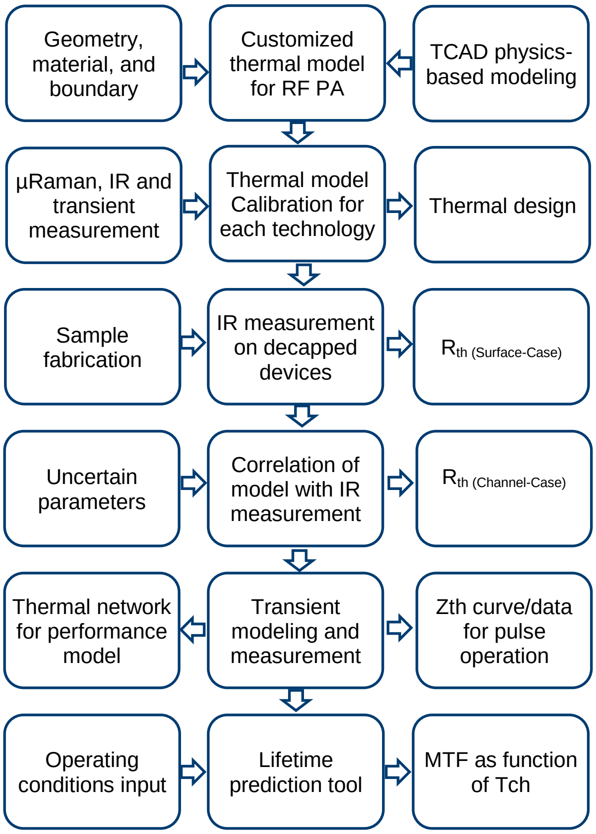


Figure 2. Methodology for GaN thermal evaluation

# 5. Definition of Rth

The junction-to-case thermal resistance $R_{th(J\text{-}C)}$ is a measure of the ability of a semiconductor device to dissipate heat from the operating portion of a semiconductor device to the outside surface of the package (case). During a GaN HEMT’s operation, peak temperature is reached within the channel where electrons flow from the drain to the source. For the GaN device, the junction temperature refers to the maximum temperature of the hottest channel (usually in the middle of a FET unit cell). So, the thermal resistance between channel to case is calculated as:

$$R_{th(ch-c)} = (T_{Ch} - T_C)/P_D$$

where $P_D$ is the dissipated power in the given operating condition and calculated as:

$$P_D = P_{in} + P_{DC} - P_{out}$$

where $P_{in}$ and $P_{out}$ are the RF input and output power and $P_{DC}$ is the DC input power. The channel temperature cannot be measured directly and is calculated based on the thermal model. The measurable temperature by IR camera is on the surface and thermal resistance between the surface to case is calculated as:

$$R_{th(s-c)} = (T_S - T_C)/P_D$$

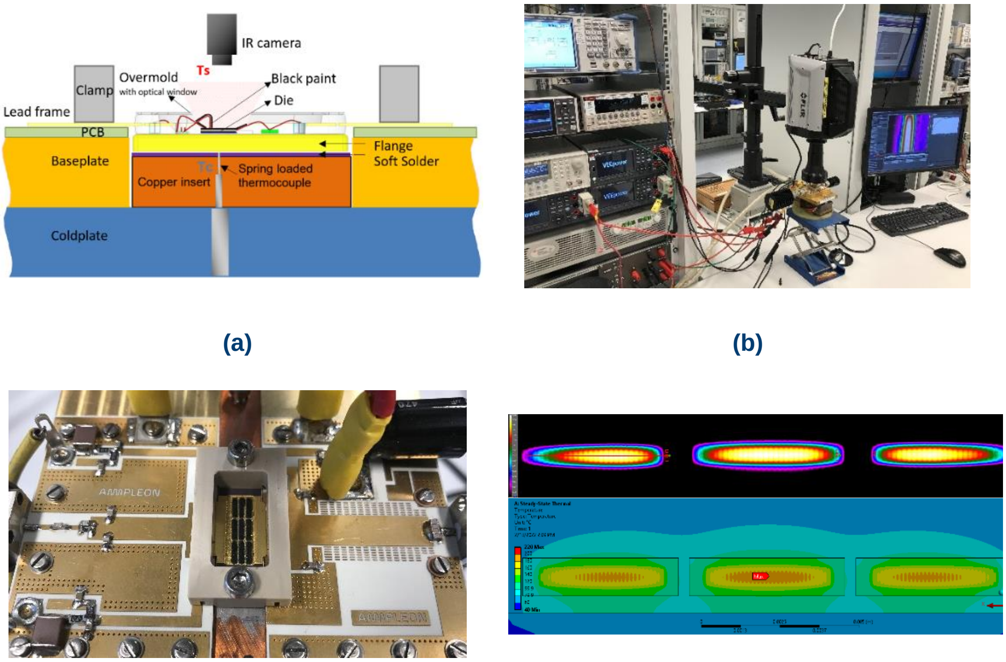
## 6. IR Measurement for $R_{th(s-c)}$

The most popular technique to determine the maximum surface temperature of a power amplifier device under operation is using infrared thermography. Ampleon datasheets present $R_{th(s-c)}$ based on IR measurements to enable application of customers' system-level IR measurement data, and comparison with the thermal data listed on competitors' datasheets.

An image and schematic of the IR setup is shown in Figure 3. The IR camera used is a FLIR8600 IR microscope with a 5-20 µm resolution, depending on the selected lens and extension ring. The RF amplifier consists of three parts. The package is attached to the center part (copper insert) using a clamp and proper thermal interface to ensure good thermal and electrical contact for the case and leads of the package. The RF matching boards for input and output are attached to two metal blocks adjacent to the copper insert part. All these parts are tightly pressed together and bolted down to the base plate with a proper thermal interface. The bottom (base) plate is temperature-controlled using a liquid cooling system to set the desired case temperature of the transistor accurately. The case temperature ($T_C$) of the package is measured by a spring-loaded thermocouple which is mounted within the heatsink and insert. The lid or plastic encapsulant is removed prior to IR imaging for visible access to the die surface. The exposed die is coated with a fixed high emissivity coating. Once the supply voltage and biasing are applied to the circuit, the RF signal is switched on and set to the required RF output power level. The IR scan image is captured, and data is recorded when all required settings are stable along with all corresponding electrical data. To confirm data, another measurement is done with the RF turned off. If the two Rth's (RF on and off) differ too much, the energy conducted across passives to the ground has likely been considered.

The thermal resistance is specified under a chosen operating condition and case temperature. One thermal resistance value is reported in the datasheet based on the maximum surface temperature ($T_s$) and total heat dissipation for single-stage transistor products with multiple dies. For multistage MMIC products, each stage is reported separately in the datasheet. Since thermal resistance is dependent on temperature, it is recommended to measure at various heat dissipations.

A minimum of five devices from multiple lots are IR scanned to produce enough data points, and the mean value is used for the datasheet. Due to dispersion in transistors and measuring instruments, the thermal resistance of a transistor should not deviate by more than 5%.



**(a)** **(b)**

**(c)** **(d)**

**Figure 3. (a) Schematic and (b) image of the IR setup, (c) sample test board, (d) measured and modeled sample.**

## 7. Thermal Model for $R_{th(ch-c)}$

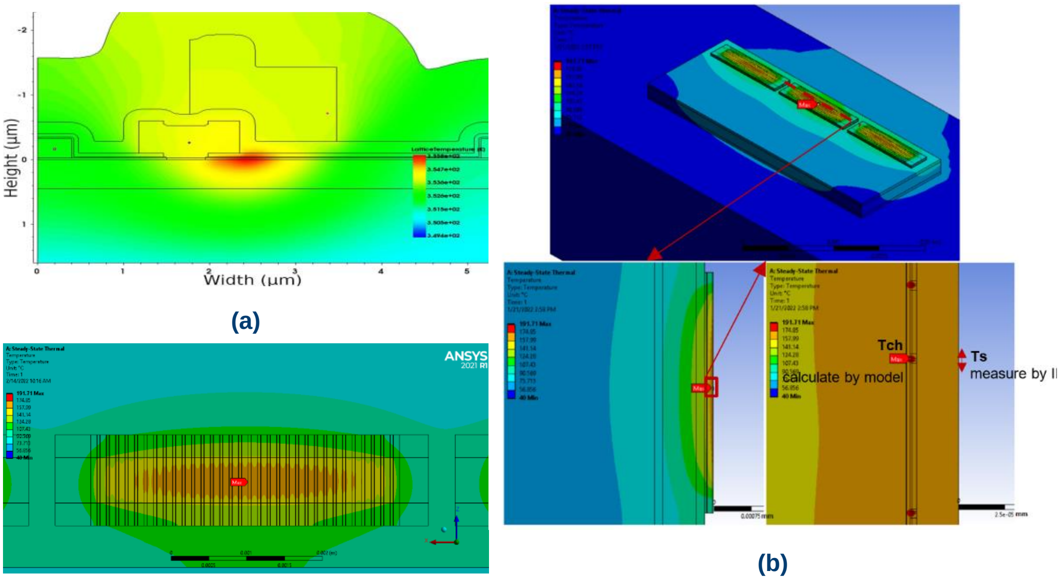
Accurate determination of the channel temperature relies on finite element thermal modeling correlated with measurement. Ampleon datasheets present $R_{th(ch-c)}$ based on thermal modeling to enable lifetime prediction and ensure the safe operation area of the device.

The automated thermal modeling process shortens design time, standardizes processes, and provides consistent and reliable results. The thermal model, with a customized workflow in Ansys software, generates geometry from the input of die layout and package specifications. Material properties of the basic model are defined based on datasheets and known published literature. Physics-based modeling of GaN devices is used to estimate the heat generation volume. Heat load and boundary conditions, such as constant temperature on the heat sink, are assigned. A refined and independent multi-zone mesh is generated, and the steady-state thermal analysis presents the temperature distribution on the device.

For each process technology, the thermal model is calibrated on material properties (specifically thin layers) and geometry with accurate IR and µRaman measurements on various steady heat dissipations, in addition to transient electrical-based measurements. The calibrated model is benchmarked to ensure versatility and range of applicability.

Correlation of simulation results to IR measurements is performed to ensure that the model predicts the real fabrication process. The model is created to reproduce the devices under the IR camera system. For all transistor applications, this includes a decapped packaged device with 30-50 µm black paint, with the bottom of the fixture having a fixed-temperature boundary condition based on the measured case temperature. The temperature of the model is calculated across an IR spatial resolution centered on the peak surface temperature. If the model data falls within the limits of the IR measurement data, the correlation between the model and IR data is successful. The channel temperature of the model is used to establish the thermal resistance of the device.

Due to the nonlinearity of material properties (GaN and SiC have temperature-dependent thermal conductivity), the thermal resistance slightly depends on heat dissipation and case temperature.



(a)

(b)

(c)

Figure 4. (a) TCAD modeling of gate finger transistor. (b) Simulated temperature distribution in sample GaN device on cross-section and (c) top view.

## 8. Transient Thermal Response

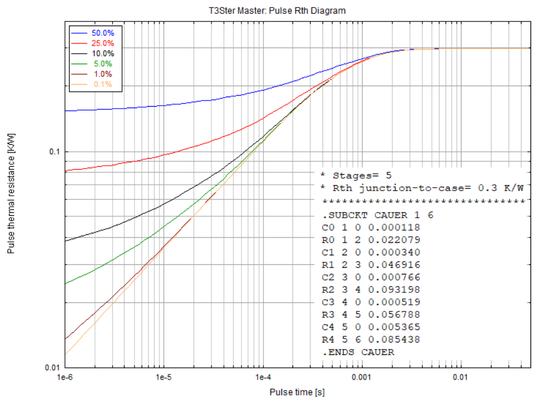
Systems employing power amplifiers usually operate in pulse modes rather than continuous wave (CW) modes, making it important to understand the transient response of a device through modeling and measurement. The thermal impedance can be modeled by transient thermal analysis and measured using a transient thermal tester based on the JESD 51-14 standard. The Transient Dual Interface (TDI) method is used to identify the back of the package without measuring the case temperature. Postprocessing the results derives the thermal resistance vs. pulse time on a log scale for several duty cycles.

For very short pulses, the power source can be interpreted as an effective source with power downscaled by the duty cycle. For very long pulses, the original heating curve is obtained again. This curve is extremely useful for producing data sheets for devices and designing switching-type power supplies.

To calculate the temperature rise within the junction of a power amplifier, the power and duration of the pulse and duty cycle delivered to the device must be known. If the power pulse is square, the thermal impedance can be read from the $Z_{th}$ chart. The product of this value with the power gives the temperature rise within the junction. If constant power is applied to the device, the steady-state thermal impedance ($R_{th}$) can be used.

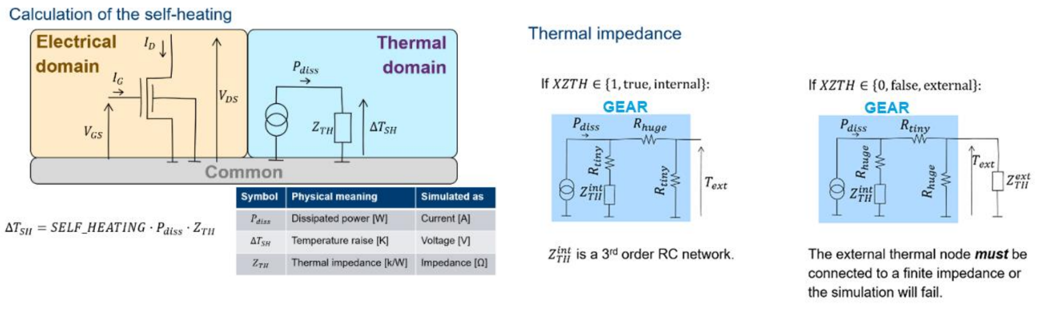
To represent $Z_{th}$ as a function of time, we can draw upon the thermal-electrical analogy and represent it as a series of RC charging equations or as an RC ladder. Zth can then be represented in a SPICE environment for ease of calculation of the junction temperature.

The impedance and thermal network can be used for modeling self-heating in device modeling. It calculates the instantaneous power provided through the gate and drain terminals to consider the temperature dependency of device characteristics. This circuit becomes effective if the model parameter XZTH is set to a non-zero value.



```
* Stages= 5
* Rth junction-to-case= 0.3 K/W
********************************
.SUBCKT CAUER 1 6
C0 1 0 0.000118
R0 1 2 0.022079
C1 2 0 0.000340
R1 2 3 0.046916
C2 3 0 0.000766
R2 3 4 0.093198
C3 4 0 0.000519
R3 4 5 0.056788
C4 5 0 0.005365
R4 5 6 0.085438
.ENDS CAUER
```

Figure 5. Pulse thermal impedance and network in sample GaN device



$$\Delta T_{SH} = SELF\_HEATING \cdot P_{diss} \cdot Z_{TH}$$

| Symbol | Physical meaning | Simulated as |
|---|---|---|
| $P_{diss}$ | Dissipated power [W] | Current [A] |
| $\Delta T_{SH}$ | Temperature raise [K] | Voltage [V] |
| $Z_{TH}$ | Thermal impedance [k/W] | Impedance [Ω] |

If $XZTH \in \{1, \text{true}, \text{internal}\}$:

$Z_{TH}^{int}$ is a 3rd order RC network.

If $XZTH \in \{0, \text{false}, \text{external}\}$:

The external thermal node ***must*** be connected to a finite impedance or the simulation will fail.

(a)

(b)

Figure 6. (a) Self-heating and (b) thermal impedance for considering temperature in device modeling

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