AN181008

BLF0910H9LS600

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AMPLEON

Application note

Document information

Info	Content
Keywords	BLF0910H9LS600, Gen9, LDMOS, RF Energy
Abstract	This application note provides general PCB design and transistor mounting guidelines to achieve optimum performance with the BLF0910H9LS600.

Revision history

Rev	Date	Description
AN181008#1	20180130	Initial document

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1. Introduction

The BLF0910H9LS600 transistor is one of Ampleon's high performance transistors and can deliver 600 W of output power at a gain of 19 dB and an efficiency higher than 66 % across the 902 MHz to 928 MHz band. This transistor should deliver this power at a rather limited footprint to enable cost effective designs in terms of physical dimensions. Above combination requires many design and mounting challenges to get the best performance out of this device. These challenges will be addressed in the reference layout and transistor mounting guideline chapters.

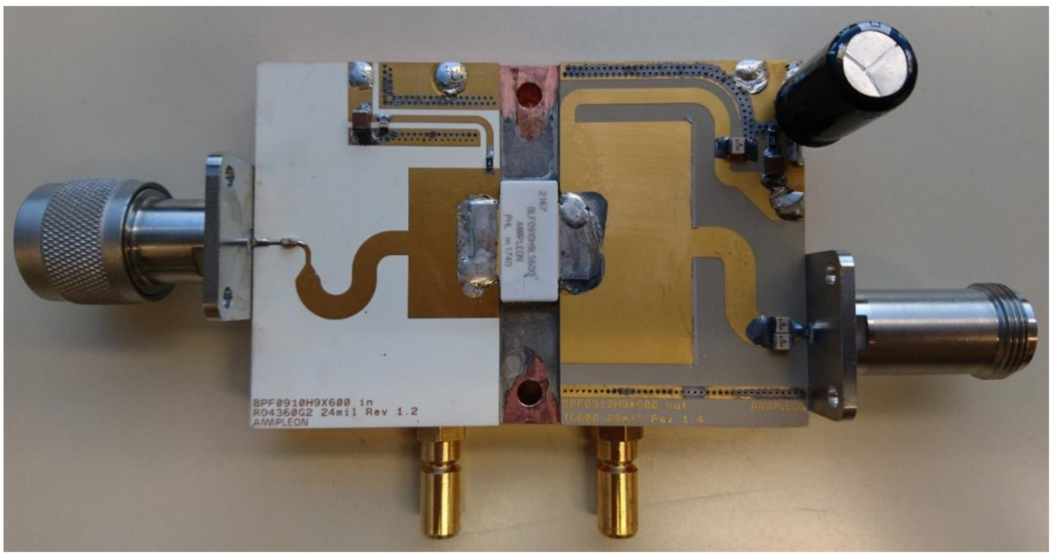

Figure 1. Demo board of the BLF0910H9LS600

2. RF characteristics

Table 1. RF characteristics

Test signal: CW; RF performance at V_{DS} = 50 V; Total I_{Dq} = 90 mA; T_{amb} = 25 °C

Symbol	Parameter	Conditions	Typ	Unit
f	Frequency		902 – 928	MHz
V_{DS}	Drain-source voltage		50	V
V_{GS}	Gate-source voltage	Total I_{Dq} = 90 mA	1.73	V
G_p	Power gain	P_L = 600 W	> 19	dB
η_D	Drain efficiency	P_L = 600 W	> 66	%

3. Reference layout

An inherent side effect of high power transistors is that the output impedance decreases for increasing output power. For the BLF0910H9LS600 this output impedance at the drain lead is 0.45+j0.2 Ohm. To transform this impedance to the 50Ohm system impedance, requires a careful design of the matching networks. One can imagine that any slight impedance variation has more impact on a low output impedance than that it would have on a higher impedance for lower power rated transistors. Therefore, the matching design should be as symmetric as possible on the drain lead to provide equal impedances to the internal LDMOS power dies. In this way, the power is delivered to the matching circuit in the most optimal way. This can be seen in Figure 2 where the reference layout of the BLF0910H9LS600 demo board is being showed. It's recommended to make both the input and output matching circuitry symmetric.

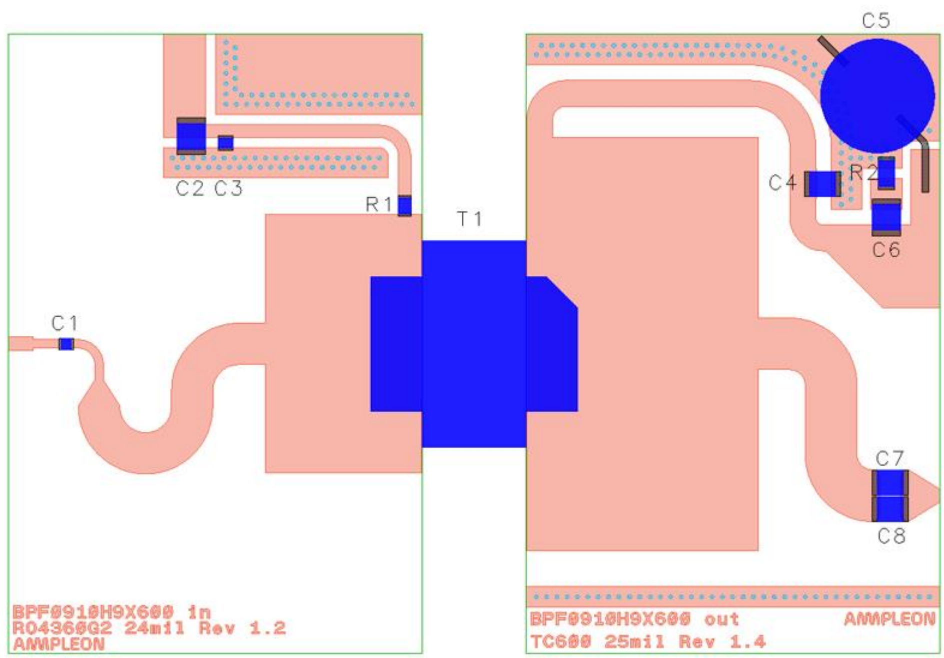

Figure 2. BLF0910H9LS600 reference layout

To provide the DC bias to the transistor, one quarter wavelength line is being used. Since this bias line acts as an open in the 902-928 MHz band, the matching circuitry remains symmetric. Besides this, it also reduces the demo board physical dimensions. However, if there is space available it is recommended to put bias lines at both sides of the matching structures as well at the gate side as the drain side for optimal symmetry.
To reduce the demo board dimensions even further a TC600 substrate with a thickness of 25 mil is used. This substrate is Teflon based and has a high relative permittivity.
The in- and output matching networks consist each of two transmission line elements.
The second matching step at the drain side is matching to 50 Ohm at exactly the edge of the PCB. On this PCB material it is not possible to extend this line with a 50 Ohm one because such a line would be too narrow to carry the power. It is recommended to round the corners of the pads below the DC blocking capacitors. This will lower the electric field there to avoid dielectric breakdown of the material below the capacitors. For these blocking capacitors, it is recommended to use capacitors with appropriate voltage level to avoid the capacitors to breakdown at possible mismatch conditions.

4. Transistor mounting guidelines

For the BLF0910H9LS600 it is important to correctly mount this transistor to the baseplate. The load impedance of this transistor is approximately 0.5 Ohm which means that every change in load impedance has quite some impact on the performance of this transistor. The transistor should be carefully mounted and the PCBs with matching networks should be soldered to the baseplate. The transistor should be soldered in the cavity without or minimizing the number of voids between transistor flange and baseplate. Another important aspect is the alignment of the transistor w.r.t. the cavity and matching structure on the PCB. Due to the mentioned low impedances, one can imagine that any misalignment of the transistor leads on the matching network will influence the internal transistor loading and reduces the transistor stability. This is an inherent (unwanted) side-effect of high power transistors.

Another important effect on transistor stability is the soldering of the transistor flange to the baseplate. In the electrical domain, this solder layer is represented as a source inductance. It's generally known that any increase of this inductance, in case of improper soldering, will decrease the transistor stability. Besides this, in proper soldering will lead to asymmetric thermal and electrical behavior inside the transistor.

The following guidelines should be followed for optimum performance:

1. Minimize the gap between transistor and PCB at the drain side. Figure 3 shows a picture of a wrong and a correct positioning. The left picture shows a gap between transistor and output matching PCB which is not desired. The right picture shows the desired situation where there is no gap between transistor and output matching PCB.

Figure 3. The gap between drain and PCB should be minimized

2. Center the transistor leads exactly in the middle of the matching networks for optimum performance and transistor stability. Figure 4 shows that both red arrows should have the same length.

Figure 4. The transistor should be centered inside the matching networks. Both arrows indicate the same distance from lead to edge matching network

The effect of the gap between drain and the output matching PCB is that the load impedance will be different due to the introduction of extra length in the matching network. This will result in loss of performance. Simulations are done to study the effect of the gap between drain and PCB. Simulations are done with a gap size of 0.4 mm. in figure 5 the results are shown. Output power can decrease by 40 W and efficiency can decrease by 7 %.

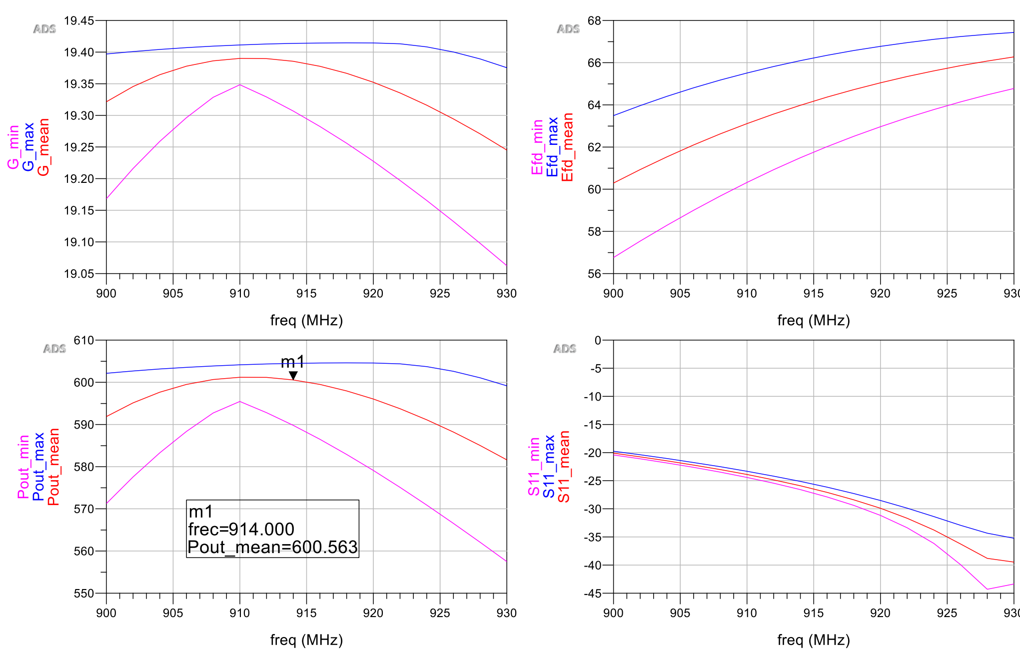

Figure 5. Simulations of 0.4mm gap at drain side

5. Summary

In this application note, the importance has been shown of proper design of the transistor matching networks and mounting. This can be summarized as follows:

- Design symmetric matching networks with preferable 2 bias lines or 1 bias line implemented as a quarter wavelength line.
- Center the drain lead symmetric on the output matching track.
- Align the drain lead as close as possible to the output matching track.
- Ensure proper soldering of the transistor flange to the baseplate.

6. Bill of Materials

Table 2. Bill of Materials

Part	Description	Part number	Value
C1, C3	Chip capacitor	ATC100A101JT150XT	100 pF
C2, C6	Chip capacitor	C3225X7S2A475K200AE	4.7 uF / 100 V
C4, C7, C8	Chip capacitor	ATC100B510FT500XT	51 pF
C5	Electrolytic capacitor	ECA1JHG471	470 uF/ 63 V
R1	Chip resistor	ERJT06J100V	10 Ohm
R2	Chip resistor	ERJP08J3R0V	3 Ohm
T1	LDMOS transistor	BLF0910H9LS600	
Input board	RO4360G2		24 mil thickness
Output board	TC600		25 mil thickness

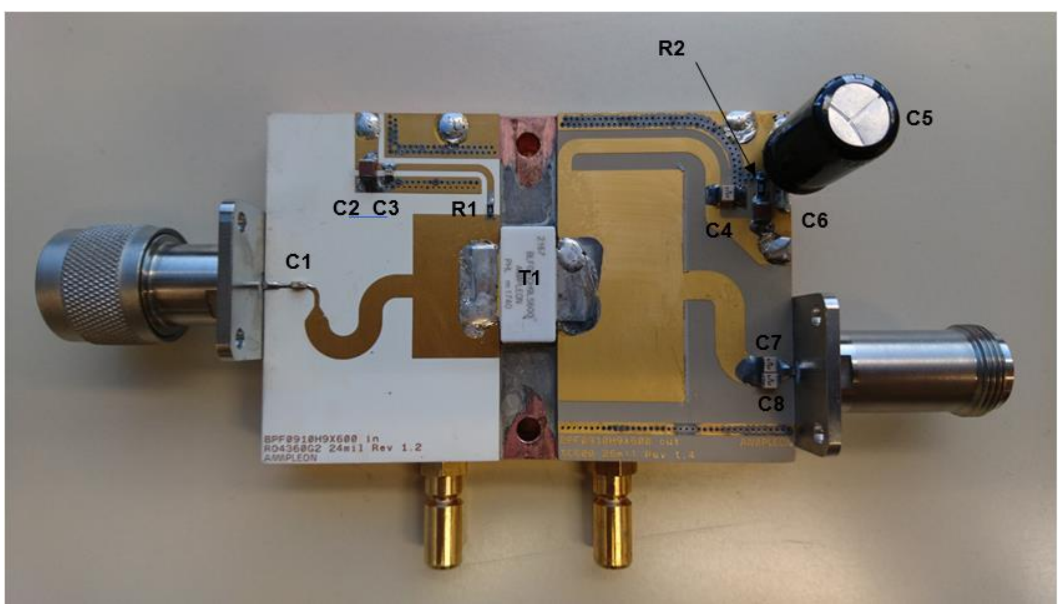

Figure 6. BLF0910H9LS600 demo board component description

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