AN1503

Application Note OM3999

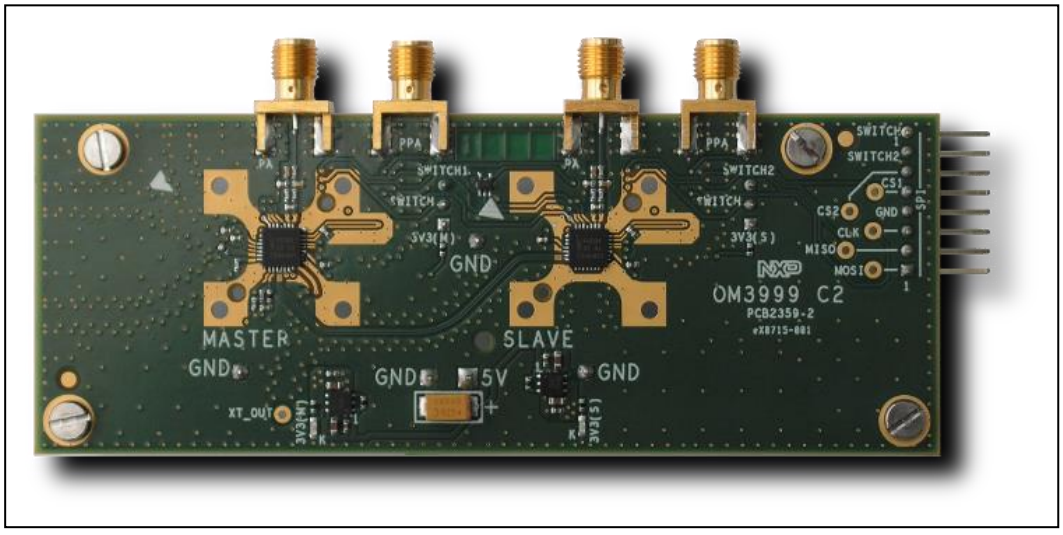
Rev. 1.4 — 22 March 2018

AMPLEON

Application note

Document information

Info	Content
Keywords	RF energy, OM3999, BLP25RFE001
Abstract	This document helps the user to build up his/her own application based on the schematic and layout of the OM3999 reference design.



Revision history

Rev	Date	Description
1.0	2015 01 14	Creation
1.1	2015 02 03	Layout recommendation for LO daisy chain
1.2	2015 02 17	Recommendations for unused LO pins or RF outputs
1.3	2015 03 31	Update with the latest demoboard OM3999-C2
1.4	2018 03 22	Update with the latest formatting

Contact information

For more information, please visit: http://www.ampleon.com

For sales office addresses, please visit: http://www.ampleon.com/sales

1. Introduction

The OM3999-C2 reference board is described here to explain how to best use the BLP25RFE001 integrated circuit in a customer application. It is useful for all targeted applications like RF cooking or RF lighting.

The purpose of this application note is to provide a reference to keep the best tradeoff between best performances and BOM optimization.

This application note includes:

- A short description of each part, schematics and layout of the reference design.
- Layout recommendations to implement properly the Ampleon components in a dedicated customer application.

2. Related materials

Besides this application note, several documents and materials are available:

- Datasheet:
  - BLP25RFE001 datasheet
- Ampleon hardware:
  - OM3999-C2 evaluation board embedding 2 ICs BLP25RFE001, available for customer evaluation.
- Other hardware:
  - FTDI USB 2.0 cable used to connect the SPI interface. Reference: *C232HM-DDHSL-0*. It can be found here: http://www.ftdichip.com/Products/Cables/USBMPSSE.htm
- Application note:
  - AN1502 QuickStart OM3999 (how to setup Ampleon reference board and evaluation software)
- Software:
  - OM3999 evaluation software
  - Driver source code for BLP25RFE001
- Reference design:
  - OM3999-C2 Orcad CAD project (schematic: file .DSN; layout: file .BRD)
- Package:
  - AN10365: Surface mount reflow soldering description
  - AN10366: HVQFN mounting guideline (this is the reference document for soldering BLP25RFE001)

3. Typical applications

Different applications can be addressed with the BLP25RFE001 ICs, described below. They usually rely on an embedded platform with a microcontroller. This microcontroller must have an SPI interface to control one or more BLP25RFE001 circuits.

3.1 Application: RF cooking

For RF cooking application, several ICs BLP25RFE001 are used as signal generators and power amplifier drivers.

A single device BLP25RFE001 is used to generate the signal frequency, the local oscillator being propagated in a daisy chain through LOout and LOin pins as shown on the next figure.

The phase shift between all paths is fixed at initialization, allowing afterwards to minutely control the phase shift applied selectively on all paths.

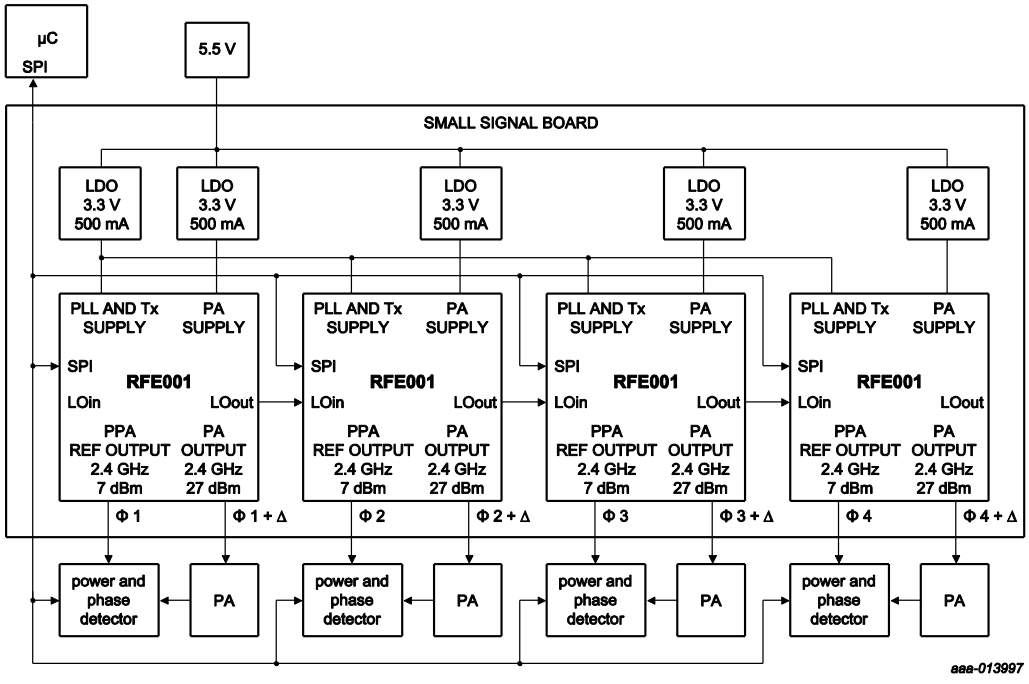


Fig 1. Application diagram for cooking application

3.2 Application: RF lighting

For RF lighting, the BLP25RFE001 serves as a power amplifier driver for a single plasma lamp.

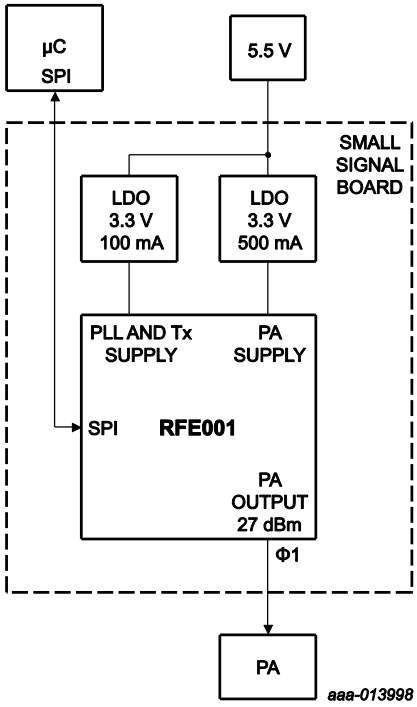


Fig 2. Application diagram for lighting application

4. BLP25RFE001

4.1 General description

The product provides an all-in-one solution for the small signal generation in the RF energy solutions such as cooking and lighting markets.

The product facilitates RF energy design by:

- Allowing on-board integration
- Providing flexibility in system solution development

The function description can be found in the product datasheet.

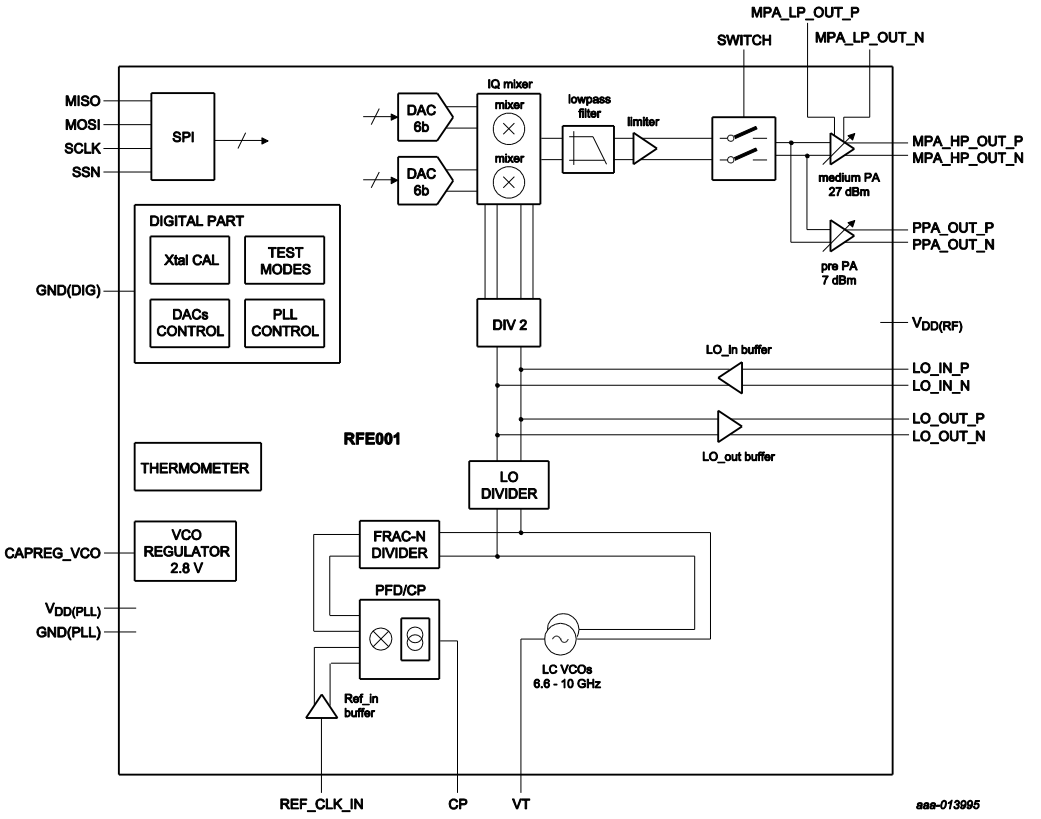


Fig 3. BLP25RFE001 block diagram

4.2 Pinning

The BLP25RFE001 chip is mounted in a HVQFN28 package.

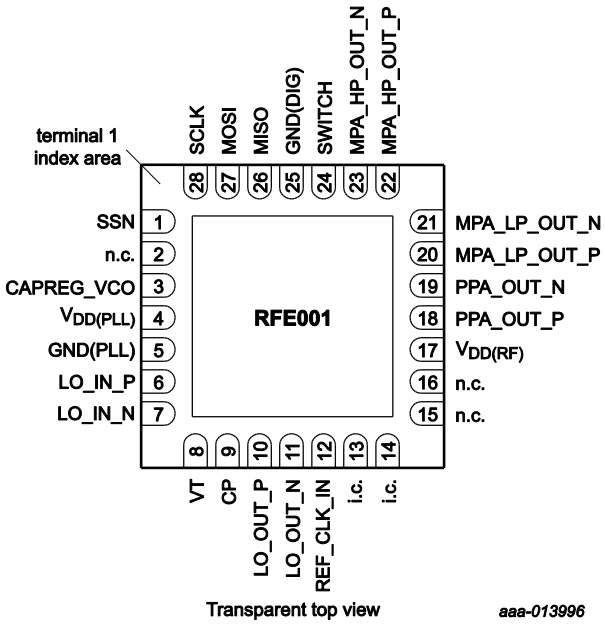


Fig 4. BLP25RFE001 pinning

4.3 Features

The BLP25RFE001 features are listed hereafter:

- Support from 2400 MHz to 2483.5 MHz, from 902 MHz to 928 MHz and from 433 MHz to 434.8 MHz ISM bands
- Single 3.3 V supply voltage
- SPI-bus interface up to 20 MHz
- Fully integrated LC-VCO operating in the range from 6.6 GHz to 10 GHz and used with a ΣΔ PLL to generate the frequency
- Very fast tuning and hopping time PLL
- High frequency daisy chaining allowing coherent excitation of multiple RF amplifier chains
- 360° phase shifter with 1.4° steps
- Medium Power Amplifier (MPA) delivering an output up to +27 dBm
- Integrated 20 dB gain control
- Integrated RF switch allowing PWM control
- Temperature sensor indicates the junction temperature of the die
- RoHS compliant

4.4 BLP25RFE001 key inputs/outputs

4.4.1 Power supplies

- The BLP25RFE001 needs a 3.3V power supply
- The consumption can be up to 500mA (at 27dBm output power)

4.4.2 SPI

The SPI requires 4 logical signals, so 4 pins for each BLP25RFE001:

- SCLK — Serial Clock (from the master/µC)
- MOSI — Master Output (from the master/µC)
- MISO — Master Input, Slave Output (from the slave/BLP25RFE001)
- SSN — Slave Select (active low, from the master/µC)

In an application with more than one BLP25RFE001, each IC requires a dedicated SSN pin from the micro-controller.

Note that the MISO output pin of the BLP25RFE001 does not switch to tri-state when the device is not selected (SSN high). Then it is not possible to use the independent slave configuration sharing the same SPI bus with dedicated SSN chip select pins.

To handle an application with multiple BLP25RFE001 devices, there are two approaches:

- Using a dedicated SPI bus for each BLP25RFE001 device. Hence, a 2-chip application would require 2 dedicated SPI buses.

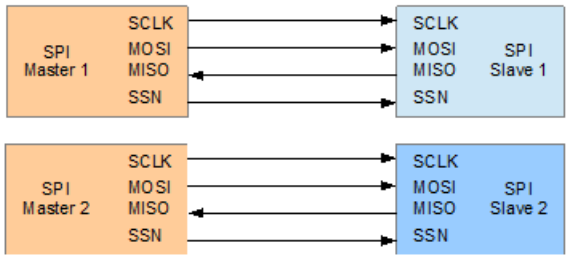


Fig 5. SPI configuration with 2 SPI masters

- Adding some logic to retrieve an acceptable common MISO output like in combining MISO and SSN signals. Possible options detailed below in a dual device configuration.

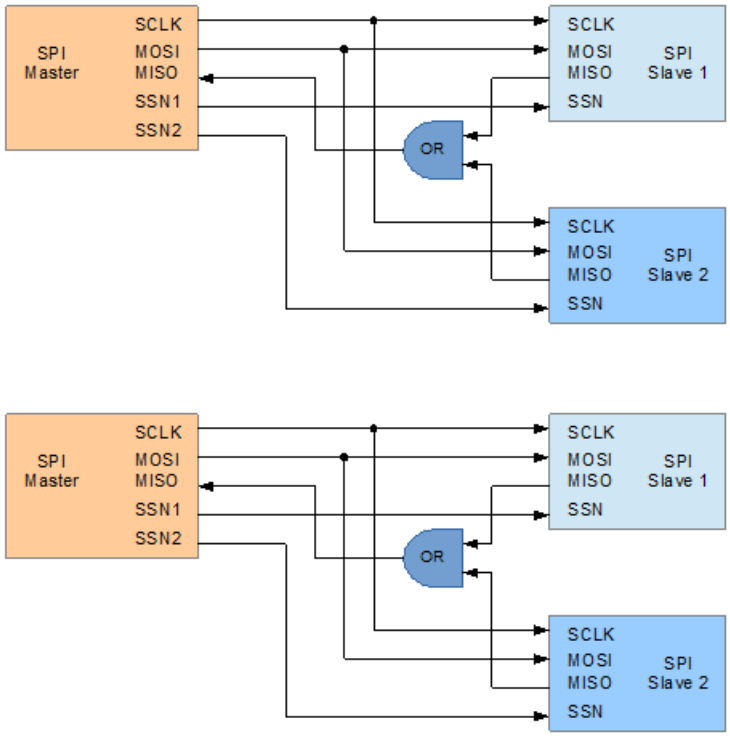


Fig 6. SPI configurations with one SPI master and additional logic

It is also advised to insert a Schottky diode between SSN pin and VCC, when the voltage on SSN pin might exceed the supply voltage on BLP25RFE001 (VCC). Refer to the application picture in the datasheet.

4.4.3 Reference clock

The reference clock must be a 16 MHz frequency signal.

4.4.3.1 Buffer mode

The oscillator only supports the buffer mode. This mode requires an external signal.

- The 16 MHz clock reference must be delivered to the pin REF_CLK_IN.
- AC coupling is required (using a 100pF capacitor).

The Ampleon reference design uses the following crystal clock oscillator to keep a stable reference frequency over the temperature range:

- Manufacturer: NDK
- Reference:
  - NZ2520SB 16MHz END4688A (used on the reference schematics)
  - NZ2016SA 16MHz END4690A (smaller size, lower cost)

4.4.3.2 Oscillator mode

Currently, the external crystal configuration is not supported due to a high sensitivity to the output power.

4.4.4 Loop filter

The loop filter is located between CP and VT pins. It is designed for a particular signal bandwidth.

4.4.5 Local oscillator input/output

With multiple BLP25RFE001 ICs, some applications might require to use the same output signal frequency with an accurate phase control. In this situation, the reference frequency might be shared among several ICs. A single BLP25RFE001 selects the frequency through its own VCO, then it generates a reference LO signal at twice the frequency of the RF output signal. This reference LO can be cascaded from the outputs LO_OUT_P/ LO_OUT_N to the inputs LO_IN_P/ LO_IN_N.

This use case is depicted in the RF cooking application (refer to Fig 1).

For the master device, considered as the generator, the LO input is not used. For the master device only, the pins LO_IN_P/LO_IN_N must be carefully connected to a 50Ω resistor and a 6.8pF capacitor, as shown in Fig 7.

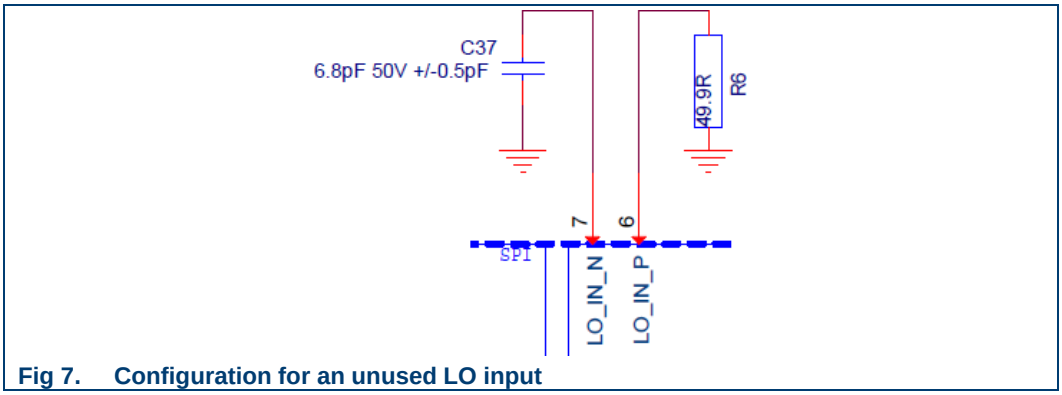


Fig 7. Configuration for an unused LO input

For a device not connected to a slave, the LO output signal is not cascaded. In such a case, the pins LO_OUT_P/LO_OUT_N can remain unconnected.

4.4.6 Switch

The input pin SWITCH allows to switch on/off the RF output signals, both the MPA and PPA outputs. The pin is active high.

4.4.7 PPA output (low power)

A low power level can be obtained from the differential output PPA_OUT on the pins PPA_OUT_P and PPA_OUT_N. This output can deliver a power level up to 7 dBm. The differential outputs require a balun and a proper impedance matching to deliver the maximum expected power level. For this matter, the external components depend on the selected frequency band.

When not used, the pins PPA_OUT_P and PPA_OUT_N can be connected directly to the 3.3V power supply.

4.4.8 MPA output (medium power)

A medium power level can be obtained from the differential output MPA_HP_OUT on the pins MPA_HP_OUT _P and MPA_HP_OUT _N. This output can deliver a power level up to 27 dBm. The differential outputs require a balun and a proper impedance matching to deliver the maximum expected power level. For this matter, the external components depend on the selected frequency band.

When not used, the pins MPA_HP_OUT_P and MPA_HP_OUT_N can be connected directly to the 3.3V power supply.

4.5 Layout recommendations

4.5.1 Reference clock

In buffer mode, the reference clock input must be carefully filtered to reject the RF output signal, especially at highest output power (27 dBm). See the reference schematic and layout on the reference clock pin.

4.5.2 Grounding

Due to the high temperature dissipation, the exposed die pad must be carefully grounded with a high number of via holes. On the OM3999 reference board, a matrix of 25 via holes is used.

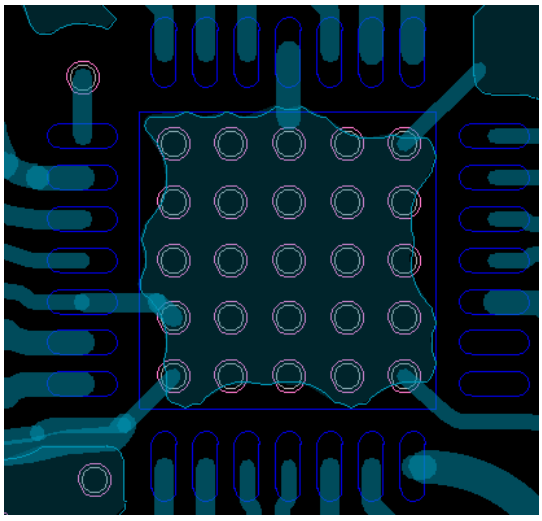


Fig 8. Ground of the die ground

4.5.3 RF output

The two differential RF outputs for medium and low power level are expected to be loaded with a 50Ω impedance. Hence, the micro strip line must have a 50Ω characteristic impedance.

The layout of the line depends on the board characteristics. Basically, the conductor thickness, dielectric type of insulator, depth between conductive top layer and ground layer, etc… Some tools can help to design such RF lines, like:

- *AppCAD* from *Agilent/Avago Technologies*
- *PCB Toolkit* from *Saturn PCB Design*

The recommended microwave line is a coplanar strip line with a ground plane underneath (see Fig 9).

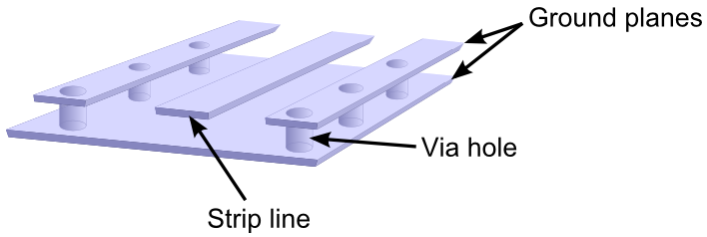


Fig 9. Coplanar strip line with ground plane

5. Schematic

The most relevant page of the reference schematic is shown hereafter. For the complete schematics, refer to the reference hardware package of the OM3999 board.

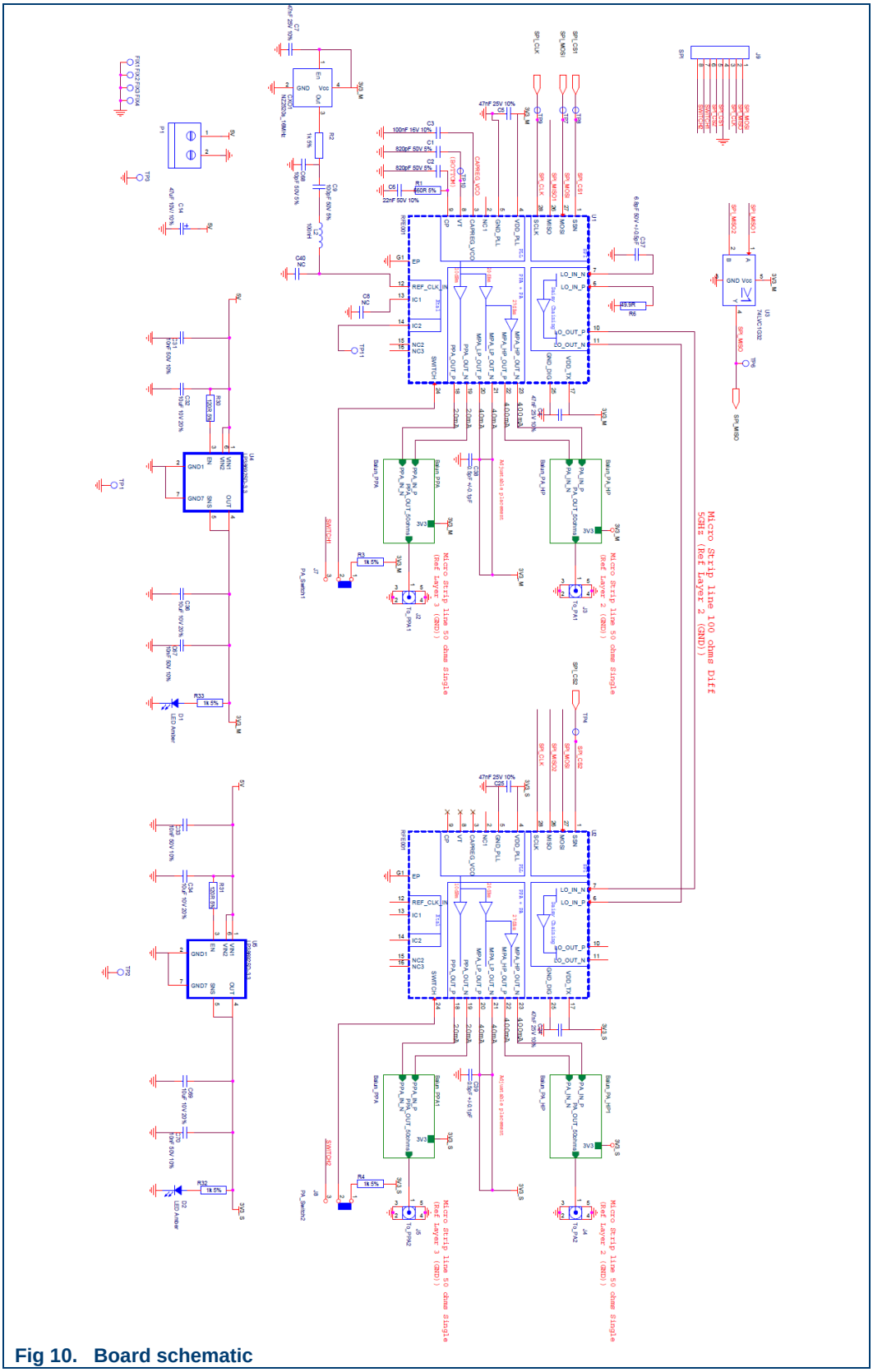


Fig 10. Board schematic

5.1 Low power level

5.1.1 Impedance matching at 2.4GHz

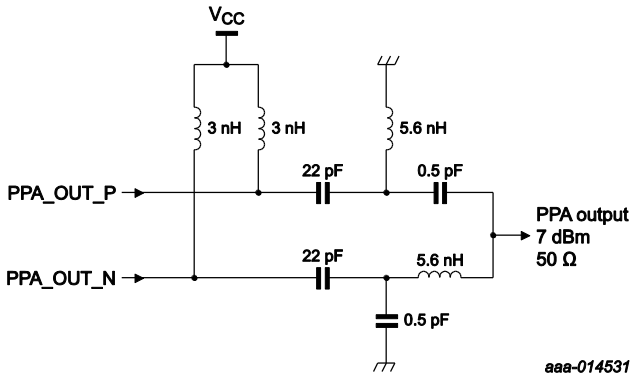


Fig 11. Matching network of low power output at 2.4GHz

5.1.2 Impedance matching at 915MHz

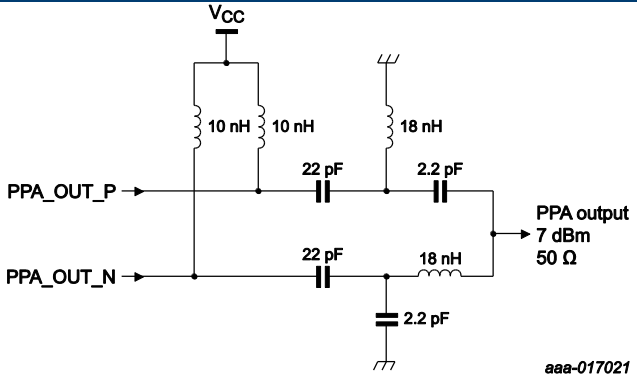


Fig 12. Matching network of low power output at 915MHz

5.2 Medium power level

5.2.1 Impedance matching at 2.4GHz

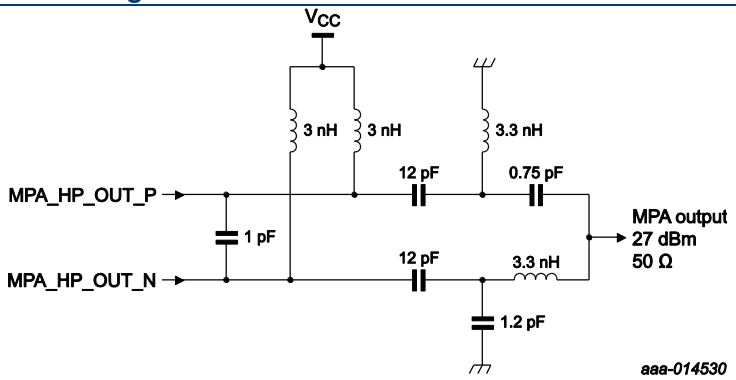


Fig 13. Matching network of medium power output at 2.4GHz

5.2.2 Impedance matching at 915MHz

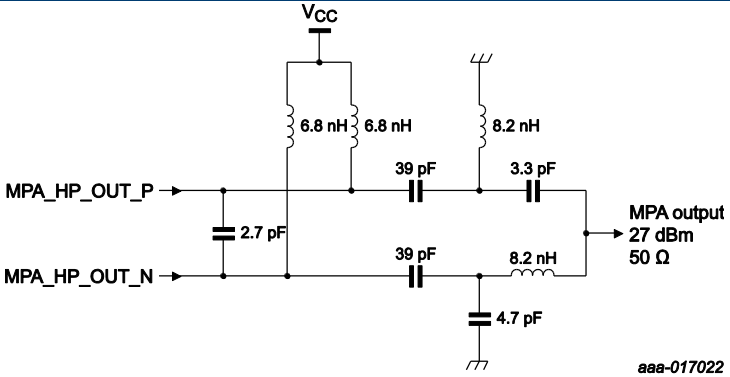


Fig 14. Matching network of medium power output at 915MHz

6. Layout

These layout recommendations concerns the OM3999 application, which combines two devices BLP25RFE001.

6.1 LO daisy chain

For an application with two devices BLP25RFE001, there is usually one master and one slave. In such configuration, the master controls the signal frequency through its local oscillator, whose LO signal is transmitted to the slave.

With more than two devices, there is usually one master for all slaves. Each slave transmits its LO signal to the next slave.

This is clearly depicted in the typical cooking application diagram (refer to Fig 1).

The daisy chaining must take great care of the LO transmit line from master to slave or from slave to slave. This is achieved with a differential micro strip line with a 100 Ω characteristic impedance. The OM3999 layout can be used as a reference, knowing that the line impedance depends on the PCB characteristics.

7. Legal information

7.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Ampleon does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Ampleon does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Ampleon takes no responsibility for the content in this document if provided by an information source outside of Ampleon.

In no event shall Ampleon be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Ampleon' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of Ampleon.

Right to make changes — Ampleon reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Ampleon products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Ampleon product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Ampleon and its suppliers accept no liability for inclusion and/or use of Ampleon products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Ampleon makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Ampleon products, and Ampleon accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Ampleon product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s).

Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Ampleon does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Ampleon products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Ampleon does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Terms and conditions of commercial sale — Ampleon products are sold subject to the general terms and conditions of commercial sale, as published at http://www.ampleon.com/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Ampleon hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Ampleon products by customer.

7.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

Any reference or use of any 'NXP' trademark in this document or in or on the surface of Ampleon products does not result in any claim, liability or entitlement vis-à-vis the owner of this trademark. Ampleon is no longer part of the NXP group of companies and any reference to or use of the 'NXP' trademarks will be replaced by reference to or use of Ampleon's own trademarks.

8. List of figures

9. Contents

For more information, visit: http://www.ampleon.com
For sales office addresses, please visit: http://www.ampleon.com/sales

Date of release: 22 March 2018
Document identifier: BLP25RFE001-0