AN11766

Uppsala University's BLF188XR single ended amplifier at 352 MHz

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Application note

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1. Introduction

1.1 General description

At FREIA, Facility for Research Instrumentation and Accelerator Development at Uppsala University, Sweden we develop and test particles accelerator components. Initially, FREIA develops the RF system for the spoke cavities of the European Spallation Source (ESS) linear accelerator (LINAC) and tests prototype spoke cavities at 352 MHz and nominal RF power of 400 kW. For this purpose, a helium liquefaction plant is installed with a versatile horizontal test cryostat accommodating two spoke cavities, fed by two RF power stations, each based on two tetrodes [1]. Solid-state based RF power stations are generating an increasingly higher interest, considering the higher efficiency, reduced maintenance, higher operability and life expectancy of the technology. In this context, we develop high power amplifiers build around commercially available LDMOS transistors.

At FREIA laboratory we develop also compact power combination, up to the MW level [2]. For the power generation, we consider that each amplifier module, using for example the BLF188XR LDMOS transistor from Ampleon, would provide a nominal output power of about 1 kW.

At Ampleon high performance, high power LDMOS transistors are developed, which are excellently suited for applications like an amplifier to drive a particle accelerator installation. In this amplifier the BLF188XR was used because of its high power, high efficiency and excellent ruggedness capabilities. The Ampleon application support department assisted in the design and evaluation needed for this work.

This document shows the measurement results of the 352 MHz single ended demonstrator amplifier designed by the University of Uppsala, FREIA laboratory, using one BLF188XR. The amplifier is primarily meant for application in power generators for particle accelerators under pulsed operation. Preliminary measurements show that the amplifier is capable of producing over 1 kW output power at efficiencies of 67-68 % in pulsed conditions with high duty cycle 10% and about 61 % under full CW conditions, with a gain about 20 dB [3]. In ESS mode, i.e. Duty Cycle=5%, pulse duration of 3.5 ms and 14 Hz repetition, thermal effects are attenuated due to the larger time between pulses, allowing the amplifier to cool down in between pulses, efficiency reaches 71% at an output power of 1250 W.

1.2 Test object details

Transistor type:	BLF188XR Bolted down, using WPS2 compound	
Package:	SOT539A	
Board:	output:	University of Uppsala board design
	Input:	University of Uppsala board design
	Circuit on aluminum base plate, cooling water channel in base plate.	

The demo circuit has been designed on Rogers RO3003, Er = 3, h = 0.76 mm.

[1] R. Ruber et al., "The New FREIA Laboratory for Accelerator Development", IPAC 2014, THPRO077.

[2] V. Goryashko, D. Dancila, A. Rydberg and R. Ruber, A Mega Watt class compact power combiner for solid state amplifiers, Journal of Electromagnetic Waves and Applications, Sept. 2014, 1-14. DOI: 10.1080/09205071.2014.962187

[3] D. Dancila et al., "Solid-state amplifier development at FREIA", IPAC 2014, WEPME012

1.3 Design considerations

Characteristic parameters for ESS are as follows: long CW pulses of 3.5 ms length, 14 Hz repetition rate (5% duty cycle) at 352 and 704 MHz. The goal of the amplifier design demonstrator is to use the BLF188XR transistor producing about 1 kW output power (pulsed and full CW) with a sufficient efficiency for green particles accelerators, i.e. efficiency higher than 60% at 1 kW power level, while maintaining harmonics at very low level, i.e. below 20 dBc. In addition, all components should be machine surface mounted in prevision for mass fabrication. The matching network (one wide, stepped stripline) between the drains of the MOSFET and the output is fine-tuned using SMD capacitors during hot-S parameters measurements. Drain feed is done by connecting the supply voltage via a thick wire air coil. The input circuit uses a similar design to transform the 50 Ohms input impedance to match the transistor input impedance. Such a way, the amplifier design avoids using input and output baluns in a push pull configuration that would implement coaxial or PCB integrated striplines.

1.4 Circuit design

The source and load impedances to the transistor for optimal working conditions were obtained using load-pull and source-pull simulations with ADS software [4] and LDMOS model from Ampleon. The optimal load and source impedances for an optimal PAE at are 0.341 + j0.464 and 0.363 + j0.716, respectively [5].The amplifier is not matched for maximum gain, as this would result in a lower efficiency, but in between maximum gain and maximum drain efficiency impedance points. Note that impedances are roughly four times smaller than for the push-pull, differential case.

1.5 Layouts and components

The circuit has been designed on Rogers RO3003, ε_r=3, tanδ=0.001, Cu=35µm and h=0.76mm. Cooling is provided by connecting a water supply to the aluminium baseplate with cooling tubes. All RF capacitors are from American Technical Ceramics type 800B, suited for high power use. Following Fig 1, capacitors C1, C2, C3 and C13, C14, C15 (560 pF) are decoupling capacitors, similar to C7 and C8, used as DC blocks. The input circuit uses a two steps micro stripline transformer. The output circuit uses a 2 step micro stripline transformer. Drain bias is supplied via a heavy wire (1 mm diameter, 10 mm external diameter and 10 mm long) enamel copper choke inductor, connected close to the drain lead. The matching capacitor close to the drain of optimal value 15 pF was split in three capacitors C10, C11 and C12 to lower the heat dissipation per capacitor. The circuit can be slightly tuned for different combinations of power and efficiency by varying the value and position of those capacitors in the output circuit. Decreasing the value will result in a higher power and a lower efficiency. Likewise, slightly increasing C10, C11 and C12 will decrease the power and slightly increase the efficiency. A detailed overview of the components used is presented in Table 1.

[4] http://www.keysight.com/en/pc-1297113/advanced-design-system-ads?cc=US&lc=eng

[5] http://www.ampleon.com/products/broadcast/0-500-mhz-rf-power-transistors/BLF188XR.html

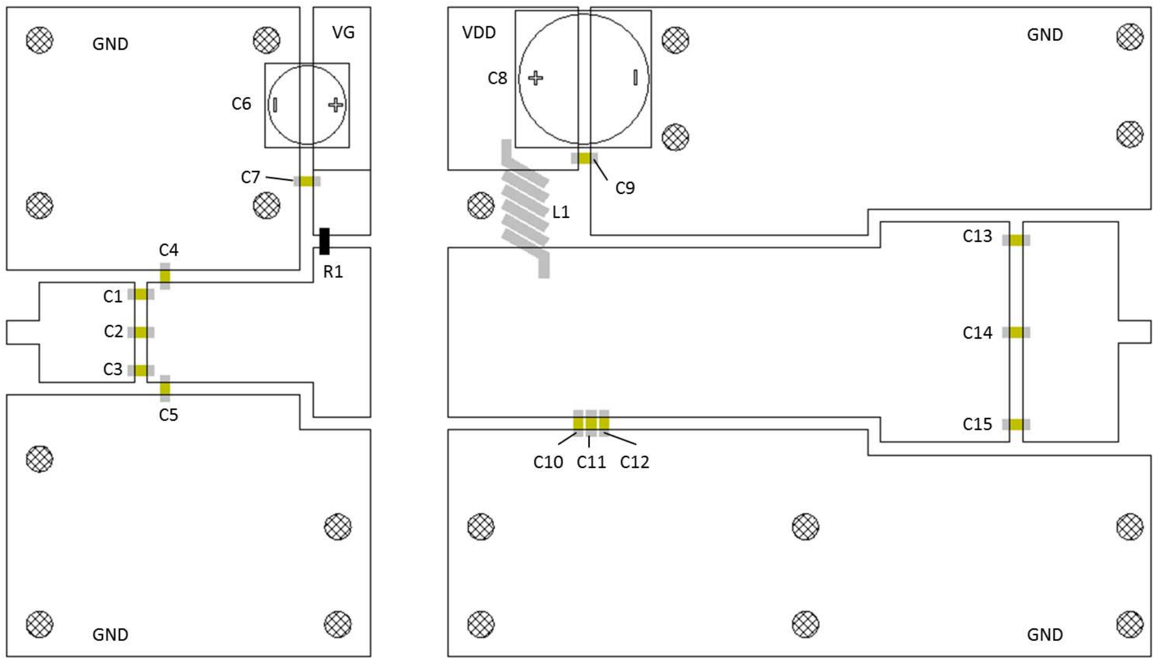


Fig 1. Circuit layout

Table 1. Circuit components

Component	Description	Value	Remark
PCB	Rogers 3003, Er=3, h=0.76 mm, Cu 1 oz		
C1, C2, C3, C7, C9, C13, C14, C15	multilayer ceramic chip capacitor	560 pF	[1]
C4, C5	multilayer ceramic chip capacitor	47 pF	[1]
C6	electrolytic capacitor	47 μF, 63 V	
C8	electrolytic capacitor	470 μF, 63 V	
R1	resistor SMD1206	47 Ω	3W
L1	6 turns, 1 mm wire enamel copper	D = 10 mm, length = 10 mm	
C10, C11, C12	multilayer ceramic chip capacitor	15 pF	[1]

[1] American Technical Ceramics type 800B or capacitor of same quality.

1.6 Harmonic balance simulations

The validation of the designed matching networks and dimensions optimization is realized using ADS. The layout, comprising both input and output matching networks is used for Momentum simulations, see, Fig 2. The mesh, also visible in this Figure, is used for the method of moments (MoM) simulation; connecting ports are also indicated. In addition of the input and output ports, a number of additional ports is implemented that will later be used to connect matching and decoupling capacitors, the BLF188XR transistor, DC biasing networks and output and input coaxial connectors.

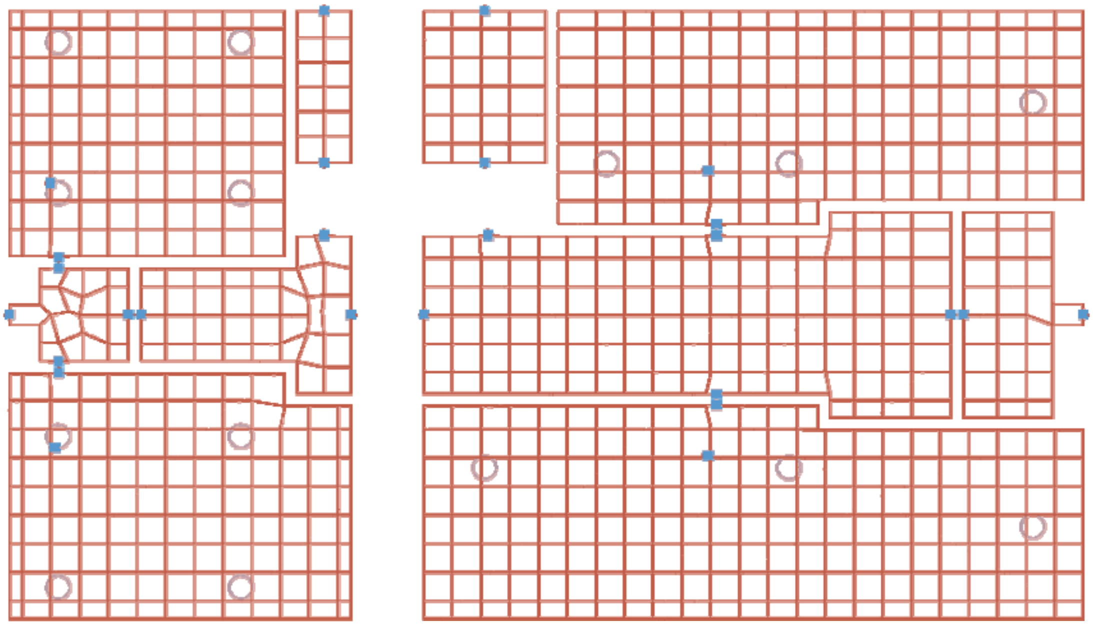
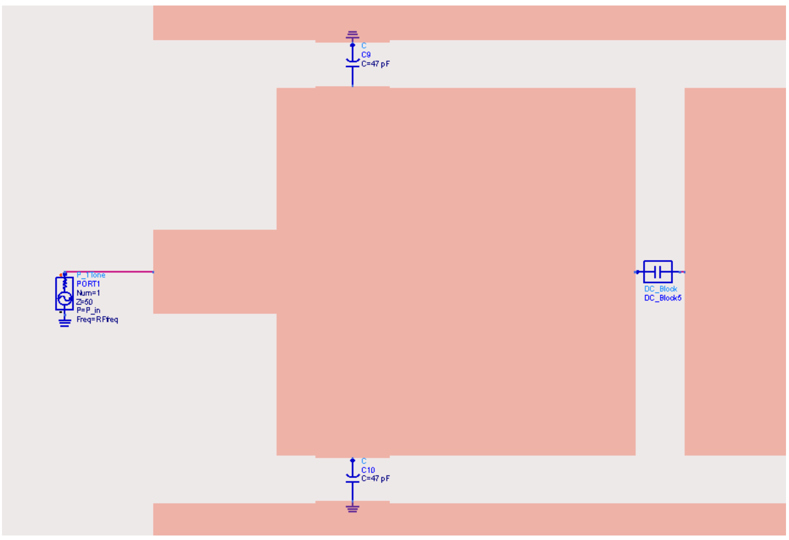
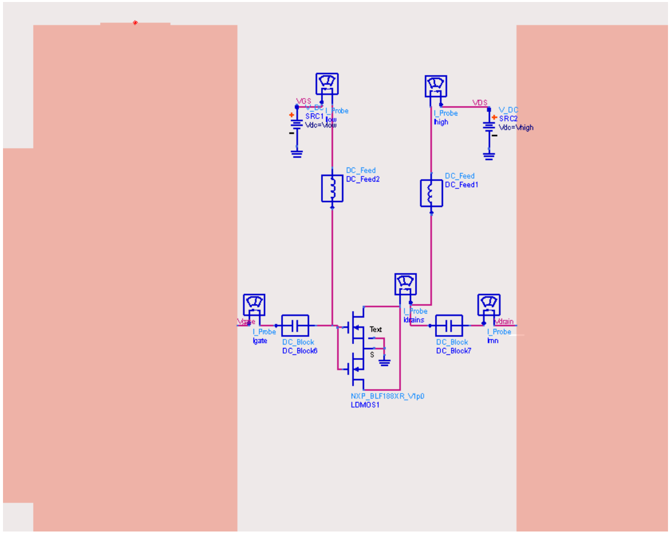


Fig 2. Momentum simulation set-up in ADS with the MoM mesh

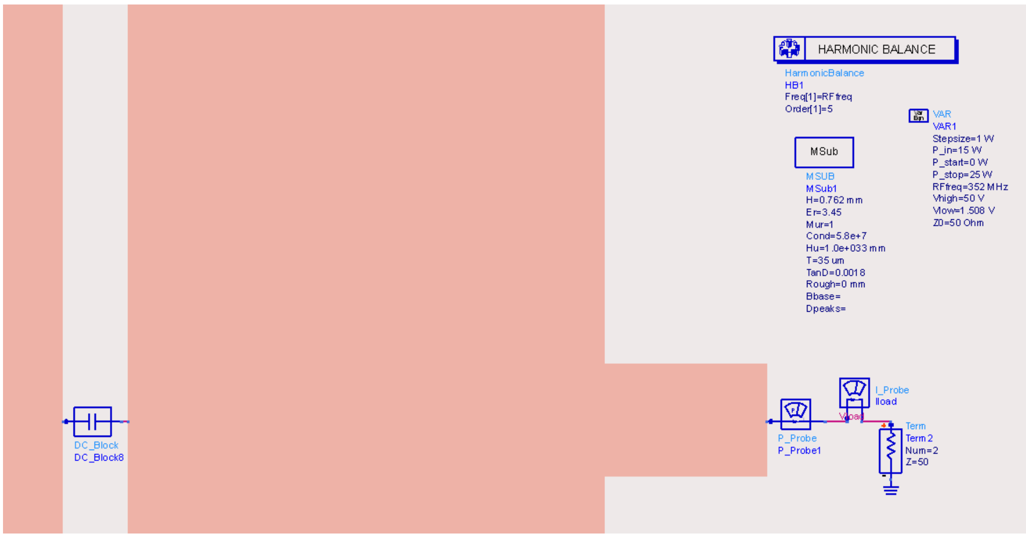
The matching networks are used in combination with Ampleon's transistor model for Harmonic Balance (HB) simulations with essential details, such as: input, transistor connection and output, see Fig 3.



a) input



b) transistor connection



c) output

Fig 3. Momentum simulation set-up in ADS

The output power obtained around 1 dB compression from the maximum gain 18.35 dB is about 1466 W and the efficiency about 69.6%, see Fig 4.

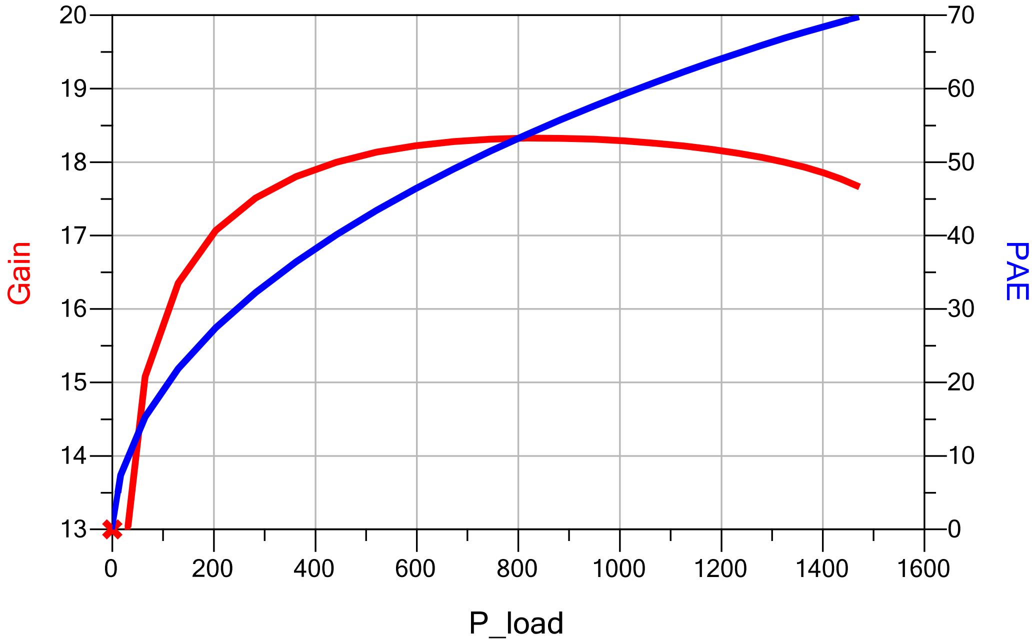


Fig 4. Typical results obtained for the HB simulations with ADS.

1.7 Mechanical drawings

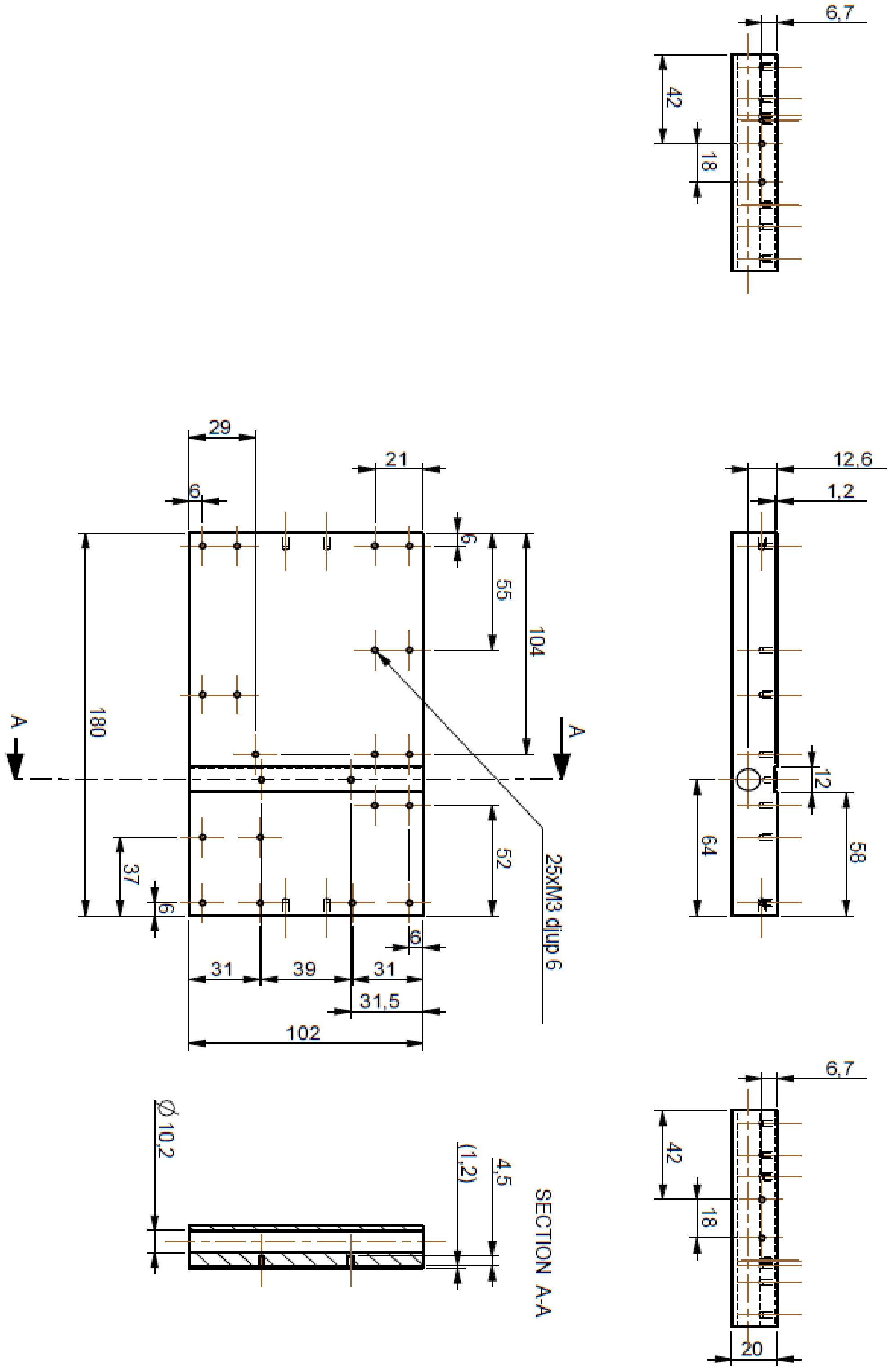


Fig 5. Mechanical drawing

1.8 Test setup

In addition of the standard Power/Gain/Efficiency measurements in CW and Pulsed Peak Power operation we perform Hot S-parameters measurements to fine tune the matching networks at high power, i.e. above 1 kW level. In this particular measurement, the amplifier is excited at some given power level in the normal way. In addition, a small pilot tone is used to directly measure the reflection coefficient of the output port of the DUT. The analysis here will assume that the main drive signal is sinusoidal and offset slightly in frequency from the probe tone to allow for receiver selectivity [6]. In order to measure hot S-parameters, a dedicated measurement set-up is implemented, see Fig 6. The set-up consists in externalising 2 ports of the PNA network analyser N5230A, using high power components such as bidirectional couplers and circulators. The PNA is provided with two signal generators which are used in this measurement, configured in frequency offset. Signal S3 runs in pulsed mode at the carrier frequency of 352 MHz and feeds a 100 W pre-amplifier of about 50 dB gain. The PNA's second source is used in addition to perform S-parameter measurements at ports 1 and 2 (S1 and S2), in a frequency sweep of 25 MHz around the carrier frequency. The reference ports (R1 and R2) measure the incident power to the DUT amplifier. In order to measure the return loss, ports (A and B) measure the reflection signal back from the amplifier at the input and output, respectively. The complex values return loss are obtained from the ratio S11 = R1 \ A and S22 = B \ R2, at port 1 and 2, respectively.

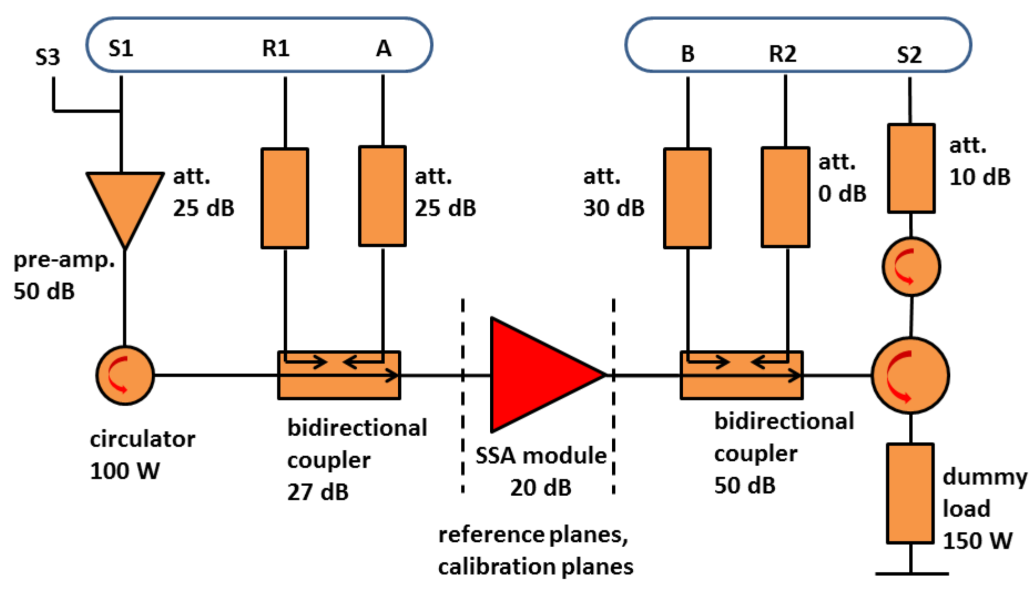


Fig 6. Test measurement setup for hot S-parameters measurements.

The test measurement setup for hot S-parameters measurements is essentially used in a preliminary stage where the prototype needs fine tuning, and the matching networks need some minor adaptation. In addition, the same set-up is essential in developing amplifiers with output impedance different from 50 Ohm. Typical output impedances such as 25 and 12.5 Ohm are very useful in a combination scheme for few kW larger amplifiers.

[6] Anritsu, “Hot S22 and Hot K-factor Measurements”, Application Note 11410-00295

Although not reported on in this report the hot S parameter setup can also be used to investigate stability of an amplifier under full load conditions. We may suggest to use this for follow up work.

2. Measurements results

2.1 Used test signals

The following tests have been performed:

- Power/Gain/Efficiency measurements.

- Pulsed Peak Power and CW sweeps

- Harmonic Level and Spectral Purity Tests

- Hot S-parameters measurements.

Pulsed, 100µS, Duty Cycle=10%, 3.5 mS (Fig 8 and Fig 9), Duty Cycle=5% (Fig 10) and full CW (Fig 7). Measurements have been performed at VDS =50 V (Fig 7 and Fig 8) and V_{DS} =55 V (Fig 9), IDQ = 40 to 200 mA, and T_h = 25C, unless otherwise specified.

2.2 CW/Pulsed – Gain and Efficiecy vs Power

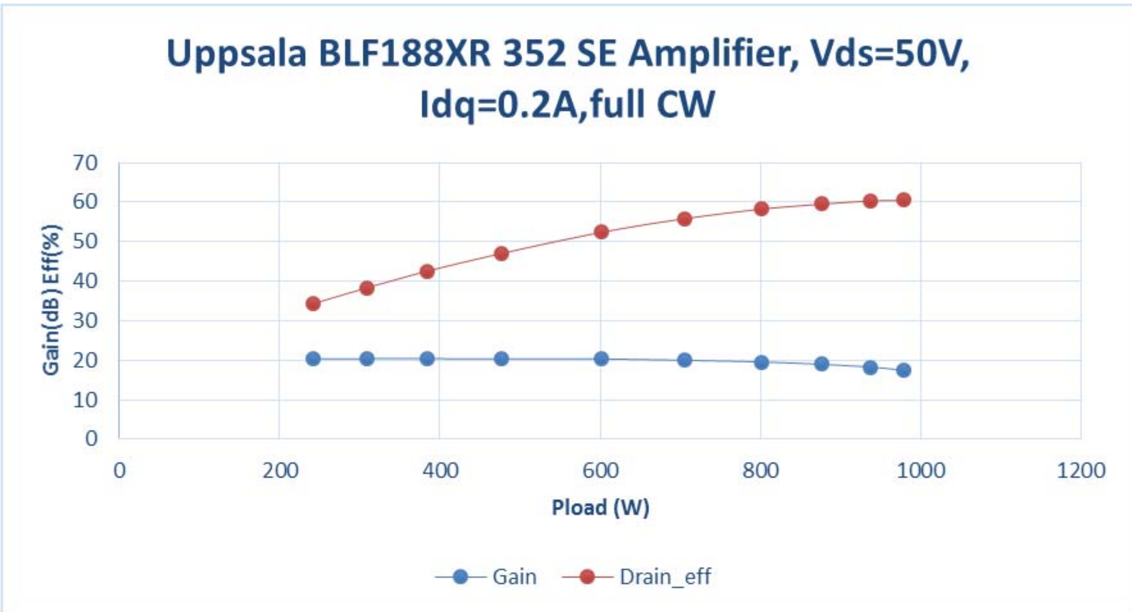


Fig 7. CW Power and efficiency (Vds=50 V)

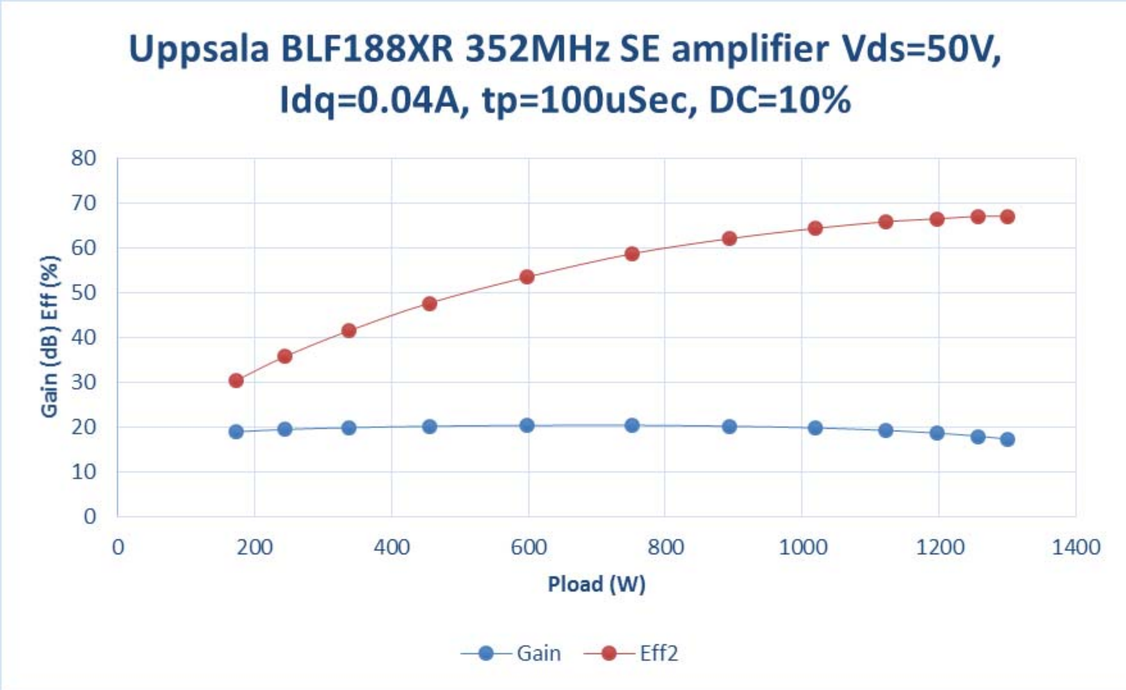


Fig 8. Pulsed power and efficiency (Vds=50 V)

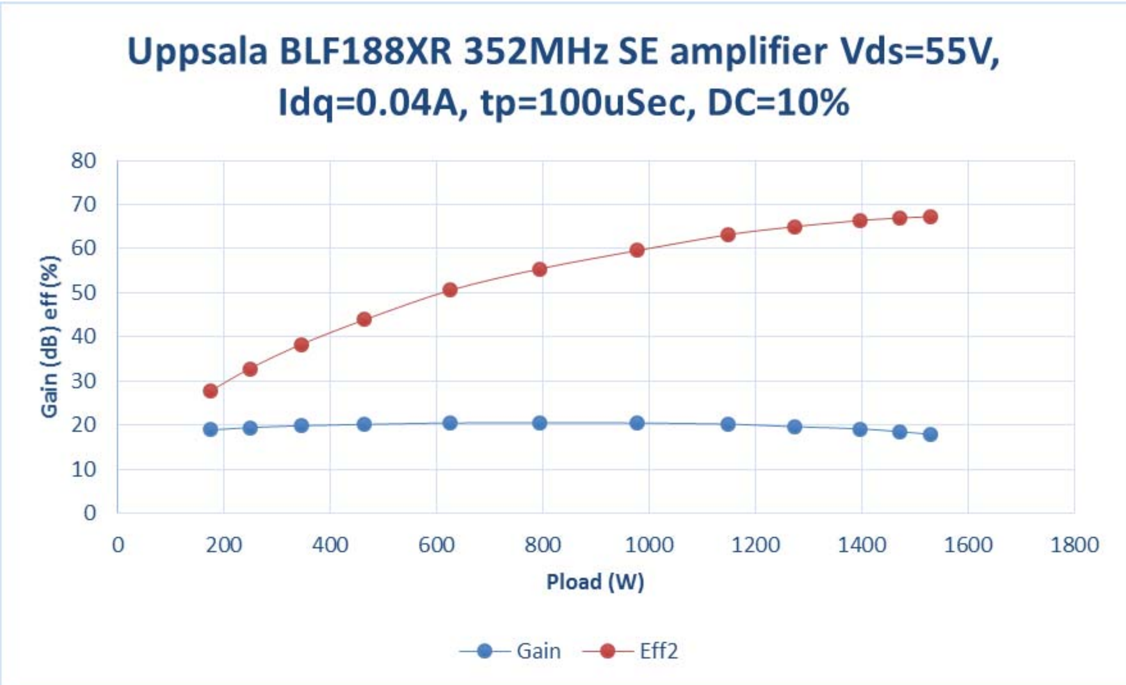


Fig 9. Pulsed power and Efficiency (Vds=55 V)

Input return loss was measured at 12dB at 352MHz at full power.

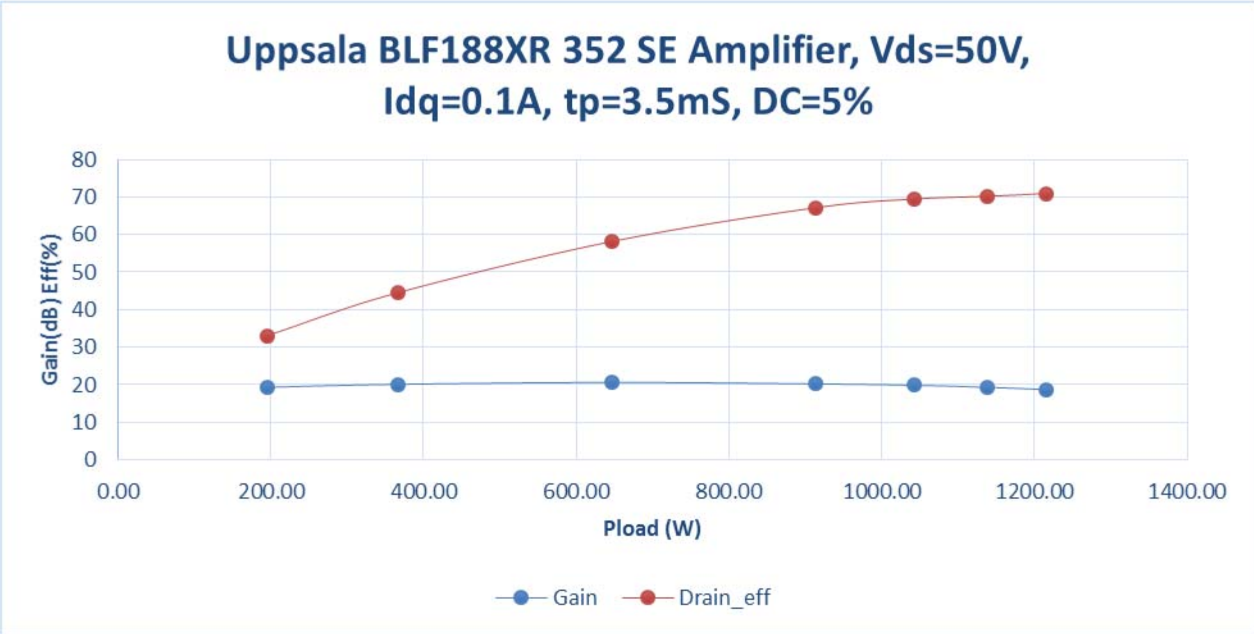


Fig 10. Pulsed power and Efficiency (Idq=0.1A, Vds=50 V, tp=3.5mS, Duty Cycle=5%)

In ESS mode, at 5% duty cycle, thermal effects are attenuated due to the larger time between pulses, allowing the amplifier to cool down in between pulses. Efficiency reaches 71% at an output power of 1250 W.

2.3 Harmonic signal levels

The harmonic suppression with regards the carrier frequency is measured and presented Table 2.

Table 2. Harmonic signal levels

Harmonic suppression wrt carrier, Vds=50V, Idq=0.2A, f=352MHz, 50 Ohm load
Pload = 1kW CW

Harmonic	Level (dB)
2nd	-25
3rd	-35
4th	-44
5th	<-60

Such low harmonic signal levels are unusual for a single ended amplifier design and are comparable to the harmonic levels of those amplifiers using baluns transformers. Therefore, an investigation of the transfer function of the output matching network was realized. In the following simulation, port 1 is the drain impedance for optimal PAE (0.341 + j0.464) and port 2 is the 50 Ohm output port. The output matching network behaves as a narrow band-pass filter, centred at the fundamental frequency of 352 MHz, i.e. the carrier frequency as can be seen in Fig 12. The insertion losses of the output matching network are low at the carrier frequency (IL = 0.1 dB) but are increasingly high with higher order harmonics (at 720 MHz, IL = 11 dB and at 1047 MHz, IL = 14 dB). The output matching network behaves like a lowpass network, filtering out harmonics and resulting in very good frequency behavior, as can be seen from the measurements in Table 2.

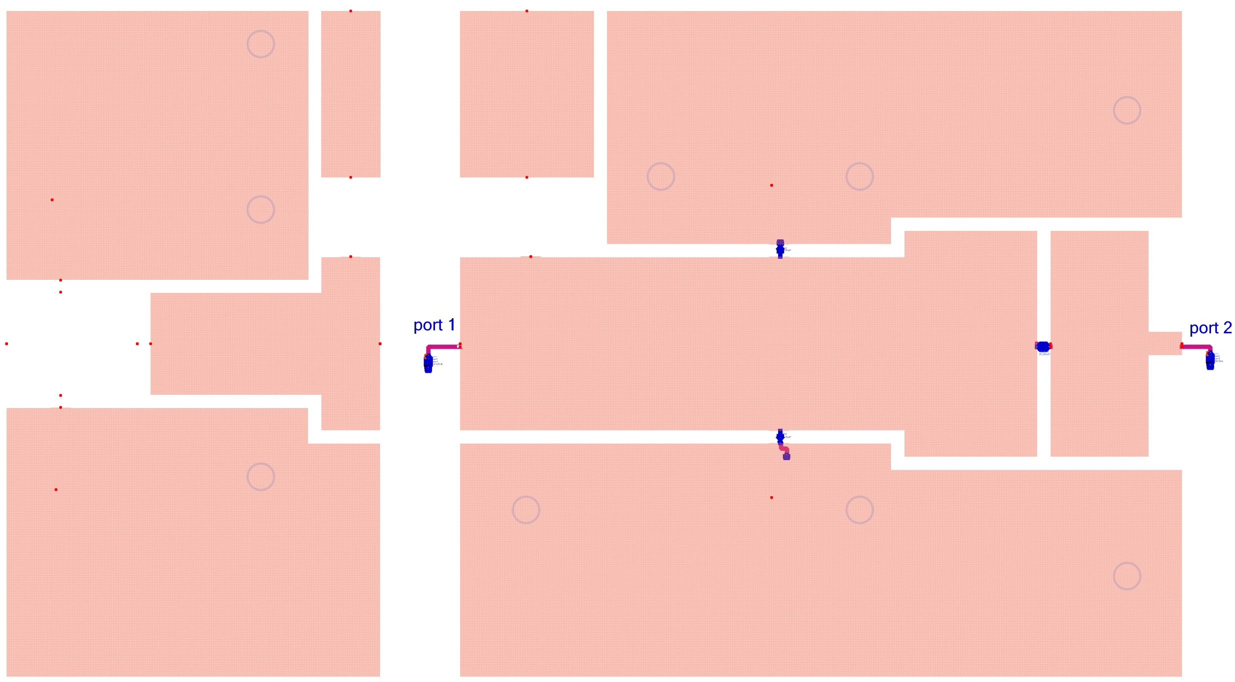


Fig 11. Evaluation of the output matching network transfer function and ADS simulation set-up

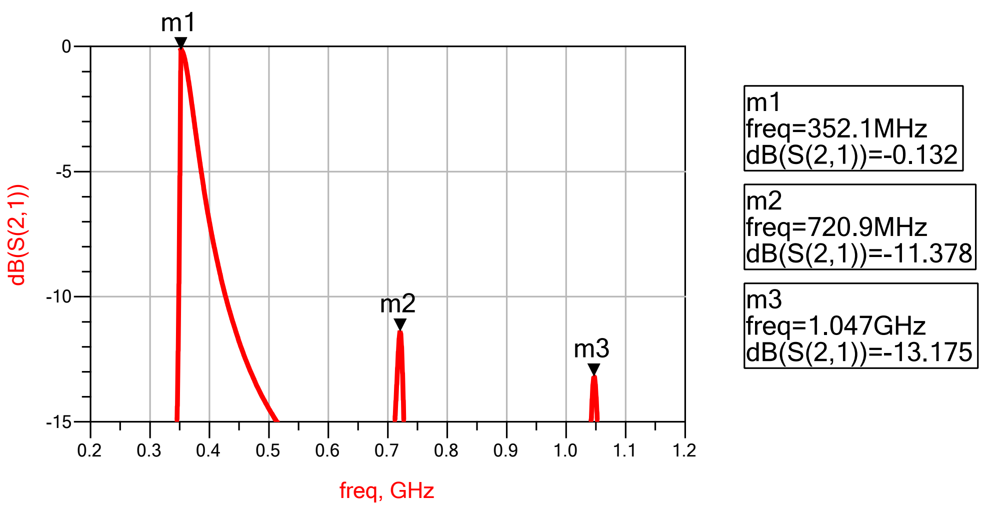


Fig 12. Filter behavior of the output matching network

2.4 Hot S-parameters measurements

The measured hot S-parameters of the demonstrator board are shown Fig 15. The S-parameters are measured in a frequency sweep of 25 MHz, between 340 and 365 MHz, while the carrier frequency is set at 352 MHz. The biasing conditions are: quiescent current IDq = 100 mA, drain voltage VDS = 50 V, Duty Cycle=5% and pulse period is 3.5 mS. The input impedance is well matched over the bandwidth, with an input reflection coefficient S11 roughly at -15 dB level for all measured output power. The output power spans over 50 W to 1300 W. A high variation of the transistor's output impedance with high output power is observed. The matching is fine-tuned for the maximum power measured of 1300 W. The equivalent output reactance is inductive and reduces with increasing output power, as can be seen Fig 13. Above 1000 W, the amplifier is into gain compression, and non linearities appear in the reactance. Output return loss, i.e. the Hot S22 parameter is also provided in a logarithmic scale as a function of output power, see Fig 14

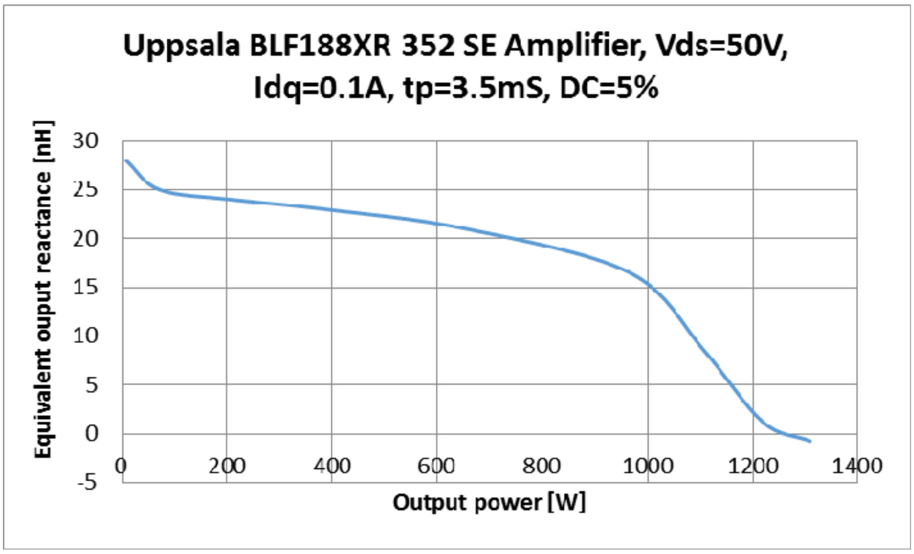


Fig 13. Equivalent output reactance as a function of output power

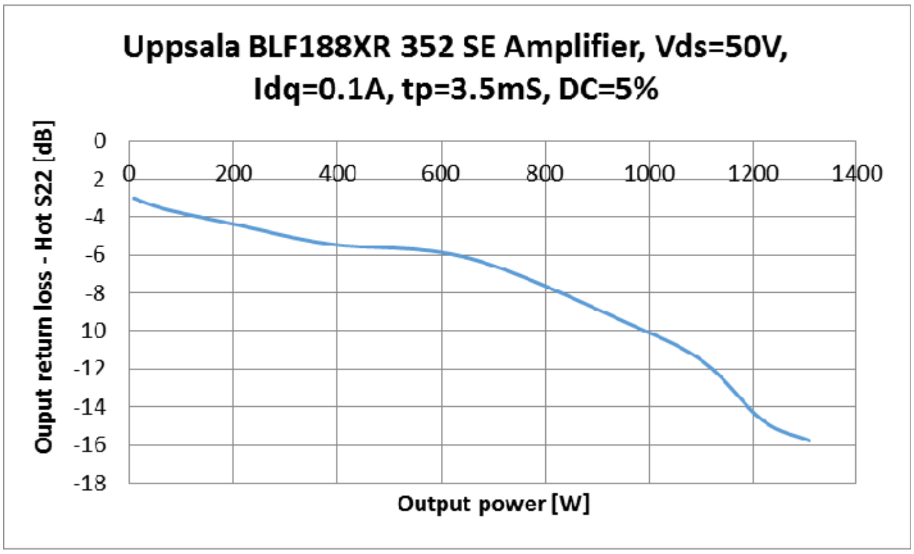
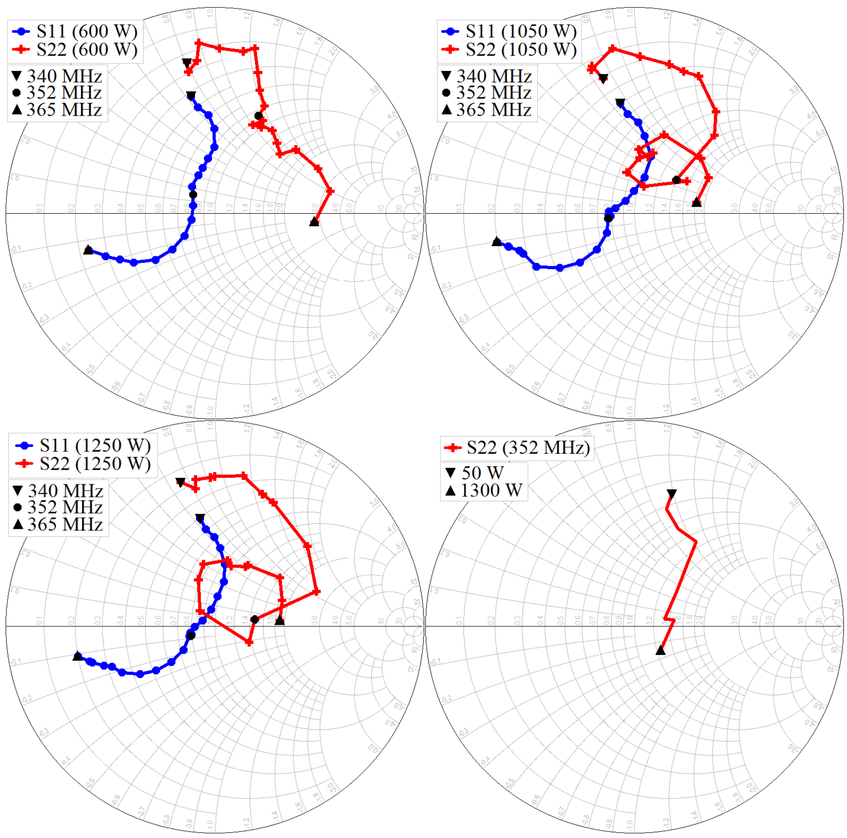


Fig 14. Output return loss – Hot S22 parameter as a function of output power



Vds=50V, Idq=0.1A, tp=3.5mS, duty cycle=5%

Fig 15. Hot S-parameters measured at different output powers and progression at 352 MHz

2.5 Thermal images of the amplifier under full CW load

Thermal images of the amplifier under ESS pulsed operation condition, i.e. pulse length 3.5 mS, 14 Hz repetition, Duty Cycle=5% at VDS =50V

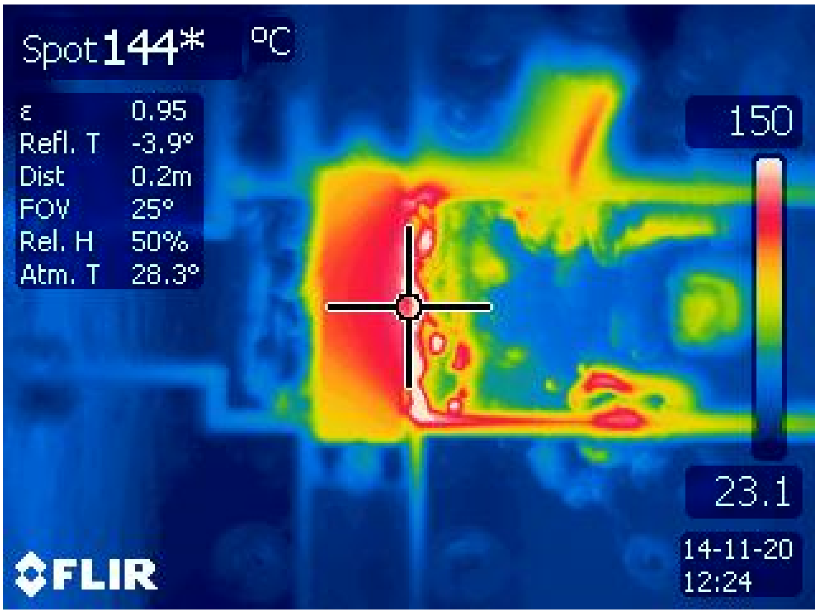


Fig 16. Thermal picture 1 @ Pload =1kW CW showing hotspots on the leads of the transistor

Showing hotspots on the leads of the transistor.

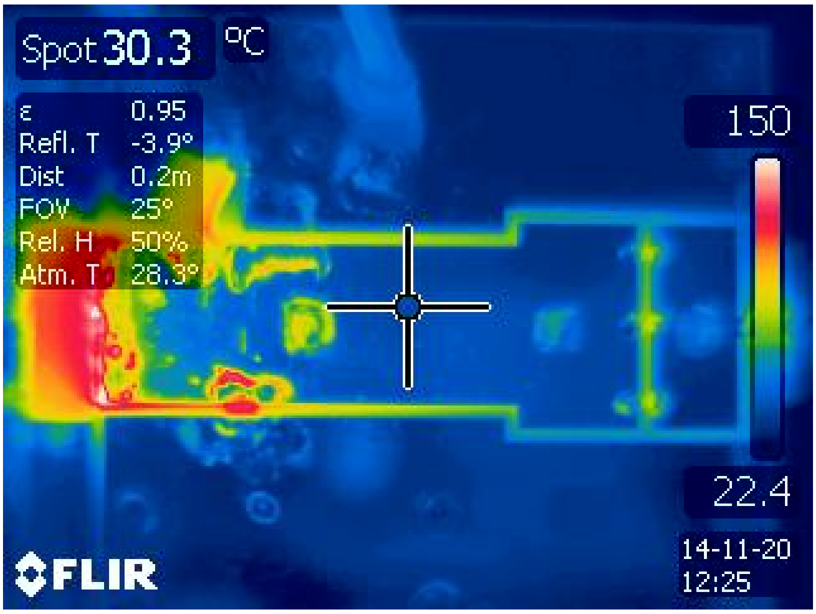


Fig 17. Thermal picture 2. @ Pload = 1kW CW. Thermally ok output circuit

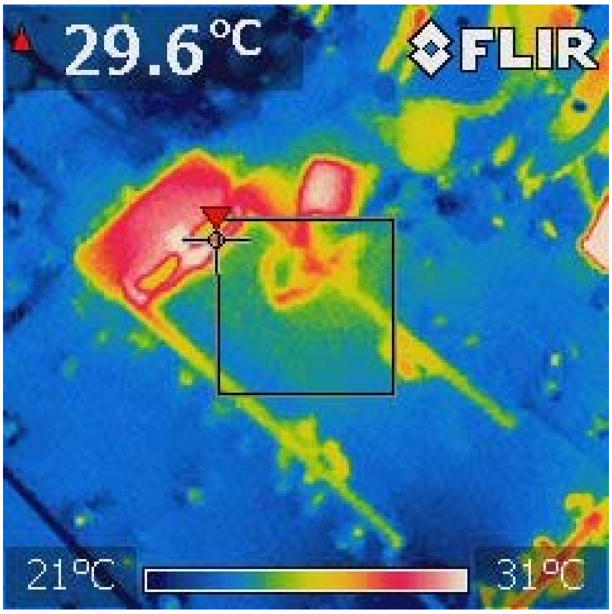


Fig 18. Thermal picture 3 @ Pload =1.3 kW, Duty Cycle=5%. Temperature is close to ambient

The temperature is about 30 C (room temperature is 20 C) when the amplifier is delivering 1300 W output power at 68% efficiency, with water cooling about 8 l/min.

2.6 Photographs of the Amplifier Board

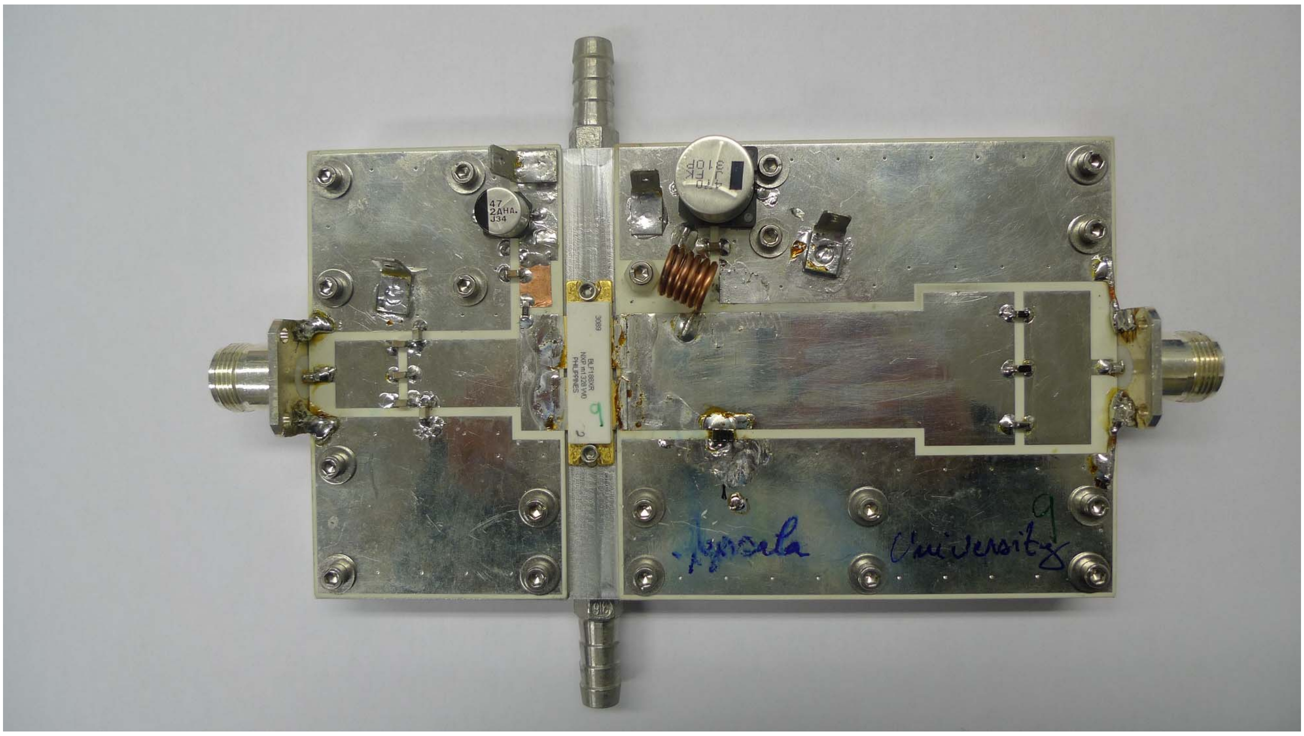


Fig 19. Overall layout of the amplifier

Fig 20. Transistor and 1 mm gap cavities. The drain is at the lower side of the image

3. Circuit details and evaluation

Below some improvements to the manufactured demonstrator to improve the CW capability.

Modification of the gate bias circuit;
Originally the gate bias was done by applying the gate voltage via a coil. This gave rise to some stability problems. To solve this, the gate bias circuit was slightly changed by connecting the bias via a resistor. In this way the gate bias voltage is applied via a 47 Ohms resistor. The Idq of the transistor can be adjusted to the correct value by starting at about 1 Volt and increasing the bias voltage slowly until the desired Idq is reached. The value needed for an I_{dq} of about 0.1A is around 1.6 V for a typical product.

Mounting of the transistor:
At high powers the BLF188XR needs an excellent thermal contact to the cooling plate. That is why it is absolutely necessary to use a thin layer of heat conducting compound between the transistor and the cooling plate. In this case heat compound of Austerlitz, type WPS2 was used.
The cavity in the cooling plate should be fitting the size of the transistor flange. In the amplifier the cavity is too wide, presently 12 mm. Although this is not an RF problem it results in a lack of cooling at the transistor leads, as the leads are in air for a length of about 1mm, clearly visible in Fig 20. If the lead would be soldered over the complete length to the board, this would cool the lead, reduce the thermal impedance and the hot spot would be much smaller. Dimensions for the cavity size and drill distances of the mounting holes (should be10 mm instead) can be found in AN10896 [7].

[7] AN10896 - Application note - Mounting and Soldering of RF transistors. Rev. 2 — 13 Nov 2012

Matching capacitors:
In the original design the matching capacitor (15 pF) close to the drain was over heating at full CW power (1kW). This is why the capacitor was split in three ATC 800B capacitors to lower the heat dissipation per capacitor. Fig 17 shows a thermal image of the complete output circuit under full load conditions. The matching capacitors are at an acceptable temperature.

Vias in the output matching circuit:
In the output circuit the vias are distributed with a spacing of about 10mm. It would be beneficial for the performance of the amplifier to greatly increase the numbers of vias. This is necessary because high currents are flowing in the ground vias.

Increasing the device bias, I_{DQ}
The bias setting may need to be increased. It has been seen during some stability testing of other parts in this device family that an I_{DQ} setting of 1A helped increase the stability of the circuit. The present setting is 100mA. Increasing the gate bias will have the effect of increasing the gain, slightly decreasing the efficiency, and slightly lowering the output power for a given level of compression. The peak power capability of the part should remain unchanged, however.

Output matching network

The output matching network can be improved by smoothly increasing the output impedance till 50 Ohm.

4. Conclusions

The single ended BLF188XR amplifier design and manufactured by Uppsala University can produce 1.3kW with an efficiency of 60 (CW) – 68% (pulsed) at 352MHz.

In ESS mode, i.e. Duty Cycle=5%, pulse duration of 3.5ms and 14 Hz repetition, the demonstrator amplifier's temperature is close to the ambient temperature: the temperature is about 30 C (room temperature is 20 C), with water cooling debit of about 8 l/min. Thermal effects are attenuated due to the larger time between pulses, allowing the amplifier to cool down in between pulses. Efficiency reaches 71% at an output power of 1250 W.

Hot S-parameters measurements allow fine tuning the output impedance, for high output power. The output matching network results in a low pass circuit, filtering out harmonics. An increase of the gain can be obtained with higher quiescent currents, which is trade off because it will somewhat decrease the drain efficiency.

The use of the transistor in single ended mode makes the circuit attractive because it is relatively simple compared to the amplifiers using Planar – or Coax baluns in a push pull configuration.

By including the mentioned improvements and some more fine tuning it will be possible to improve the performance of the amplifier

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6. Contents

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