AN11520

Life-time requirements of HVSON12 high-voltage (50 V) plastic drivers

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Document information

Info	Content
Keywords	BLP10H610, LDMOS, HVSON12
Abstract	This application note describes the process of how to operate Ampleon drivers safely, using the HVSON12 package within its associated life-time requirements. It describes the life-time requirements, the relation with thermal resistance and the thermal environment. The BLP10H610 is taken from the Ampleon plastic driver portfolio as an example to relate these requirements to a CW application condition.

Revision history

Rev	Date	Description
AN11520#2	20150901	Modifications - The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. - Legal texts have been adapted to the new company name where appropriate.
AN11520#1	20140404	Initial version

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1. Introduction

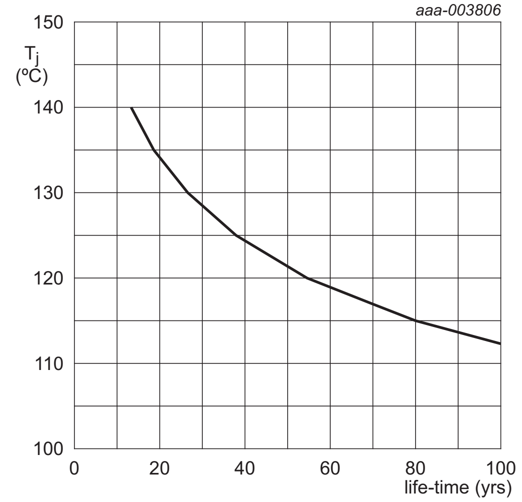
In the semiconductor industry of today, it is accepted that using a product within its life-time requirement is of upmost importance to guarantee a successful design.

This application note shows how to operate Ampleon driver products in an HVSON12 package within their life-time requirements.

The low-power driver BLP10H610 using Ampleon state of the art GEN6 HV LDMOS technology is used as the leading example. This device is perfectly suitable as a general-purpose driver in the HF to 1400 MHz frequency range.

2. Life-time

The limiting factor for the life-time of the current HVSON12-like package is the bond wire to bonding pad interconnect. The life-time graph for this interconnect is presented in Figure 1:



The absolute maximum rating of the Ampleon HVSON12 driver products is 150 °C.

The life-time is defined as 0.1 % failures of the tested interconnects, that is the interconnect shows a degradation that crosses a critical point.

Fig 1. Ampleon HVSON12 life-time in relation to junction temperature

Figure 1 shows the relation between junction temperature (T_j) and life-time ($t_{life\text{-}time}$). It shows that life-time can be increased by maintaining lower junction temperatures.

The achievable life-time depends on the application in which the product is used and determines the maximum allowable junction temperature of the device in that application. This maximum allowable junction temperature sets a boundary condition for performance and thermal budget calculations.

The maximum junction temperature depends on:

- The dissipated power; P_{diss}

- The product thermal resistance from junction to case; $R_{th(j\text{-}c)}$
- The product mounting thermal resistance; $R_{th(c\text{-}h)}$
- The heatsink temperature; T_h.

The dissipated power depends on the application conditions and can be calculated from Equation 1.

$$P_{diss} = \frac{1 - \eta_D}{\eta_D} \times P_{out} \quad (1)$$

where: η_D is the drain efficiency and P_{out} is the average output power.

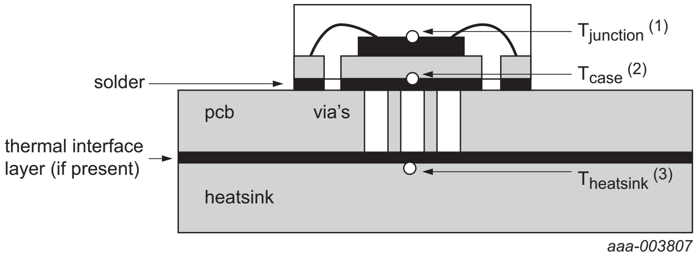
The life-time requirement sets the junction temperature and the application determines the power dissipation. As a result, these parameters set the boundary conditions for the thermal resistances as indicated by Equation 2 and Equation 3.

$$R_{th(j-case)} = \frac{T_j(t_{life-time}) - T_{case}}{P_{diss}(\eta_D, P_{out})} \quad (2)$$

$$R_{th(j-h)} = R_{th(j-case)} + R_{th(case-h)} = \frac{T_j(t_{life-time}) - T_h}{P_{diss}(\eta_D, P_{out})} \quad (3)$$

where: T_{case} is the case temperature of the product.

The $R_{th(j\text{-}h)}$ is very useful to determine the contribution of the material stack and is used together with the $R_{th(j\text{-}c)}$ in this document. In order to determine T_j, T_{case} and T_h temperatures, they are defined in Figure 2.



(1) T_j is defined as the maximum die surface temperature.
(2) T_{case} is defined as the maximum temperature of the products heatsink bottom surface.
(3) T_h is defined as 1 mm below the surface of the cooling heatsink, in the center of the product.

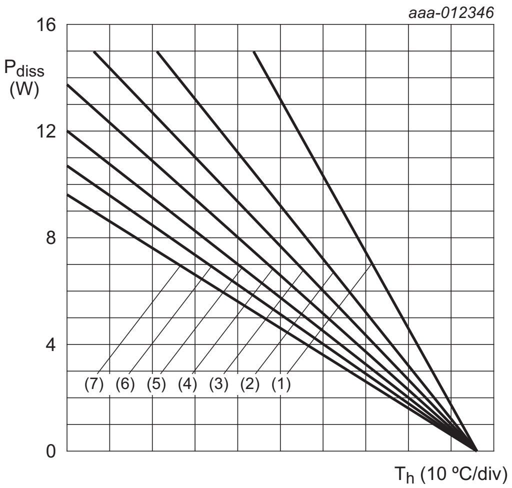
Fig 2. Thermal resistance stack

Figure 2 shows a basic setup used for thermal characterization of Ampleon HVSON12 driver products. It consists of:

- A solder layer between the product and PCB (Printed-Circuit Board).
- A PCB with vias in a regular pattern for conduction of the generated heat.
- A thermal paste between the PCB and heatsink.
- A heatsink to sink the heat to the environment.

The thermal design is optimized in the application field. Describing such optimizations is outside the scope of this application note.

To visualize and enhance the usability of Equation 2 and Equation 3, a graphical representation is shown in Figure 3.



(1) $R_{th(j-h)} = R_{th(j-c)} = 3.5$ K/W with $R_{th(c-h)} = 0$ K/W.
(Curve 1 is a special case with $R_{th(c-h)} = 0$ K/W resulting in $R_{th(j-h)} = R_{th(j-c)}$ and $T_h = T_{case}$.
(2) $R_{th(j-h)} = 5$ K/W.
(3) $R_{th(j-h)} = 6$ K/W.
(4) $R_{th(j-h)} = 7$ K/W.
(5) $R_{th(j-h)} = 8$ K/W.
(6) $R_{th(j-h)} = 9$ K/W.
(7) $R_{th(j-h)} = 10$ K/W.

Fig 3. Graphical representation of relation between life-time and thermal environment

The x-axis represents the heatsink temperature (or case temperature for curve$^{(1)}$). The point on the right lower corner of the graph T_j ($t_{life-time}$) represents the allowed junction temperature. It corresponds to a certain life-time, as required by the application and/or end user and can be determined from Figure 1.

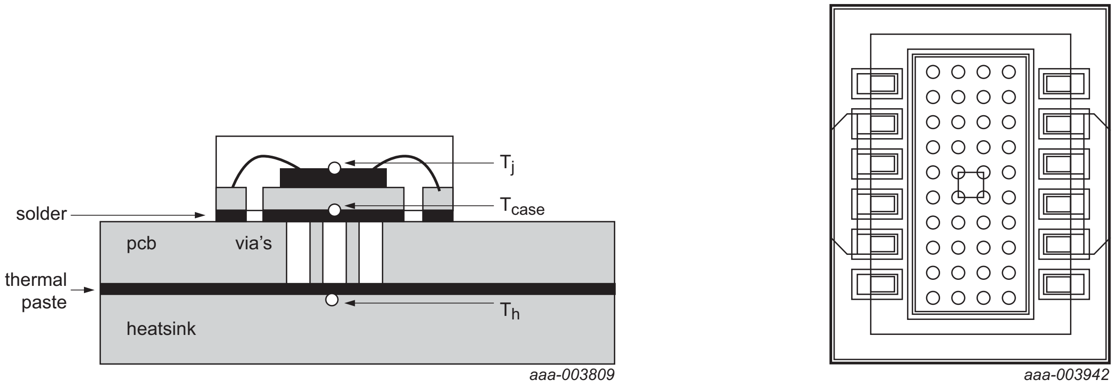
The application according to Equation 1 determines the power dissipation on the y-axis.

The product provides curve$^{(1)}$ which represents the $R_{th(j-c)}$. Curves$^{(2)}$ to $^{(7)}$ represent different $R_{th(j-h)}$ cases.

Based on this figure, the trade-off between T_h, T_c and $R_{th(j-h)}$ can be determined within the required life-time and dissipated power.

3. Thermal characterization

In order to have a successful and reliable thermal design, accurate characterization of the thermal resistance is crucial. To determine the thermal impedances $R_{th(j-c)}$ and $R_{th(j-h)}$, the product is soldered on a Printed-Circuit Board (PCB) as depicted in Figure 4.



a. Thermal resistance stack

b. Via design

Fig 4. Material stack used for thermal characterization

Figure 4a shows the thermal resistance stack as discussed in Section 2, in which the BLP10H610 is characterized. Figure 4b shows the used via pattern. The material properties of the stack are listed in Table 1

Table 1. Thermal resistance stack

Layer	Material	Dimensions
solder	17.2	-
metal PCB top	copper	35 μm
PCB	Rogers 4350	0.762 mm
thermal vias	-	vias[1] 4 × 10 = 40; D = 0.25 mm; via spacing 0.5 mm
metal PCB bottom	copper	35 μm
thermal paste	industry standard	50 μm
heatsink	brass R001	12 mm

[1] The vias are implemented in a regular pattern and can be subjected to further optimization.

Based on Figure 4 and Table 1, the thermal resistance values $R_{th(j-c)}$ and $R_{th(j-h)}$ for BLP10H610 have been measured as follows:

$R_{th(j-c)} = 3.5$ K/W.

$R_{th(j-h)} = 6.1$ K/W.

4. Design example BLP10H610

This section uses a step-by-step approach. It demonstrates how to design thermal parameters in relation to application conditions to operate the BLP10H610 safely within the life-time requirements. A 1-tone CW application condition is used as an example.

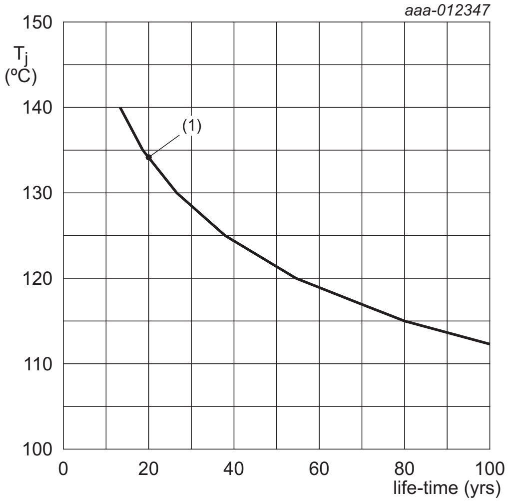
4.1 Step 1: determine the life-time requirement

The required life-time of a product is in essence determined by the end-user requirement and can vary for different application conditions.

In this example, a minimum life-time ($t_{life\text{-}time}$) of 20 years is taken.

4.2 Step 2: determine the maximum junction temperature

The minimum life-time of 20 years is used in Figure 5 to determine the maximum junction temperature T_j ($t_{life\text{-}time}$) in the application. The maximum junction temperature is 134 °C.



(1) T_j = 134 °C; $t_{life\text{-}time}$ = 20 years

Fig 5. Determine the maximum junction temperature

4.3 Step 3: determine the power dissipation

The power dissipation (P_{diss}) can be calculated from Equation 1 by using the typical 1-tone CW application performance as listed in Table 2.

Table 2. Application performance
Typical RF performance at T_{case} = 25 °C; I_{Dq} = 60 mA; in a class-AB application circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	IMD3	ACPR
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)	(dBc)
1-tone CW	860	60	50	10	22	60	-	-

The power dissipation is 6.7 W.

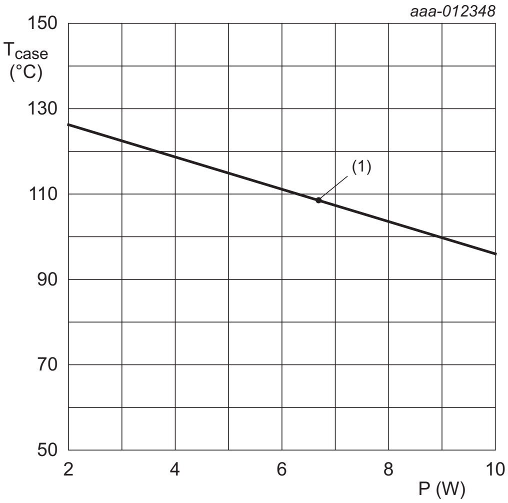
4.4 Step 4: determine the thermal resistances

The thermal resistances consist of the product resistance $R_{th(j-c)}$ and the product mounting resistance $R_{th(j-h)}$.

- The product determines the $R_{th(j-c)}$ which is 3.5 K/W
- The product determines the $R_{th(j-h)}$ by mounting method. It is 6.1 K/W for the material stack, as shown in Figure 4a.

4.5 Step 5: determine the maximum heatsink and case temperatures

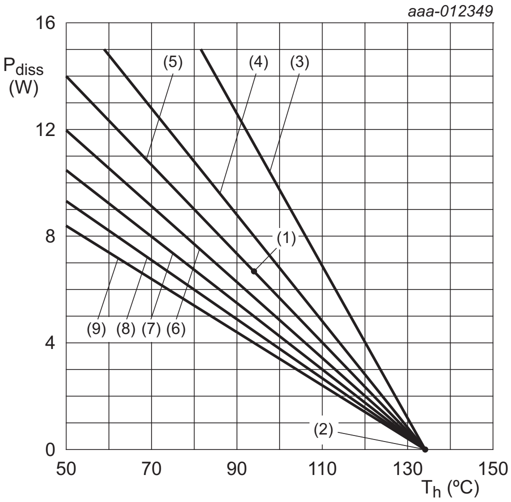
In this step, maximum junction temperature, dissipated power, and thermal resistances are used to determine maximum heatsink and case temperatures (see Figure 6 and Figure 7).



(1) T_{case} = 109 °C; P = 6.7 W.

Based on worst case $R_{th(j-c)}$.

Fig 6. BLP10H610: Recommended operating area, case temperature as a function of power dissipation



(1) $T_{h(max)}$ = 94 °C; P_{diss} = 6.7 W.

(2) T_j = 134 °C.

(3) $R_{th(j-h)} = R_{th(j-c)}$ = 3.5 K/W with $R_{th(c-h)}$ = 0 K/W.

(4) $R_{th(j-h)}$ = 5 K/W.

(5) $R_{th(j-h)}$ = 6 K/W.

(6) $R_{th(j-h)}$ = 7 K/W.

(7) $R_{th(j-h)}$ = 8 K/W.

(8) $R_{th(j-h)}$ = 9 K/W.

(9) $R_{th(j-h)}$ = 10 K/W.

Fig 7. BLP10H610: Graphical representation of relation between life-time and thermal parameters

Figure 6 shows the recommended operating area for T_j = 134 °C as presented in the data sheet. It shows that for 6.7 W power dissipation, the maximum case temperature is 109 °C. The maximum heatsink temperature can be obtained from Figure 7 and is 94 °C.

4.6 Step 6: check the case temperature

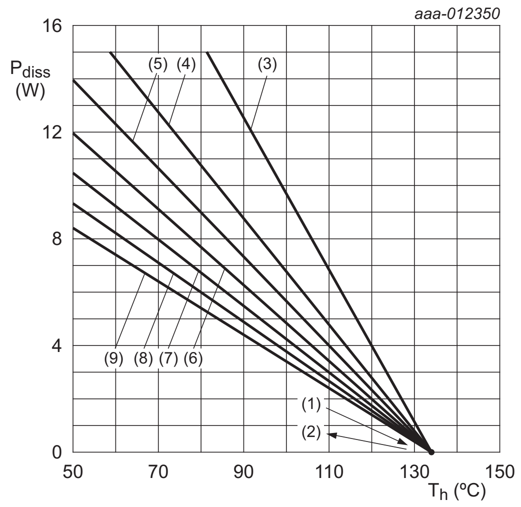
In Step 5, it was determined that the maximum allowed case temperature is 109 °C.

In general, the following limit the maximum case temperature:

1. The MOT (Maximum Operating Temperature) of the PCB material in use. The MOT is the maximum temperature at which the PCB can be operated for an indefinite period without significant degradation.
2. Reliable operation of the solder between the product case and the PCB. In this application, a value of 110 °C is used. If the case temperature is higher than 110 °C, follow Section 4.6.1 “Step 6-1: recalculation of the junction and heatsink temperatures” and Section 4.6.2 “Step 6-2: recalculation of the product life-time”.

4.6.1 Step 6-1: recalculation of the junction and heatsink temperatures

A decrease of case temperature necessitates a recalculation of the junction and heatsink temperatures as shown in Figure 8.



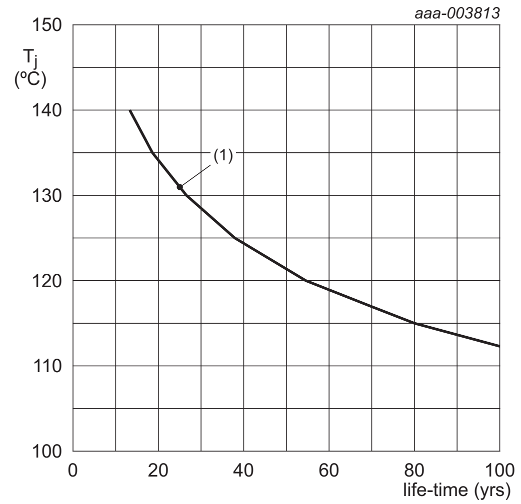
(1) T_j.
(2) $T_j - \Delta T$.
(3) $R_{th(j-h)} = R_{th(j-c)} = 3.5$ K/W with $R_{th(c-h)} = 0$ K/W.
(4) $R_{th(j-h)} = 5$ K/W.
(5) $R_{th(j-h)} = 6$ K/W.
(6) $R_{th(j-h)} = 7$ K/W.
(7) $R_{th(j-h)} = 8$ K/W.
(8) $R_{th(j-h)} = 9$ K/W.
(9) $R_{th(j-h)} = 10$ K/W.

Fig 8. BLP10H610: Recalculation of junction and heatsink temperatures

Recalculation is nothing more than applying a temperature shift of a lower junction temperature ($T_j - \Delta T$) and a maximum heatsink temperature ($T_h - \Delta T$).

4.6.2 Step 6-2: recalculation of the product life-time

The decrease in junction temperature increases the product life-time as shown in Figure 9.



(1) T_j ($t_{lifetime}$) = (T_j – ΔT) °C; $t_{lifetime}$ = $t_{lifetime}$(T_j – ΔT) years

Fig 9. Recalculation of product life-time

The product life-time is increased from 20 years to $t_{lifetime}$(T_j – ΔT) years.

4.7 Step 7: check the heatsink temperature

The heatsink temperature is determined to be 94 °C in Section 4.5 “Step 5: determine the maximum heatsink and case temperatures”.

The ability to keep the heatsink temperature below this temperature depends on the environmental temperature conditions in which the product is operating and the cooling capacity.

If higher heatsink temperatures are required, optimization of the thermal resistance stack is required. Figure 7 can be used to trade off heatsink temperature (T_h) and the total thermal resistance $R_{th(j-h)}$.

4.8 Thermal design summary

Based on the steps taken, the following thermal design is acquired as described in Table 3

Table 3. BLP10H610 thermal design summary

1-tone CW; f = 860 MHz

Type number	Life-time ($T_{life-time}$)	Junction temperature (T_j)	Case temperature (T_{case})	Heatsink temperature (T_h)	Thermal resistance junction to heatsink ($R_{th(j-h)}$)
BLP10H610	20 years	134 °C	109 °C	< 94 °C	6.1 K/W

5. Abbreviations

Table 4. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MOT	Maximum Operating Temperature
CW	Continuous Wave

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7. Tables

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