# AN11325

## 2-way Doherty amplifier with BLF888A

Rev. 2 — 1 September 2015

Application note

### Document information

| Info | Content |
|---|---|
| **Keywords** | BLF888A, Doherty, DVB-T, UHF |
| **Abstract** | This document gives a description and measurement results of a 2-way Doherty amplifier using 2 × BLF888A UHF LDMOS transistors. |

### Revision history

| Rev | Date | Description |
|---|---|---|
| v.2 | 20150901 | Modifications<br>• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.<br>• Legal texts have been adapted to the new company name where appropriate. |
| v.1 | 20131114 | Initial version |

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# 1. Introduction

The document introduces a narrowband 2-way Doherty amplifier (test) demo board. Using the board together with modeling software and measuring test equipment, details of amplifier designs for three DBV-T frequencies are given. The process of the designs and the measurements and modeling results are also given.

The test board comprises one PCB containing the broadband main and peaking amplifiers, and a second PCB containing the Doherty combiner. The main and peaking amplifiers each uses a BLF888A UHF LDMOS transistor, together with associated components. The broadband amplifier blocks cover the whole UHF band.

Amplifier bandwidth and base frequency is dependent on the Doherty combiner design. Several narrowband design versions of the Doherty combiner PCB can be built and interchanged on the demo board to determine the required amplifier frequency.

The amplifier has minimum output power of 200 W average (DBV-T) and approximately 50 MHz of bandwidth (depending on the center frequency).

Further details of the demo board operating conditions can be found at Section 6.

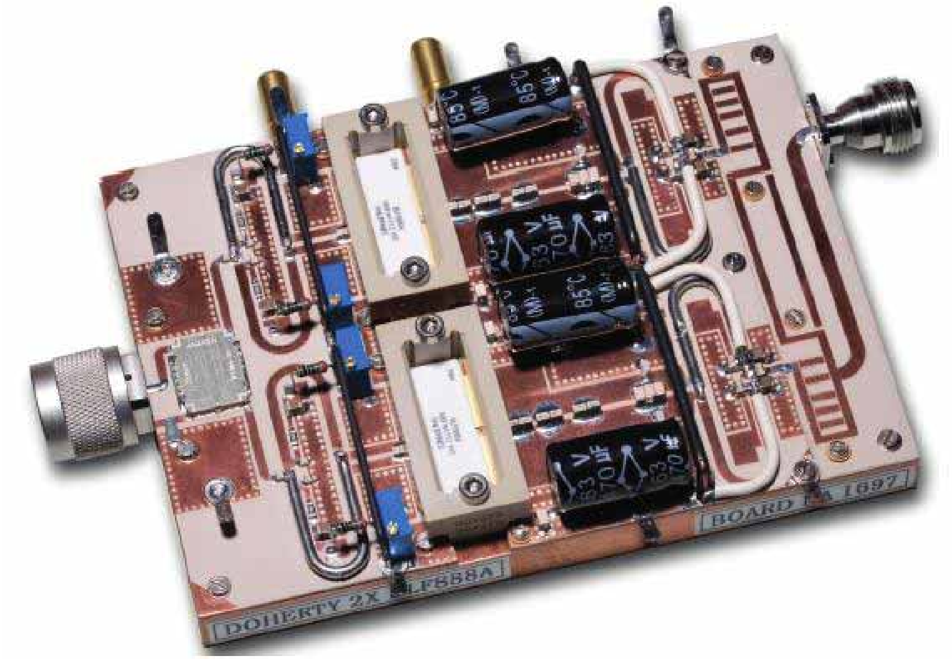


**Fig 1. Doherty amplifier demo board**

# 2. Test circuit

The test board contains two broadband BLF888A amplifiers on one common PCB (for main and peaking). The electrical circuit is completed with a Doherty combiner on a separate PCB. This combiner PCB can be replaced by another unit when changing to another frequency. The bandwidth of the Doherty amplifier is limited to approximately

50 MHz. The broadband 50 Ω amplifiers cover the whole UHF band and are not further optimized for Doherty operation. An advantage is that only the Doherty combiner needs to be redesigned per frequency band. The disadvantage is the lower efficiency compared to a narrow band design of the amplifier blocks.

The main amplifier operates in class AB and the peaking amplifier operates in class C.

The Doherty combiner consists of two offset lines (main/peaking) and a 90° transmission line (impedance inverter). The matching to 50 Ω is achieved by the addition of a 35 Ω transmission line (25 Ω to 50 Ω). This is less critical in design. Section 3 discusses the combiner offset lines.

# 3. Measurement and modeling

The characteristics of the offset lines were determined by measurement and modeling.

## 3.1 Measurement with Network Analyzer

By the use of test structures (Figure 2 and Figure 3), offset lines were measured using a network analyzer for S11 as a function of frequency (see Figure 4).

The test structures can be put on the module instead of the separate Doherty combiner PCB. By putting the supply voltage on the peaking amplifier only and choosing the right length on the PCB, the offset line can be measured. The length can be chosen by soldering the links on the PCB.

Connect the peaking amplifier and select a length on the test structure. The center frequency of the offset line is then the point where the impedance is infinite on the Smith chart (Figure 4).

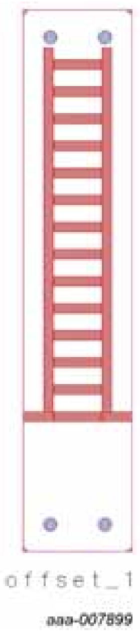


**Fig 2.** Test structure: offset 1

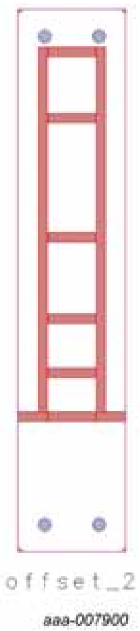
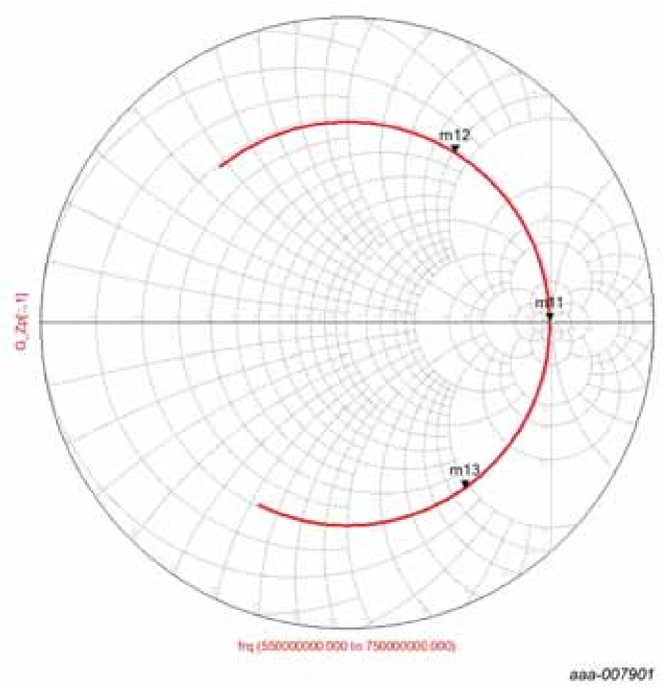


**Fig 3.** Test structure: offset 2



f = 550 MHz to 750 MHz
m11: f = 650 MHz
m12: f = 600 MHz
m13: f = 700 MHz

**Fig 4. Offset line length determination with an 'open' Smith chart.**

- The same offset lines were used for both Main and Peaking amplifier.
- The ideal offset line of the peaking amplifier is open at the combiner point (see Figure 4).
- Pulsed measurement (efficiency) at back-off power showed that this was also correct for the main amplifier.

## 3.2 Modeling

The characteristics of the offset line can be determined by passive models (equivalent), or active models of the transistor. Both methods give similar results. Figure 5 shows the broadband (peaking) amplifier output matching (block X5, BB_output_888A) and the active models (component X2 and X7). Figure 6 shows the broadband matching configuration of BLF888A in detail.

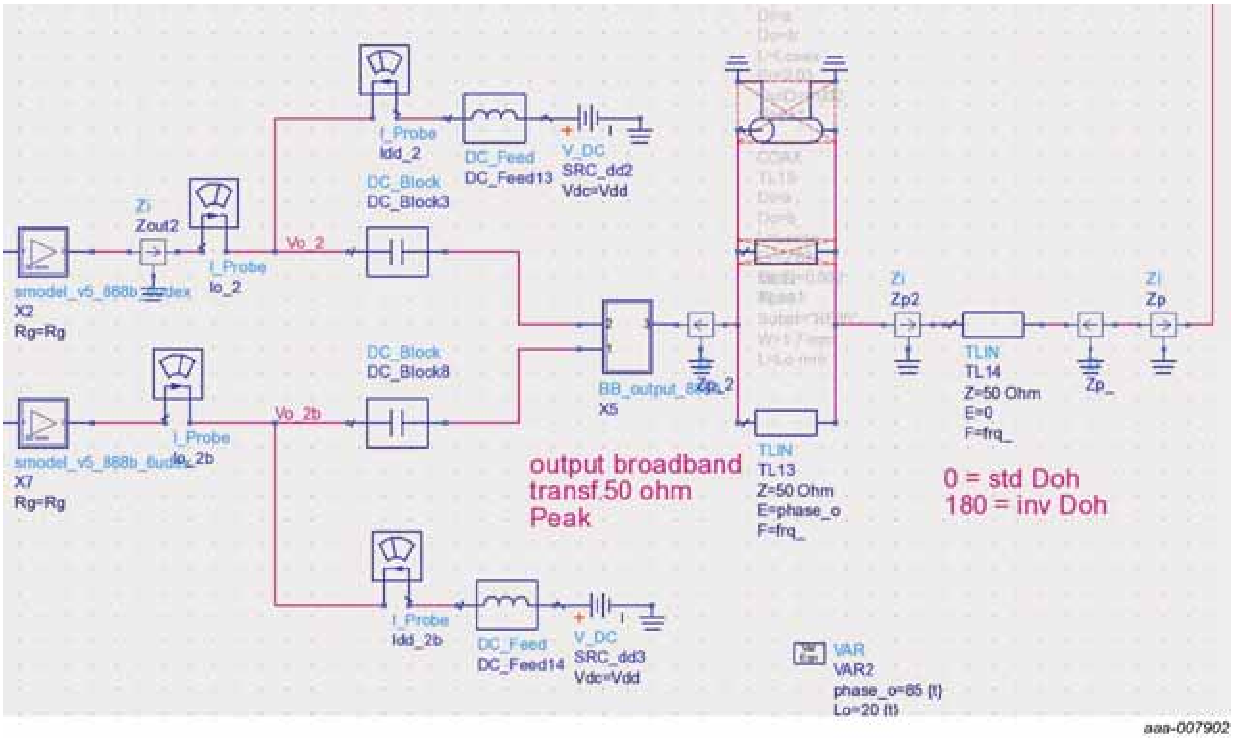


**Fig 5. Active model for determination of offset lines**

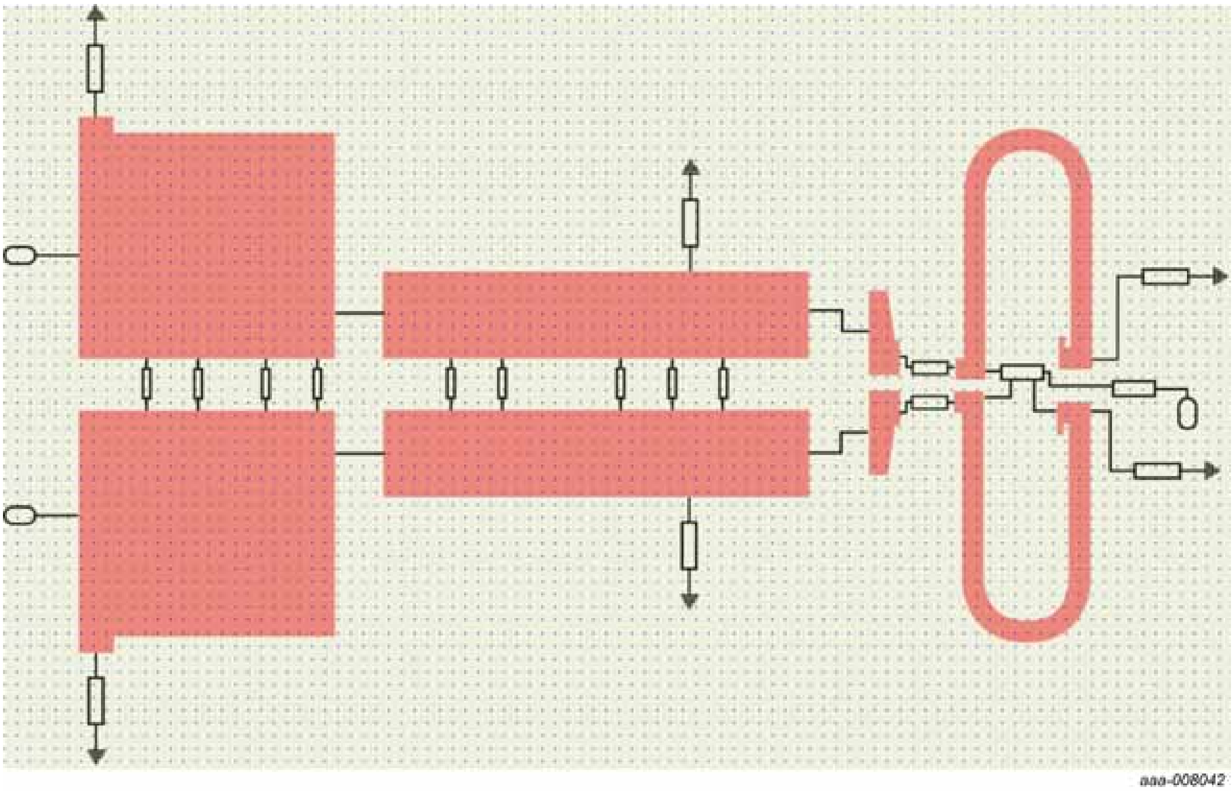
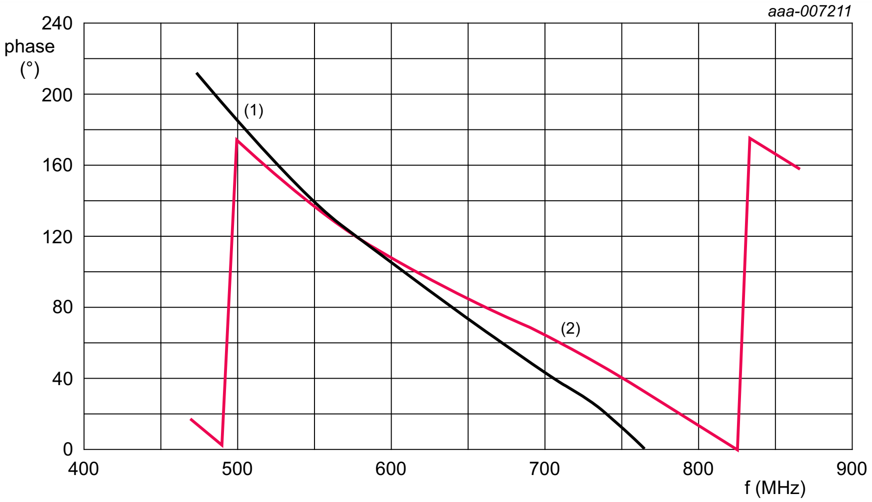


Fig 6. Broadband matching block BLF888A

## 3.3 Measurement results

Figure 7 and Figure 8 give a graphical representation of the model measurement and simulation. The offset line values are given in degrees and millimeters (length for Taconic RF35 and coaxial cable).

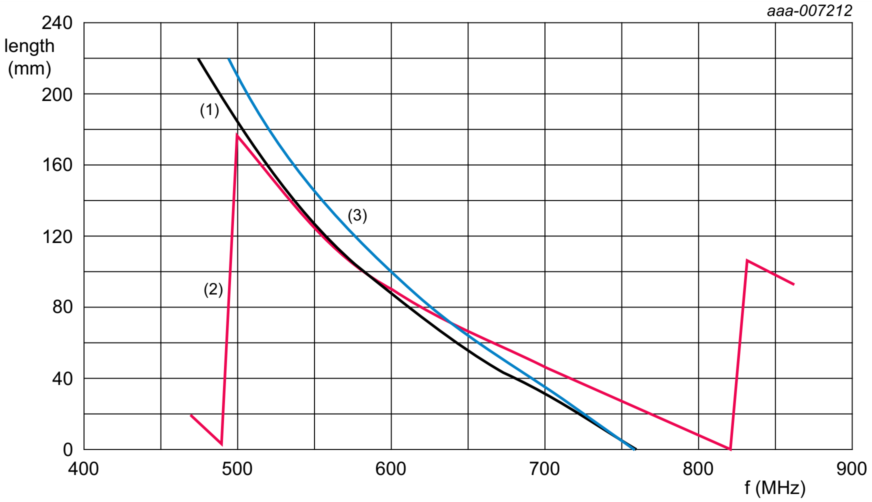
Note that the simulation shows a small error at the higher frequencies due to the inaccuracy of the transistor model and broadband matching block.



(1) Offset line determination via Network analyzer (PCB; $\varepsilon_r$ = 3.5)

(2) Offset determination via ADS model

**Fig 7. Peaking amplifier: offset line determination via ADS model and network analyzer measurement in degrees**



(1) Offset line determination via Network analyzer (PCB; $\varepsilon_r$ = 3.5)

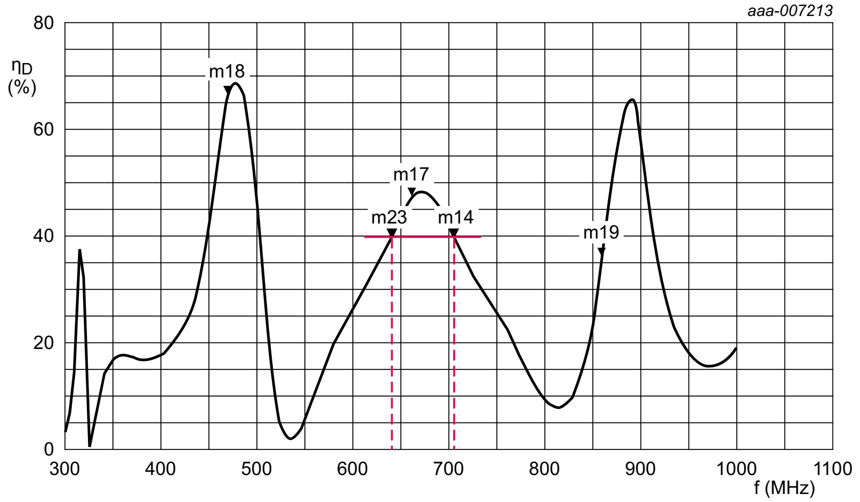
(2) Offset determination via ADS model

(3) Recalculated offset line from Figure note 1 for coaxial cable

**Fig 8. Peaking amplifier: offset line determination via ADS model and network analyzer measurement as a function of length in millimeters**

# 4. Bandwidth in UHF

Simulation shows that a bandwidth of this design, with a midband at approximately 650 MHz, is limited to approximately 50 MHz, which is the minimum (40 %) efficiency with a DVB-T signal.



m18 = 470 MHz at $\eta_D$ of 65 %

m17 = 665 MHz at $\eta_D$ of 47 %

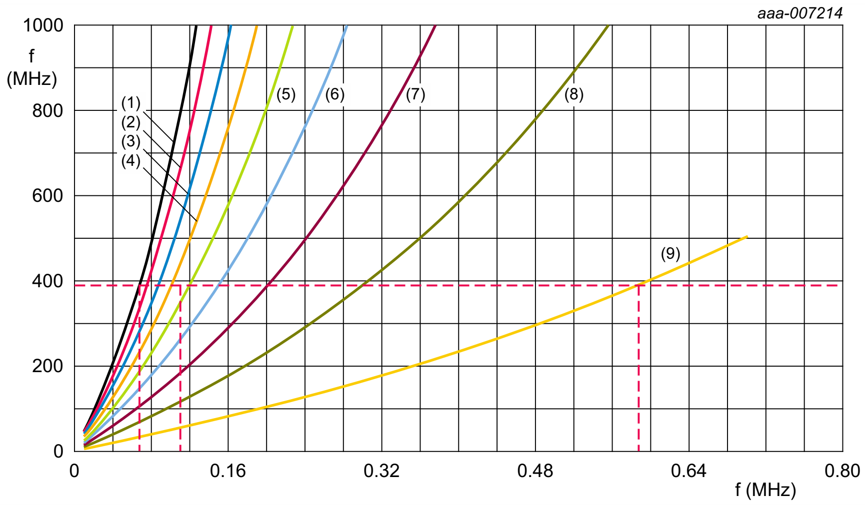
m23 = 640 MHz at $\eta_D$ of 39 %

m14 = 705 MHz at $\eta_D$ of 40 %

m19 = 860 MHz at $\eta_D$ of 36 %

**Fig 9. Simulation in back-off at center frequency**

The number of different Doherty combiner designs to cover the whole UHF band can be determined from Figure 10. For example, a fractional bandwidth of 0.07 results in nine different combiner designs, while a fractional bandwidth of 0.11 results in six different combiner designs. A full band design (470 MHz to 860 MHz) would need a fractional bandwidth of approximately 0.6.



Bandwidth (Q) 470 MHz to 860 MHz

(1) number of designs = 9
(2) number of designs = 8
(3) number of designs = 7
(4) number of designs = 6
(5) number of designs = 5
(6) number of designs = 4
(7) number of designs = 3
(8) number of designs = 2
(9) number of designs = 1

**Fig 10. Number of Doherty designs as a function of relative bandwidth (Q) and absolute bandwidth (B)**

# 5. Narrowband designs

## 5.1 Summary

In total four combiner designs were created and tested:

- 675 MHz
- 710 MHz
- 770 MHz
- 500 MHz

The 675 MHz and 710 MHz designs are similar, only differing in the 90° line.

The combiner lengths are shown in Table 1.

Note that:

- The 500 MHz design is not made on the combiner PCB because of the size of the offset lines (design with coaxial cables)

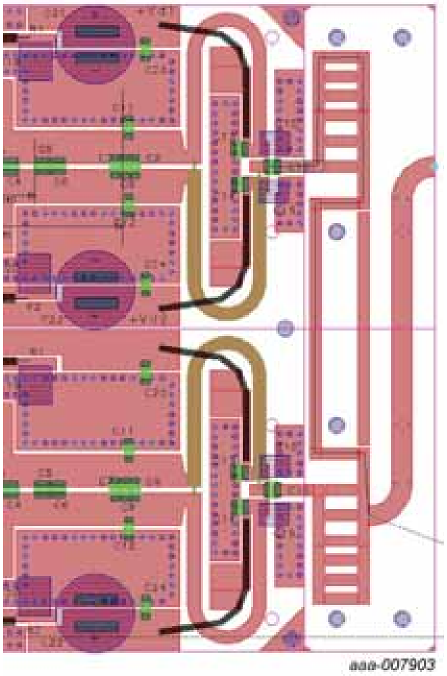
- The offset line length at 675 MHz is not optimum and this will result in slightly lower efficiency compared to 710 MHz
- The broadband matching of the amplifier blocks has a significant influence on the measured efficiency
- The broadband amplifiers were not correctly tuned below 500 MHz which influenced the result of the 500 MHz design at the lower frequencies
- In some measurements, extra attenuation at the input of the main amplifier was added (parallel 50 Ω resistor to ground). This only gave slightly better results. This was frequency-dependent due to the changing input matching over frequency. A better option would be to use an asymmetrical splitter design.

**Table 1. Combiner characteristics**

| f (MHz) | Simulation offset line Peaking amp | | | Peaking amp | | Main amp | |
|---|---|---|---|---|---|---|---|
| | Phase offset line (°) | Length (mm) $\varepsilon_r$ = 3.5 | Length (mm) $\varepsilon_r$ = 2.03 (coax) | Length offset line (mm) | Actual length offset line (mm) | Length offset line +90° (mm) | Actual length offset line +90° (mm) |
| 470 | 18 | 19 | 22.40 | | | 115.23 | |
| 500 | 175 | 177 | 204.71 | | | 267.45 | |
| 500 | | | | 200 | 200 (coaxial) | | 300 (coaxial) |
| 550 | 136 | 125 | 144.63 | | | 207.23 | |
| 600 | 107 | 90 | 104.30 | | | 165.38 | |
| 650 | 85 | 66 | 76.49 | | | 135.58 | |
| 665 | 79 | 60 | 69.48 | | | 128.01 | |
| 675 | 75 | 55.8 | 64.99 | 55.48 | | 122.80 | |
| **675** | | | | **43** | **43 (PCB)** | | **117 (PCB)** |
| 700 | 64 | 46 | 53.48 | 46 | | 110.61 | |
| 710 | 59.9 | 42.4 | 49.34 | 42.40 | | 106.10 | |
| **710** | | | | **43** | **43 (PCB)** | | **102 (PCB)** |
| 750 | 40 | 27 | 31.19 | 27 | | 87.30 | |
| 770 | 29.3 | 19.1 | 22.26 | 19.10 | | 77.84 | |
| **770** | | | | **12** | **12 (PCB)** | | **69 (PCB)** |
| 790 | 18 | 11 | 13.33 | 11 | | 68.25 | |
| 800 | 12 | 7.5 | 8.77 | 7.5 | | 64.03 | |
| 860 | 159 | 93 | 108.14 | 93 | | 145.59 | |
| 870 | 154 | 89 | 103.53 | 89 | | 140.98 | |

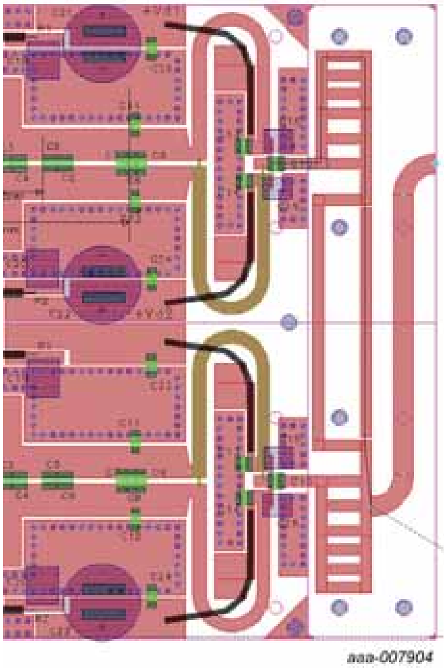
## 5.2 Design 1: 675 MHz/710 MHz

Doherty combiner design at 675 MHz and 710 MHz: the designs are similar, only differing in the 90° line.



Cumulative distance: 116.75 mm
Length 90° line = 74 mm
Length offset line = 43 mm
Length 35 Ω line = 60 mm
PCB Taconic; $\varepsilon_r$ = 3.5

**Fig 11. Doherty combiner design at 675 MHz**



Cumulative distance: 101.65 mm
Length 90° line = 59 mm
Length offset line = 43 mm
Length 35 Ω line = 60 mm
PCB Taconic; $\varepsilon_r$ = 3.5

**Fig 12. Doherty combiner design at 710 MHz**

### 5.3 Design 2: 770 MHz

Doherty combiner design at 770 MHz:

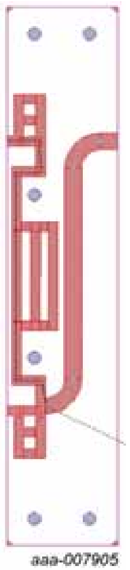


Fig 13. Doherty combiner design at 770 MHz

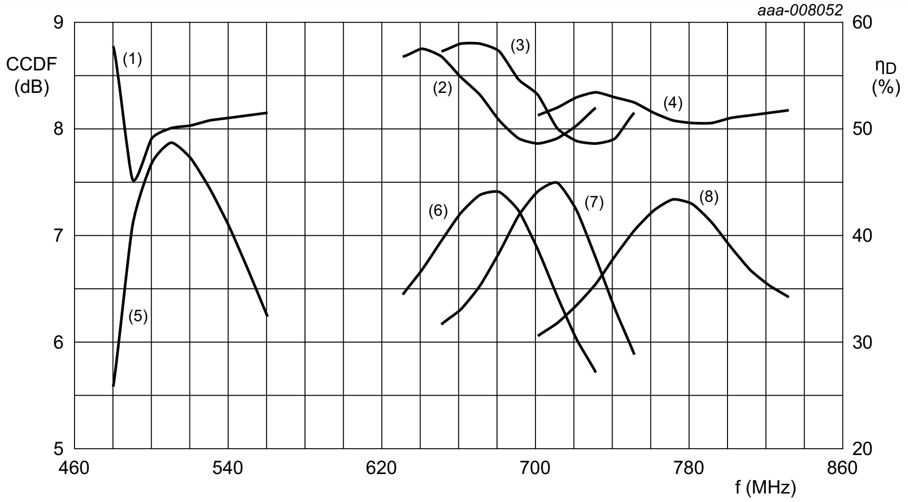
- Length 90° line = 57 mm
- Length offset line = 12 mm
- Length 35 Ω line = 50 mm
- PCB Taconic; $\varepsilon_r$ = 3.5

## 5.4 Design 3: 500 MHz

Doherty combiner design with coaxial cables. Due to length of the offset line, the PCB is too small.

- Length 90° line = 100 mm
- Length offset line = 200 mm
- Length 35 Ω line = 100 mm
- PCB Taconic; $\varepsilon_r$ = 2.03

## 5.5 DVB-T Measurements: $P_{avg}$ = 200 W, except 770 MHz $P_{avg}$ = 220 W



50 V; $I_{Dq}$ (main) = 1.2 A; $V_{GS}$ (peaking) = 0 V to 0.9 V

(1) CCDF 500 MHz design

(2) CCDF 675 MHz design

(3) CCDF 710 MHz design

(4) CCDF 770 MHz design

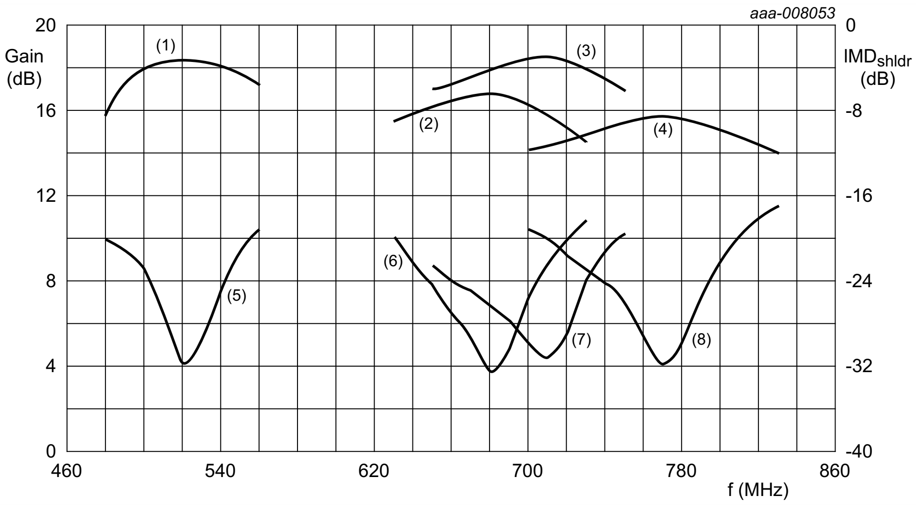
(5) $\eta_D$ 510 MHz design

(6) $\eta_D$ 680 MHz design

(7) $\eta_D$ 710 MHz design

(8) $\eta_D$ 770 MHz design

**Fig 14. Overview of four Doherty designs: CCDF and drain efficiency as functions of frequency**



50 V; $I_{Dq}$ (main) = 1.2 A; $V_{GS}$ (peaking) = 0 V to 0.9 V

(1) Gain 500 MHz design
(2) Gain 675 MHz design
(3) Gain 710 MHz design
(4) Gain 770 MHz design
(5) $IMD_{shldr}$ 500 MHz design
(6) $IMD_{shldr}$ 680 MHz design
(7) $IMD_{shldr}$ 710 MHz design
(8) $IMD_{shldr}$ 770 MHz design

**Fig 15. Overview of four Doherty designs: gain and shoulder distance (4.3 MHz from $f_c$) as functions of frequency**

### 5.5.1 Supplementary measurement conditions for Figure 14 and Figure 15

- 500 MHz: $V_{GS}$ peaking = 0.75 V; no parallel 50 Ω resistor at input of main amplifier
- 675 MHz: $V_{GS}$ peaking = 0.5 V; parallel 50 Ω resistor at input of main amplifier
- 710 MHz: $V_{GS}$ peaking = 0.9 V; no parallel 50 Ω resistor at input of main amplifier
- 770 MHz: $V_{GS}$ peaking = 0 V; parallel 50 Ω resistor at input of main amplifier.

## 5.6 Multiple bands

This Doherty design shows multiple bands, this was already seen in simulation.

Multiple bands can also be seen with small signal measurement see (Section 5.6.1).

Whether the multiple bands fall in the UHF band, depends on the total phase shift (output) of amplifier, offset line and 90° line. With 9.90° total phase shift, other bands can be used. In this application the phase shift (mid-band) of the amplifier block plus offset line is 4.90°. The impedance inverter will complete the total phase shift to 5.90°.

Note that in the present designs the multiple bands cannot be used (see Table 2).

- The input splitter has a constant phase shift which is not in line with the output impedance inverter. This will reduce peak power significantly for the other bands (in the target band the phase shift error is small enough not to cause peak power loss).
- $Z_{main}$ in back-off in the multiple bands will not be constant but will increase dependent on frequency. This will cause higher efficiency, giving a $\eta_D$ of 49.28042 % at 550 MHz (see Table 2). A too high $Z_{main}$ (in back-off) causes a problem with the peak (back-off) voltage because the maximum voltage swing cannot be achieved (knee voltage and/or breakdown limitation). This can result in lower efficiency and worse linearity. Note that this effect is dependent on the total phase shift in the amplifier (thus the increase of $Z_{main}$ is less with e.g. 9.90° than 5.90°, Section 5.6.1.

### 5.6.1 Simulation for ideal network

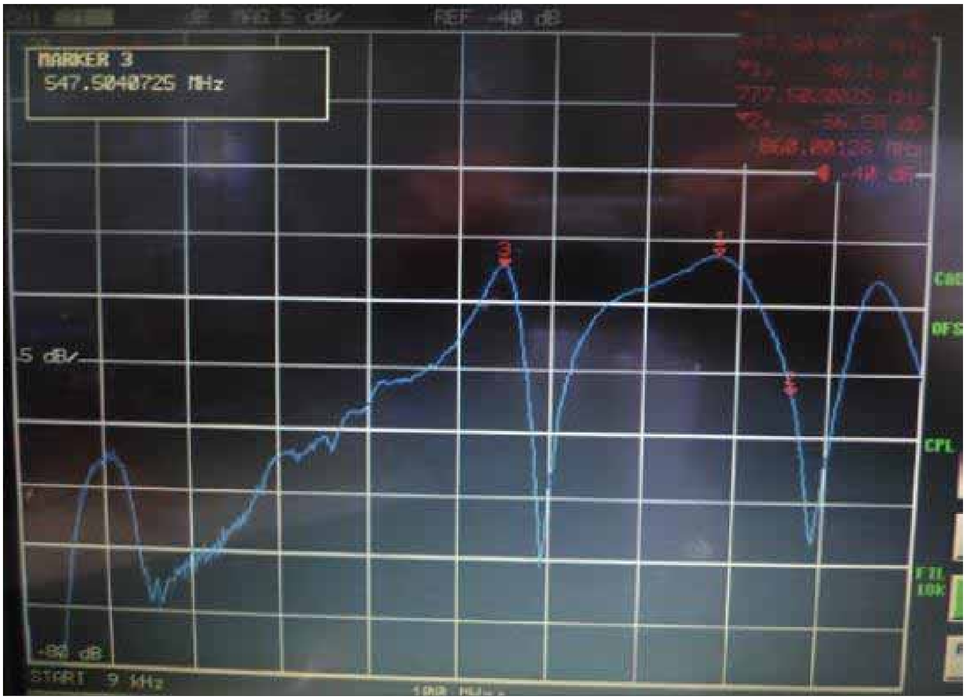


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Fig 16. Screenshot of network analyzer small signal display (Figure 17)

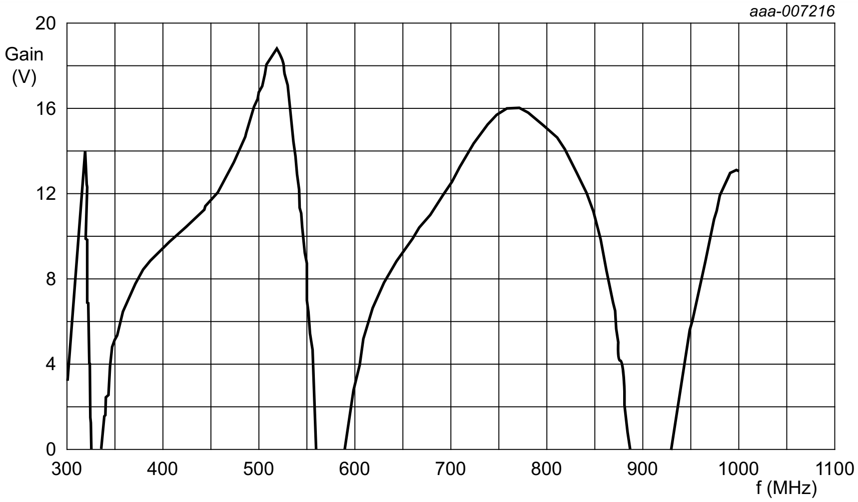
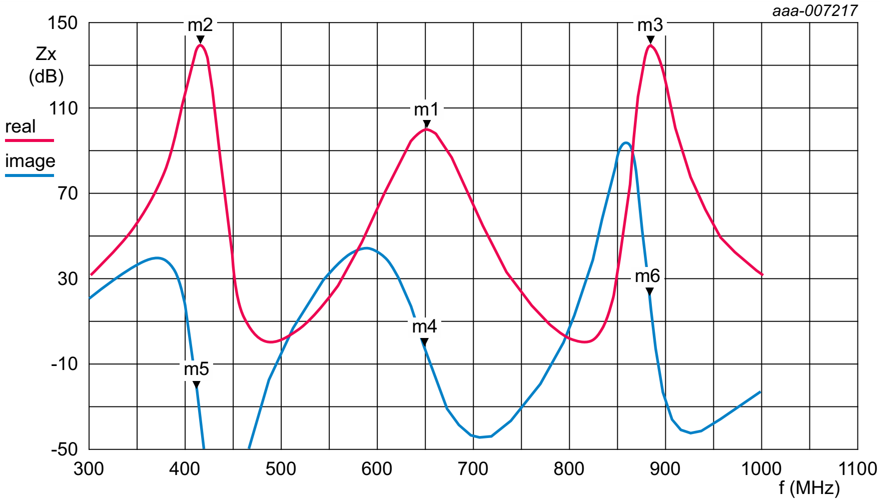


**Fig 17. Small signal simulation: gain as a function of frequency**

**Table 2. DVB-T measurement values: 770 MHz Doherty combiner; multiple band at approximately 550 MHz**

| f (MHz) | $V_{DS}$ (V) | $P_i$ (dB) | $P_L$ (W) | $G_p$ (dB) | Left $IMD_{shldr}$ (dBc) | Right $IMD_{shldr}$ (dBc) | $I_{D1}$ | $I_{D2}$ | $\eta_D$ (%) | P (W) | CCDF 0.1 % |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 570 | 49.35724 | –14.6456 | 198.1 | 15.17 | –19.6103 | –19.109 | 6.11164 | 4.72278 | 37.04486 | 336.6571 | 6.610577 |
| 560 | 49.44655 | –14.4517 | 198.3 | 15.47 | –21.3721 | –20.7245 | 5.16053 | 4.0945 | 43.33201 | 259.3293 | 6.442308 |
| **550** | **49.50541** | **–14.3658** | **198.6** | **15.66** | **–23.2219** | **–22.2718** | **4.58328** | **3.55724** | **49.28042** | **204.3998** | **6.274038** |
| 540 | 49.48266 | –13.1682 | 200.3 | 15.54 | –22.1288 | –21.1987 | 4.92998 | 3.5018 | 48.00745 | 216.9269 | 6.153846 |
| 530 | 49.37716 | –11.6353 | 198.7 | 14.94 | –22.5852 | –20.5922 | 6.03872 | 4.27817 | 39.00524 | 310.7187 | 6.298077 |



m2: f = 414 MHz

m1: f = 650 MHz

m3: f = 884 MHz

m5: f = 414 MHz

m4: f = 660 MHz

m6: f = 884 MHz

**Fig 18. Simulation (ideal network) $Z_m$ (back-off) with phase shift 5.90°; $Z_m$ ratio = 1.4**

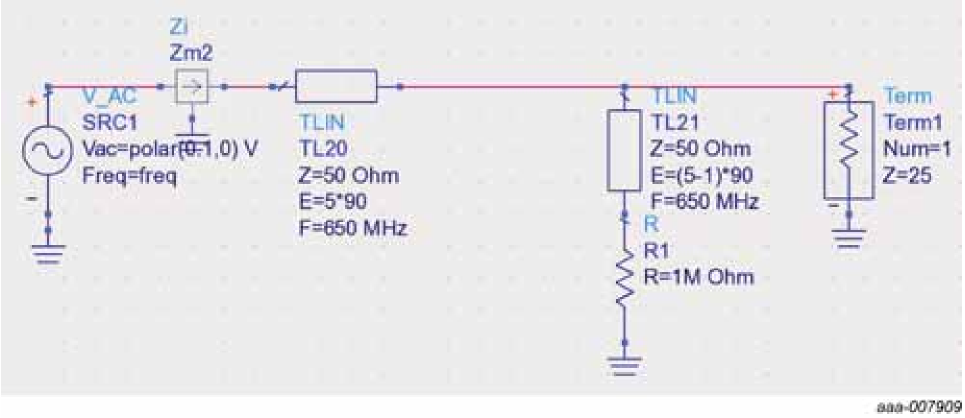
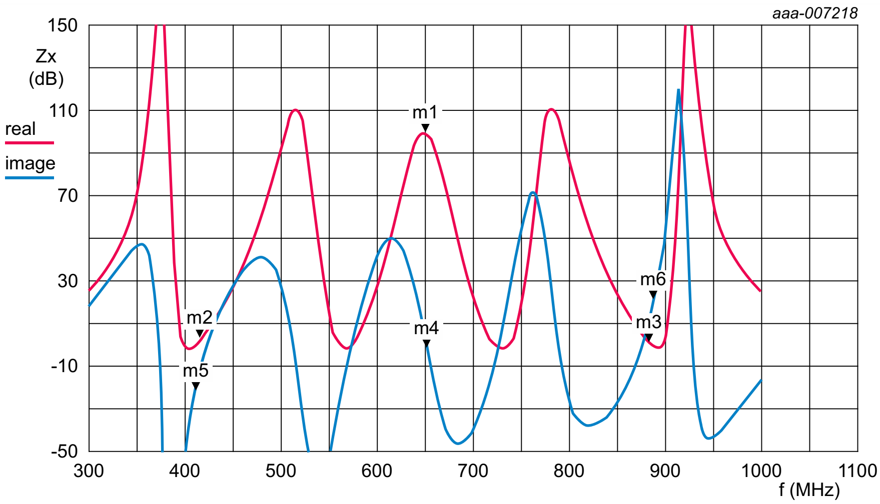


**Fig 19. Impedance model for Figure 18**



m2: f = 414 MHz

m1: f = 650 MHz

m3: f = 884 MHz

m5: f = 414 MHz

m4: f = 650 MHz

m6: f = 884 MHz

**Fig 20.** **Simulation (ideal network) $Z_m$ (back-off) with phase shift 9.90°; $Z_m$ ratio = 1.1 (nearest sub band)**

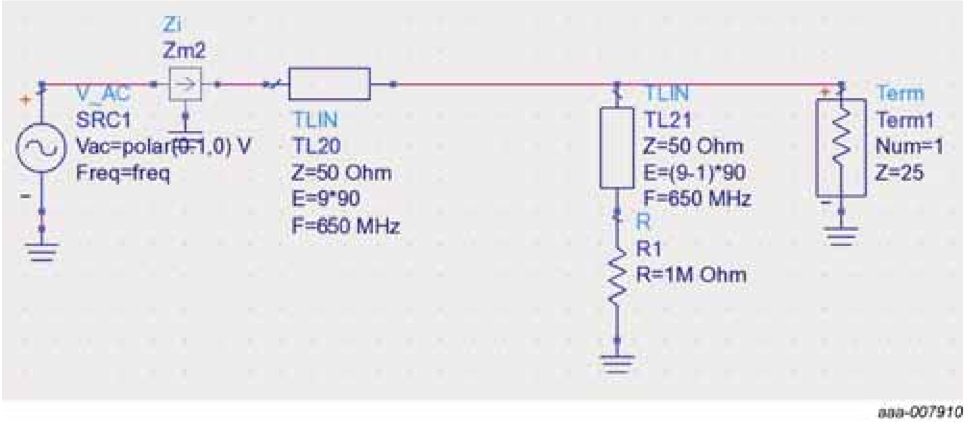


**Fig 21.** **Network model for Figure 20**

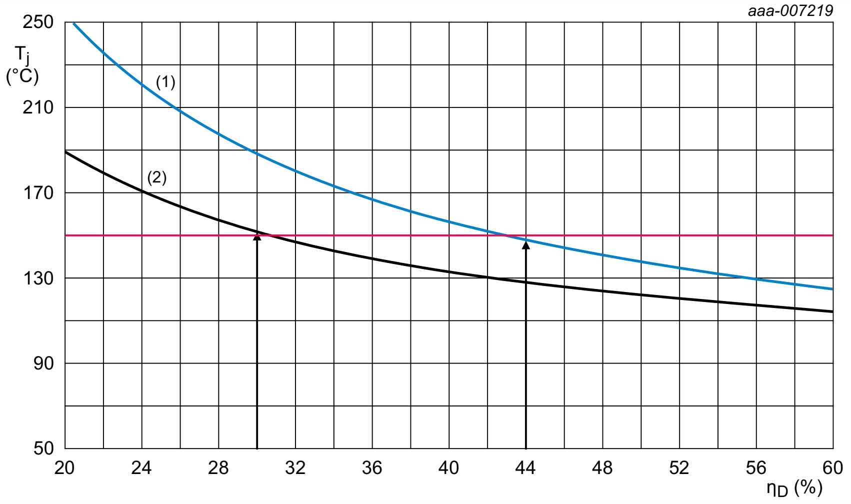
## 5.7 Thermal considerations

Figure 22 and Figure 23 show thermal properties for a Class AB push-pull amplifier and for a Doherty amplifier with two transistors - one for main, and one for peaking.

It can be seen that although the overall dissipation is less in a Doherty amplifier (40 % compared to e.g. 25 % to 30 %) the thermal stress on the main amplifier can be much greater.

Conditions for the calculation:

- $P_{L(AV)}$ = 120 W average; DVB-T, PAR 8 dB
- $R_{th(j\text{-}case)}$ = 0.15 K/W
- $T_{case}$ = 100°C
- Doherty: 85 % dissipation in Main amplifier
- Dissipation +25 % (non-ideal matching)
- Lifetime TTF 0.1 % (failure fraction: p = 0.001)

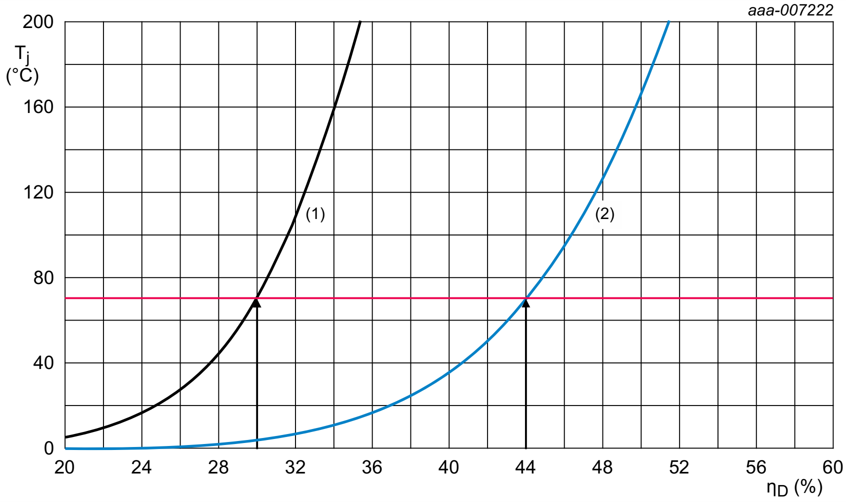


$T_{case}$ = 100 °C

(1) Main amplifier in Class AB

(2) Doherty peaking amplifier

**Fig 22. Junction temperature as a function of drain efficiency**



$T_{case}$ = 100 °C

(1) Main amplifier in Class AB

(2) Doherty peaking amplifier

**Fig 23. TTF 0.1 % as a function of drain efficiency ($\eta_D$)**

It can be seen in Figure 23 that for a junction temperature of 150 °C in class AB mode, 30 % efficiency is required. In a Doherty amplifier, the efficiency for the same junction temperature is minimum 44 %. The reason is that almost all dissipation (85 %) in Doherty is in the main amplifier in comparison with class AB where dissipation is spread over two transistors.

Note that in a Single Package Doherty (SPD) the thermal stress on the main amplifier improves significantly but this is not covered in this Application Note.

## 6. Doherty amplifier board

The test circuit (Figure 24 and Figure 25) has been designed on a Taconic RF35 PCB: h = 0.762 mm; $\varepsilon_r$ = 3.48.

Figure 26 shows the combiner designs.

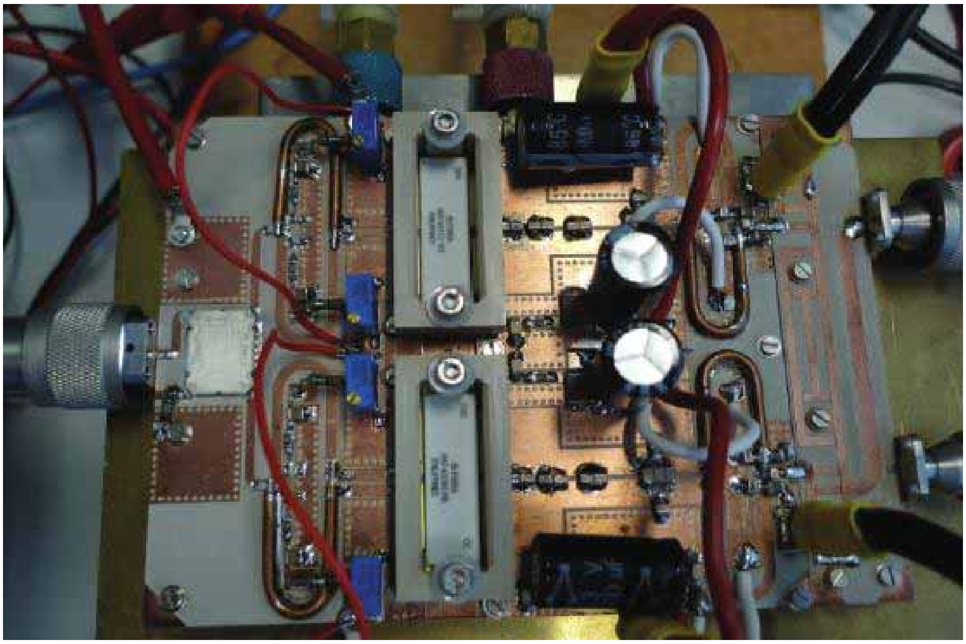


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Fig 24. Demo board for 710 MHz design RF testing

Table 3. Demo board characteristics and operating conditions

| Topic | Parameter | Conditions | Detail |
|---|---|---|---|
| Demo board | | output, input and Doherty combiner PCBs | Doh_BLF888A_pcb_V2.dxf |
| | | serial number | NA-1697, NA-xxxx |
| Supply voltage | | | 50 V |
| $I_{Dq}$ | quiescent drain current | main amplifier | 1.2 A |
| $V_{GS}$ | gate-source voltage | peaking amplifier; dependent on tested configuration and frequency | 0.9 V |
| **Test equipment** | | | |
| measurement | network analyzer | | Rohde & Schwarz ZVR |
| modeling | ADS | | Agilent Advanced Design System |
| **Test signals** | | | |
| DVB-T | | DVB-T signal with shoulder distance | 4.3 MHz from $f_c$ |
| Pulse | | 10 % pulsed CW | 100 μs |

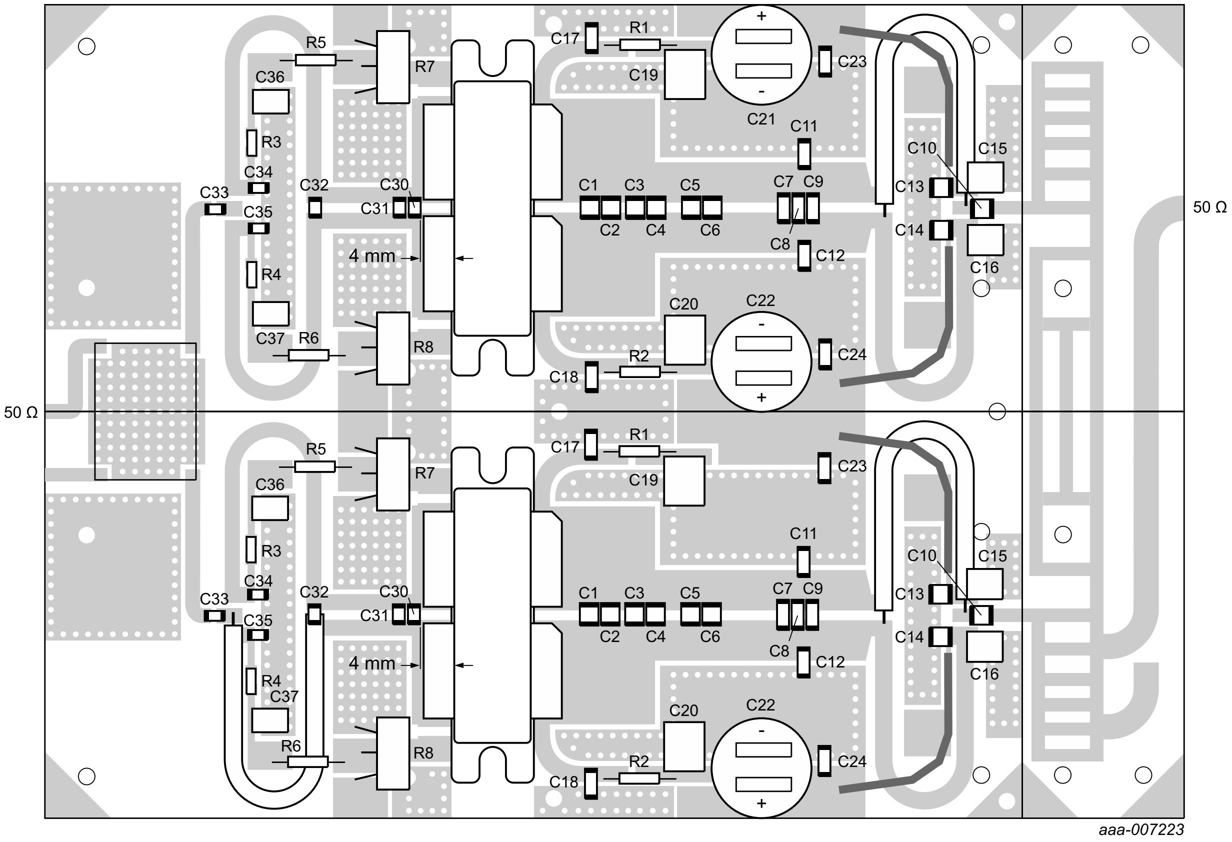

Fig 25. PCB layout: main and peaking amplifiers and combiner

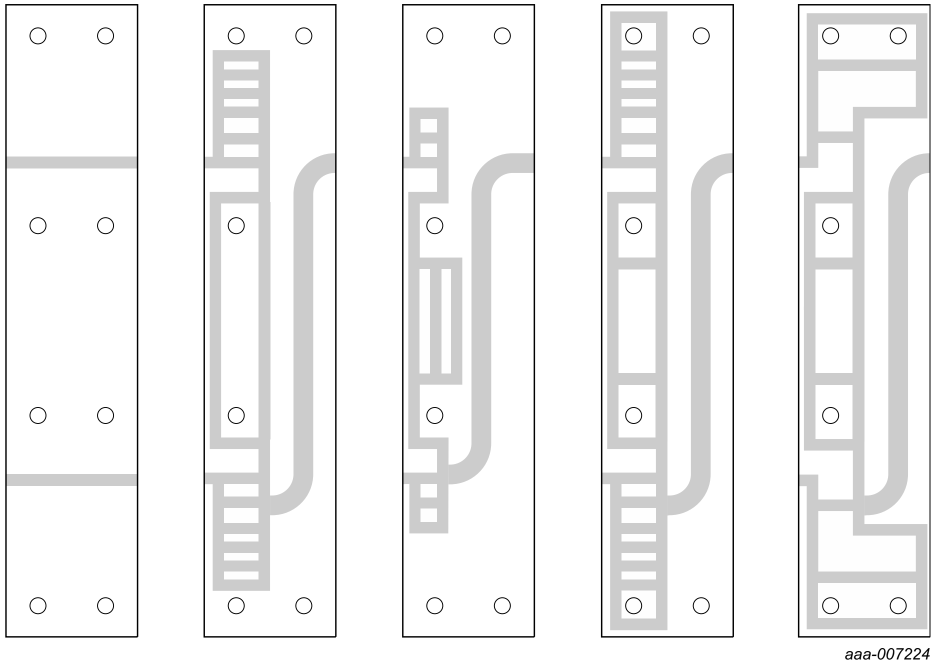

**Fig 26. Combiner designs**

**Table 4. List of components**

*For test circuit PCB layout see Figure 25*

| Component | Description | Value | Remarks |
|---|---|---|---|
| B1, B2 | semi-rigid coax cable | 25 Ω, 49.5 mm | UT-090C-25 (EZ 90-25 |
| C1 | multilayer ceramic chip capacitor | 12 pF | |
| C2, C3, C4, C5, C6 | multilayer ceramic chip capacitor | 8.2 pF | |
| C7 | multilayer ceramic chip capacitor | 6.8 pF | |
| C8 | multilayer ceramic chip capacitor | 2.7 pF | |
| C9 | multilayer ceramic chip capacitor | 2.2 pF | |
| C10, 13, C14 | multilayer ceramic chip capacitor | 100 pF | |
| C11, C12 | multilayer ceramic chip capacitor | 10 pF | |
| C15, C16 | multilayer ceramic chip capacitor | 4.7 µF, 50 V | KEMET C1210X475K5RAC-TU or capacitor of same quality |
| C17, C18, C23, C24 | multilayer ceramic chip capacitor | 100 pF | |
| C19, C20 | multilayer ceramic chip capacitor | 10 µF, 50 V | TDK C570X7R1H106KT00N or capacitor of same quality |
| C21, C22 | electrolytic capacitor | 470 µF, 63 V | |
| C30 | multilayer ceramic chip capacitor | 10 pF | |
| C31 | multilayer ceramic chip capacitor | 9.1 pF | |
| C32 | multilayer ceramic chip capacitor | 3.9 pF | |
| C33, C34, C35 | multilayer ceramic chip capacitor | 100 pF | |
| C36, C37 | multilayer ceramic chip capacitor | 4.7 µF, 50 V | TDK C4532X7R1E475MT020U or capacitor of same quality |
| L1 | microstrip | - | (W × L) 15 mm × 13 mm |

**Table 4. List of components** *...continued*
*For test circuit PCB layout see Figure 25*

| Component | Description | Value | Remarks |
|---|---|---|---|
| L2 | microstrip | - | (W × L) 5 mm × 26 mm |
| L3, L32 | microstrip | - | (W × L) 2 mm × 49.5 mm |
| L4 | microstrip | - | (W × L) 1.7 mm × 3.5 mm |
| L5 | microstrip | - | (W × L) 2 mm × 9.5 mm |
| L30 | microstrip | - | (W × L) 15 mm × 13 mm |
| L31 | microstrip | - | (W × L) 2 mm × 11 mm |
| L33 | microstrip | - | (W × L) 2 mm × 3 mm |
| R1, R2 | wire resistor | - | |
| R3, R4 | SMD resistor | - | 0805 |
| R5, R6 | wire resistor | - | |
| R7, R8 | potentiometer | - | |

[1] American technical ceramics type 800R or capacitor of same quality

[2] American technical ceramics type 800B or capacitor of same quality

[3] American technical ceramics type 180R or capacitor of same quality

[4] American technical ceramics type 100A or capacitor of same quality

[5] Printed-Circuit Board (PCB): Taconic RF35 $\varepsilon_r$ = 3.5 F/m; height = 0.762 mm; Cu (top bottom metallization); thickness copper plating = 35 $\mu$m.

# 7. Abbreviations

**Table 5. Abbreviations**

| Acronym | Description |
|---|---|
| ADS | Advanced Design System |
| CCDF | Complementary Cumulative Distribution Function |
| DVB-T | Digital Video Broadcast - Terrestrial |
| PCB | Printed-Circuit Board |
| TTF | Time-to-Failure |
| UHF | Ultra High Frequency |

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