

1.5 GHz Doherty power amplifier for base station applications using the BLF6G15L-250PBRN

Rev. 2 — 1 September 2015

Application note

Document information

Info	Content
Keywords	RF power transistor, Doherty architecture, LDMOS, Power amplifier, W-CDMA, LTE, Base station, BLF6G15L-250PBRN
Abstract	This application note describes the design and performance of a power amplifier for 1.5GHz 3GPP E-UTRA LTE base stations using two BLF6G15L-250PBRN LDMOS power transistors in Doherty architecture

Revision history

Rev	Date	Description
AN10923#2	20150901	Modifications <ul style="list-style-type: none">• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.• Legal texts have been adapted to the new company name where appropriate.
AN10923#1	20110314	Initial version

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1. Introduction

This application note describes the design and performance of a Doherty power amplifier optimized for use in 1.5 GHz 3GPP E-UTRA LTE base stations applications. The amplifier design, characteristics and the test methods used to determine the RF performance are also described.

The amplifier uses two BLF6G15L-250PBRN LDMOS power transistors in a Doherty architecture. The design ensures high efficiency while providing a peak power capability very similar to two parallel Class AB amplifiers. The input and output sections are internally matched, giving high gain with good gain flatness and phase linearity over a wide frequency band.

The BLF6G15L-250PBRN transistor is a sixth generation device using Ampleon's advanced LDMOS process.

2. Circuit description

The 1.5 GHz Doherty power amplifier employing two BLF6G15L-250PBRN power transistors is shown in the photograph of [Figure 1](#). The main amplifier is biased to operate in Class-AB mode and the peak amplifier is biased to operate in Class-C mode. The input signal is split by a 3 dB power divider and fed to each amplifier with a 90 degree phase difference. The amplified signals are recombined at the output with a power combiner. Both amplifiers operate when the input signal peaks, and each is presented with the load impedance that enables maximum output power. If the input signal amplitude drops below a preset threshold level, the Class-C peaking amplifier turns off and only the Class-AB remains active. At these lower power levels the Class-AB main amplifier is presented with higher load impedance that enables higher efficiency and gain. The result is an extremely efficient solution for amplifying the complex modulation schemes employed in current and emerging wireless systems.

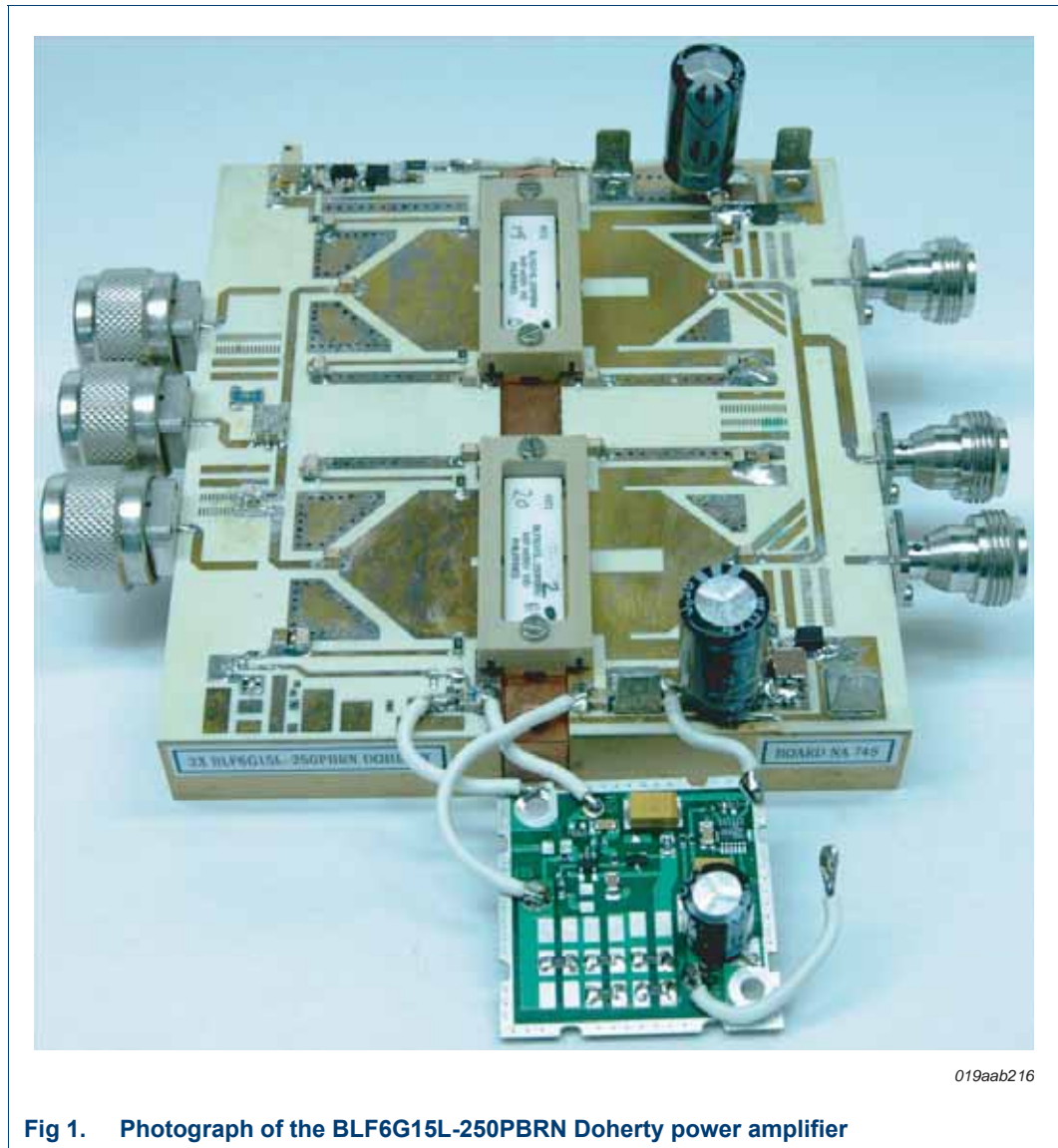


Fig 1. Photograph of the BLF6G15L-250PBRN Doherty power amplifier

3. Design and Tuning

The two-way symmetrical Doherty amplifier comprising a main amplifier and a peak amplifier, input phase splitter and power combiner was designed and optimized using the following target specification:

- Frequency band 1476 MHz to 1511 MHz
- 2-carrier W-CDMA 3 GPP, 64 DPCH, PAR = 7.5 dB at 0.01% probability per carrier, 5 MHz carrier spacing
- Drain-source voltage (V_{DS}) = 32 V
- $P_{L(3db)}$ = 58 dBm
- $P_{L(AV)}$ = 49 dBm
- Linear gain = 15 dB

- Gain ripple 0.5 dB
- RL_{in} 15 dB
- ACPR at 5 MHz offset and $P_{L(AV)} = -30$ dBc
- Efficiency at $P_{L(AV)} = 36$ %
- PCB material RO4350 30 mils

The description of the design of the single stage (Class-AB) amplifier is given in [Section 3.1](#), and the description of the Doherty design is given in [Section 3.2](#).

3.1 Design of the single stage amplifiers

The design began with calculation of the input and output requirements of a single stage amplifier working in Class-AB matched to 50Ω (main amplifier). [Table 1](#) gives the typical source and load impedances used in the matching circuit of the single stage amplifier.

The peak amplifier uses the same input and output matching design as the main amplifier. The only difference between the two amplifiers is in the bias conditions. The main amplifier is biased in Class-AB with I_{DQ} current of 1450 mA while the peak amplifier is biased in Class-C with V_{GS} of 0.4V.

Table 1. Typical impedance per section

Frequency (GHz)	$Z_S (\Omega)$	$Z_L (\Omega)$
1.48	$1.12 - j2.80$	$1.67 - j3.33$
1.51	$1.32 - j2.79$	$1.59 - j3.73$

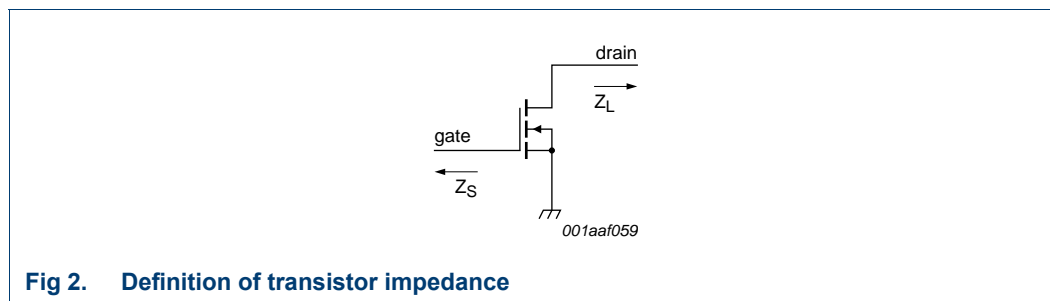


Fig 2. Definition of transistor impedance

3.2 Doherty design

For Doherty operation, the output-matching network of the main amplifier should also have the property of an impedance inverter. In order to achieve this a 50Ω stripline is added to the output matching circuit.

The peak amplifier in inactive mode has finite off-state impedance and will therefore absorb power from the main amplifier. This loss is minimized by inserting a 50Ω stripline whose length is chosen for the maximum impedance at the combining point of the power combiner when the peak amplifier is in off-state.

In order to get maximum output power from the Doherty amplifier it is necessary to provide the correct input drive level and phase to the peak and main amplifiers. Because the main and the peak amplifiers have similar gains, a symmetrical 3 dB, 90 degrees phase difference hybrid coupler is used to split the signal at the input.

It is essential that the signals from the main and peak amplifiers arrive in phase at the combining point of the power combiner. The phase difference introduced by the length of impedance inverter stripline and the off-state maximum impedance stripline therefore needs to be compensated for at the input. The phase difference caused by the different classes of operation is very small and can be ignored.

The drain bias line is one of the strongest contributors to the memory effects by the amplifiers. Making the bias line as short as possible will have a positive effect on the memory performance. In order to further reduce the drain video impedance, two parallel bias lines are placed symmetrically on both sides of every transistor.

3.3 Tuning

Adjusting the bias of the peak amplifier can further optimize the back-off efficiency of the Doherty amplifier, however this will be at the cost of linearity. Another way to optimize linearity is by adjusting the input phase shift while monitoring the AM-AM and AM-PM characteristics. This however will be at the cost of peak power and peak efficiency.

3.4 Transistor biasing

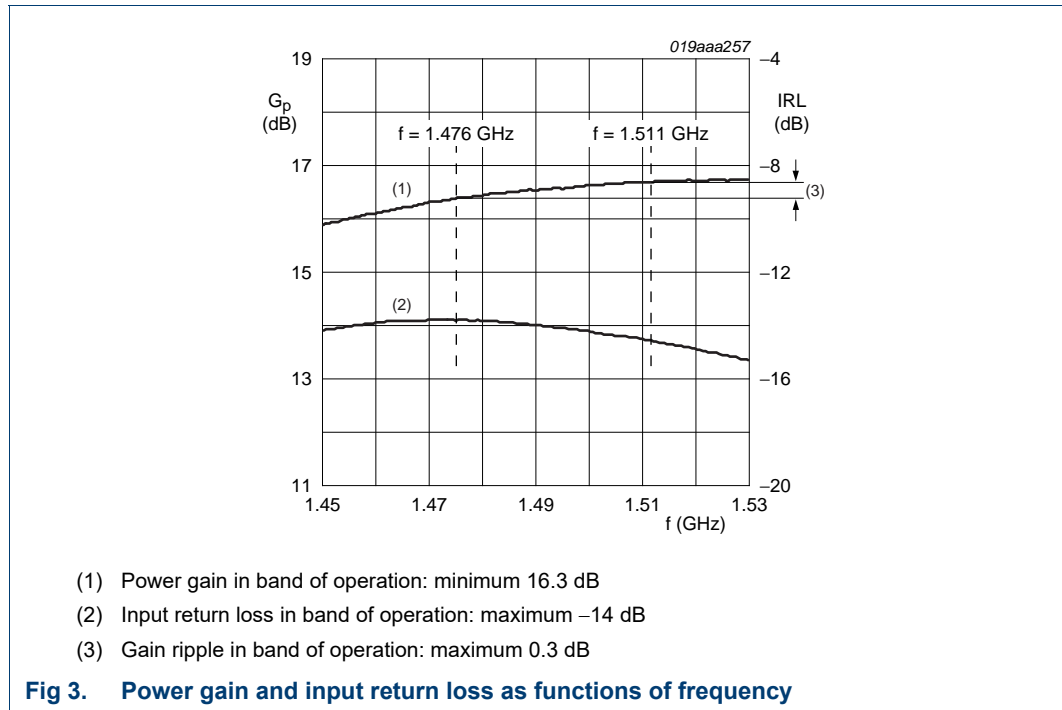
There are two ways to bias the BLF6G15-250PBRN transistor. The first is standard bias without using the sense FETs integrated in the package. In this case the sense FET leads can be removed and the bias can be applied directly to the power transistor(s) (see [Section 5 “Appendix A: PCB layout and bill of materials \(no auto bias\)”](#)). The second way of biasing is by using the sense leads. An auto bias circuit is required to provide a fixed I_{Dq} to the main RF FET. The FET is biased by a sense transistor mounted in the same package which is used as a current mirror. Details of the circuit and layout are given in [Section 6 “Appendix B: PCB layout and bill of materials with auto bias”](#), [Figure 12](#) and [Figure 13](#). The peak amplifier operates in Class-C and has a fixed gate-source voltage of 0.4 V.

4. Test results

4.1 Network analyzer frequency sweep

The network analyzer frequency sweep measurement results for the Doherty test board are shown in [Figure 3](#). The test conditions were as follows:

- $P_L = 49$ dBm
- $V_{DS} = 32$ V
- I_{Dq} (main) = 1450 mA
- $V_{GS} = 0.4$ V (peak amplifier)

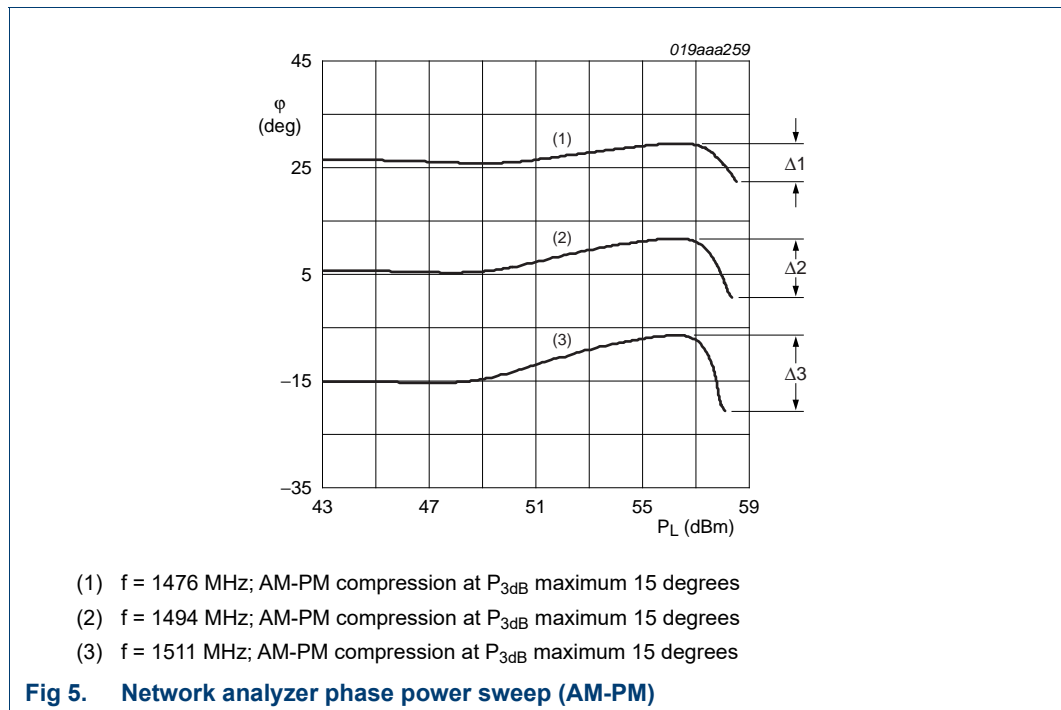
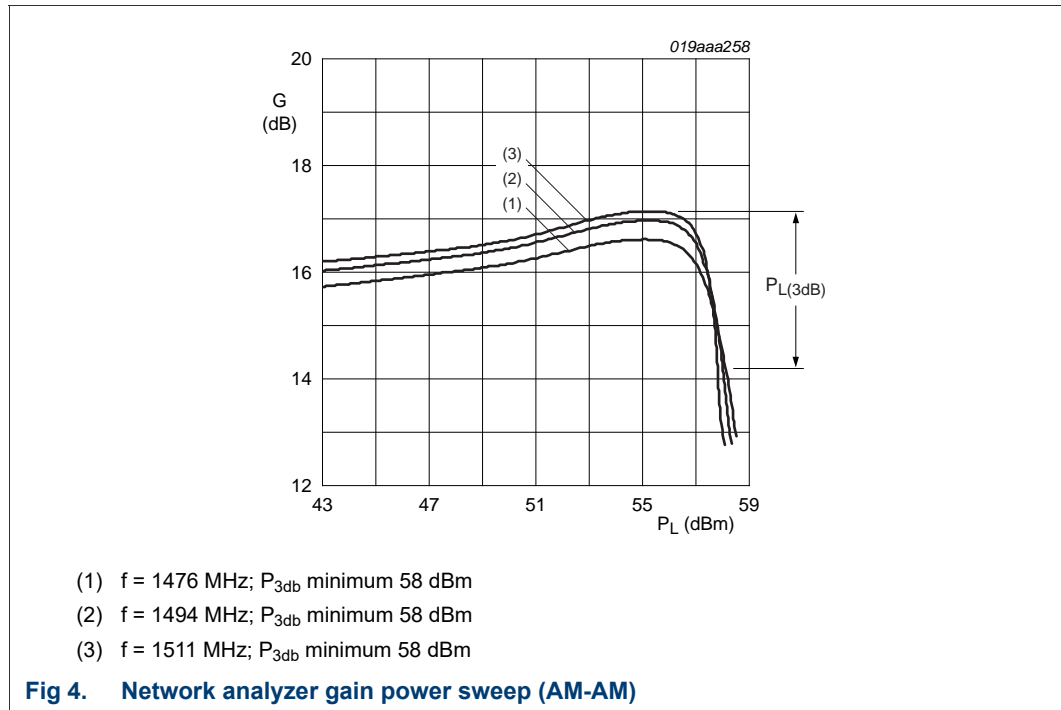


4.2 Large signal power sweeps

4.2.1 CW network analyzer power sweep (AM-AM and AM-PM)

The network analyzer measurement results for the test board are shown in [Figure 4](#) and [Figure 5](#). The test conditions were as follows:

- $V_{DS} = 32\text{ V}$
- $I_{Dq}(\text{main}) = 1450\text{ mA}$
- $V_{GS} = 0.4\text{ V}$ (peak amplifier)
- Network analyzer sweep time = 27.1 ms



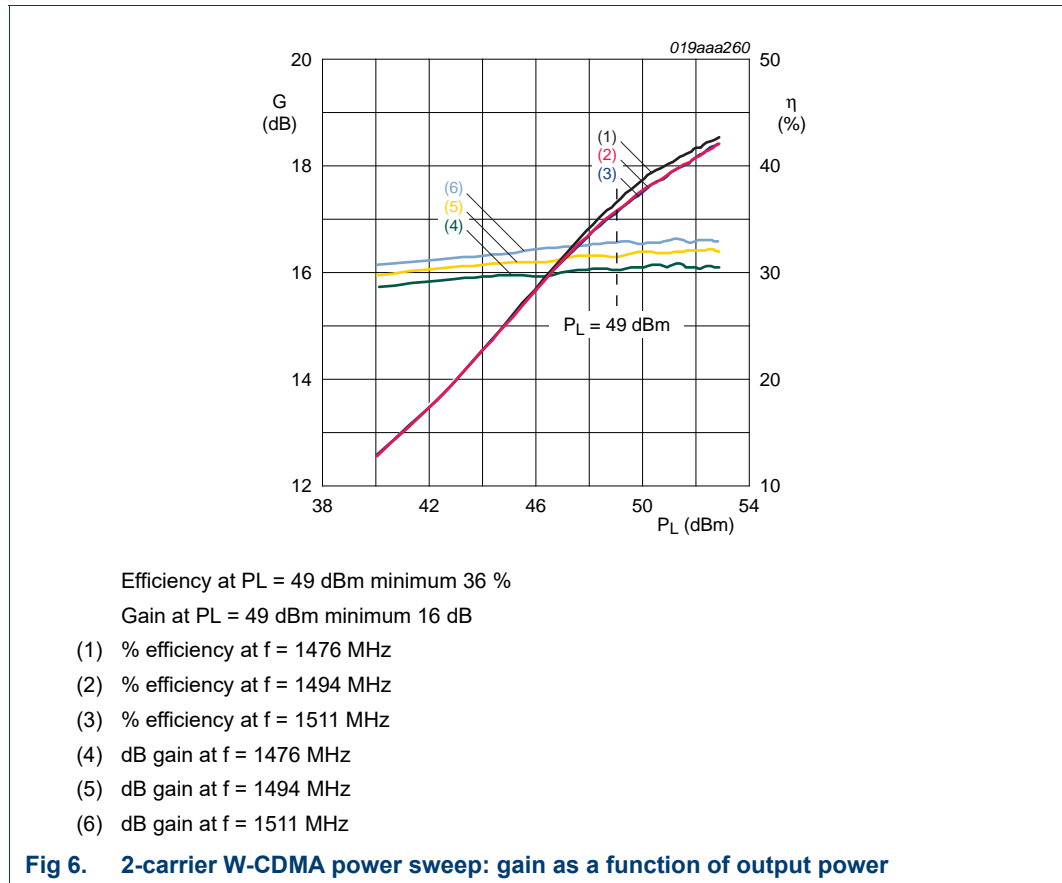
4.2.2 2-tone W-CDMA

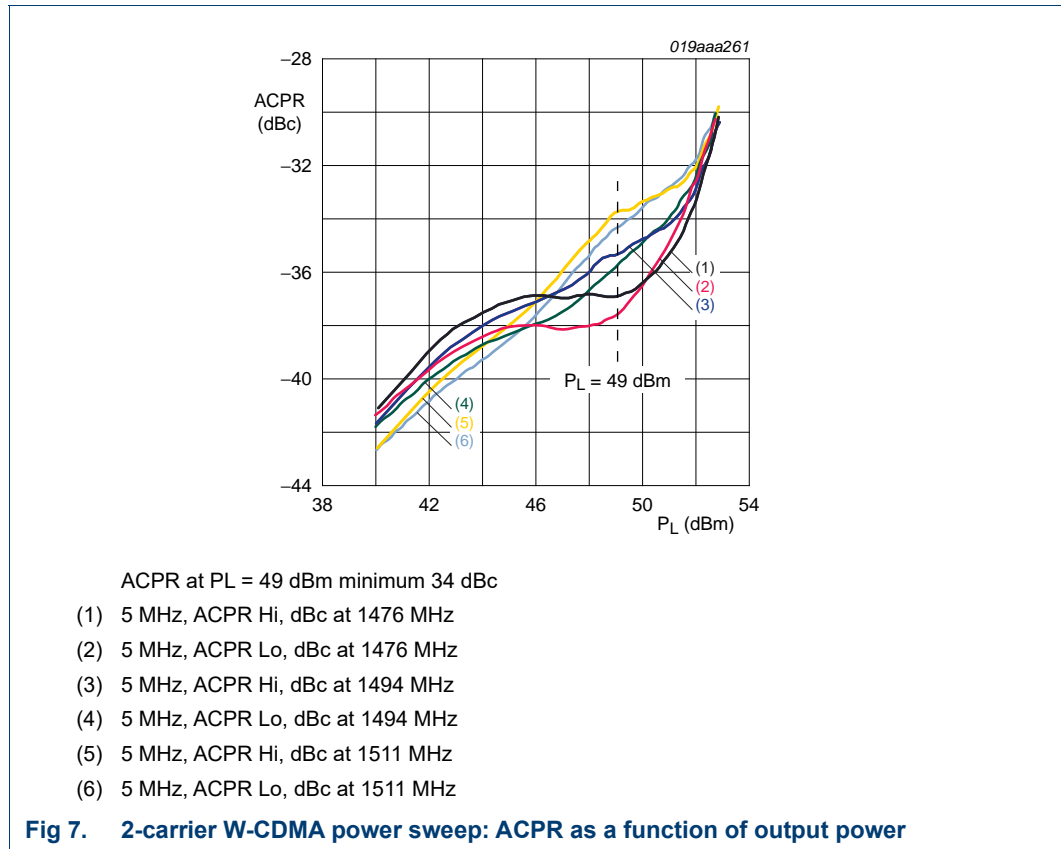
The 2-carrier W-CDMA (5 MHz spacing) measurement results for the test board are shown in [Figure 6](#) and [Figure 7](#). The test conditions were as follows:

- $V_{DS} = 32$ V
- I_{Dq} (main) = 1450 mA

1.5 GHz Doherty power amplifier using the BLF6G15L-250PBRN

- $V_{GS} = 0.4$ V (peak amplifier)
- 3 GPP, Test Model 1, 64 DPCH, PAR = 7.5 dB at 0.01% probability per carrier, 5 MHz carrier spacing

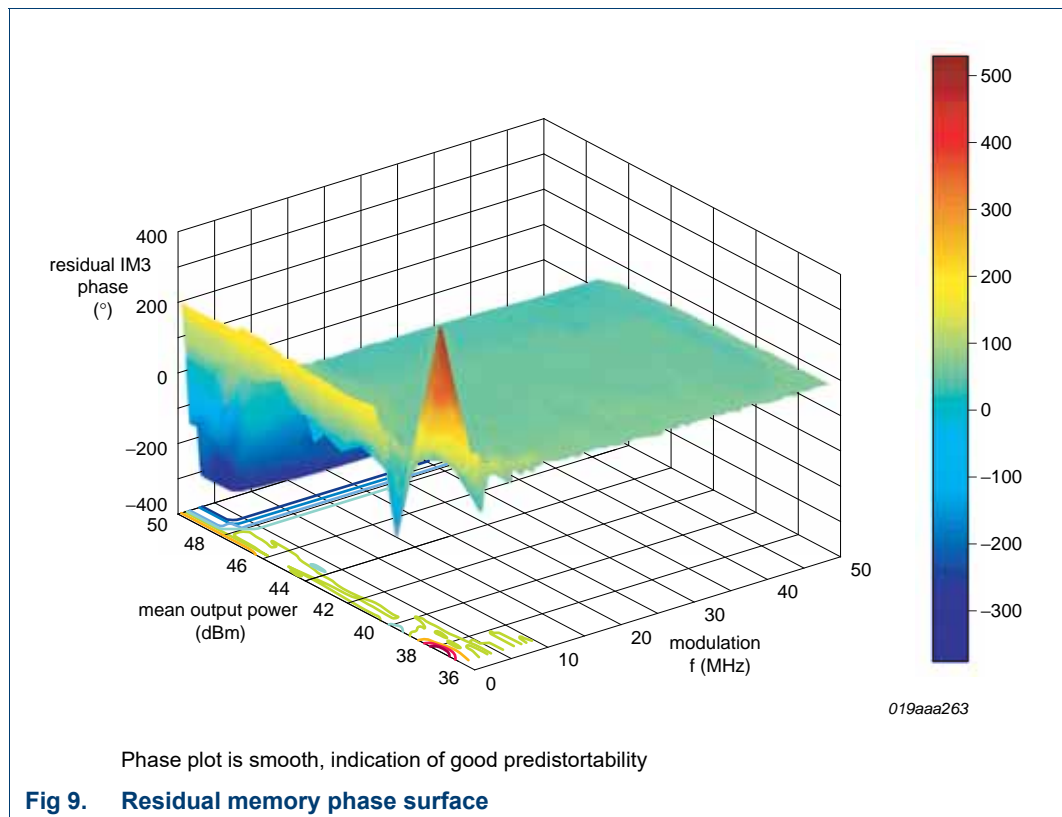
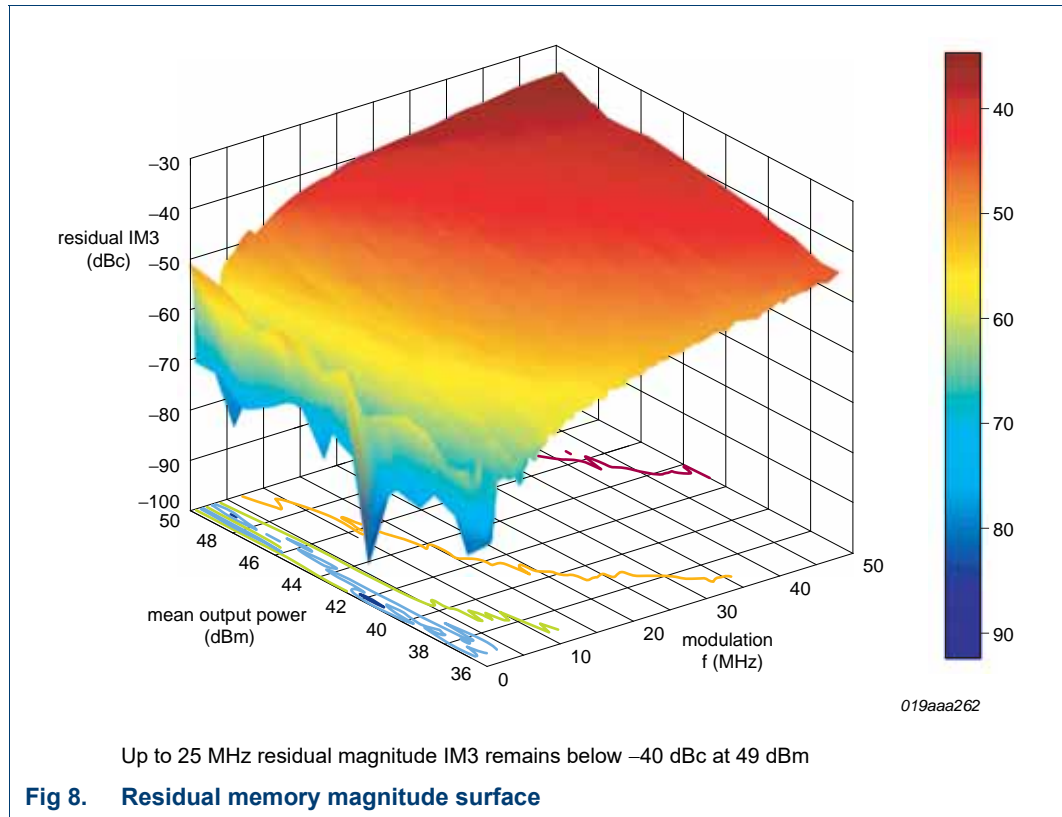




4.3 Residual memory magnitude and phase surface plots large signal power sweeps

The residual memory surface versus tone spacing and mean output power measurement results for the test board are shown in [Figure 8](#), and [Figure 9](#). The test conditions were as follows:

- $V_{DS} = 32 \text{ V}$
- $I_{Dq} \text{ (main)} = 1450 \text{ mA}$
- $V_{GS} = 0.4 \text{ V}$ (peak amplifier)



5. Appendix A: PCB layout and bill of materials (no auto bias)

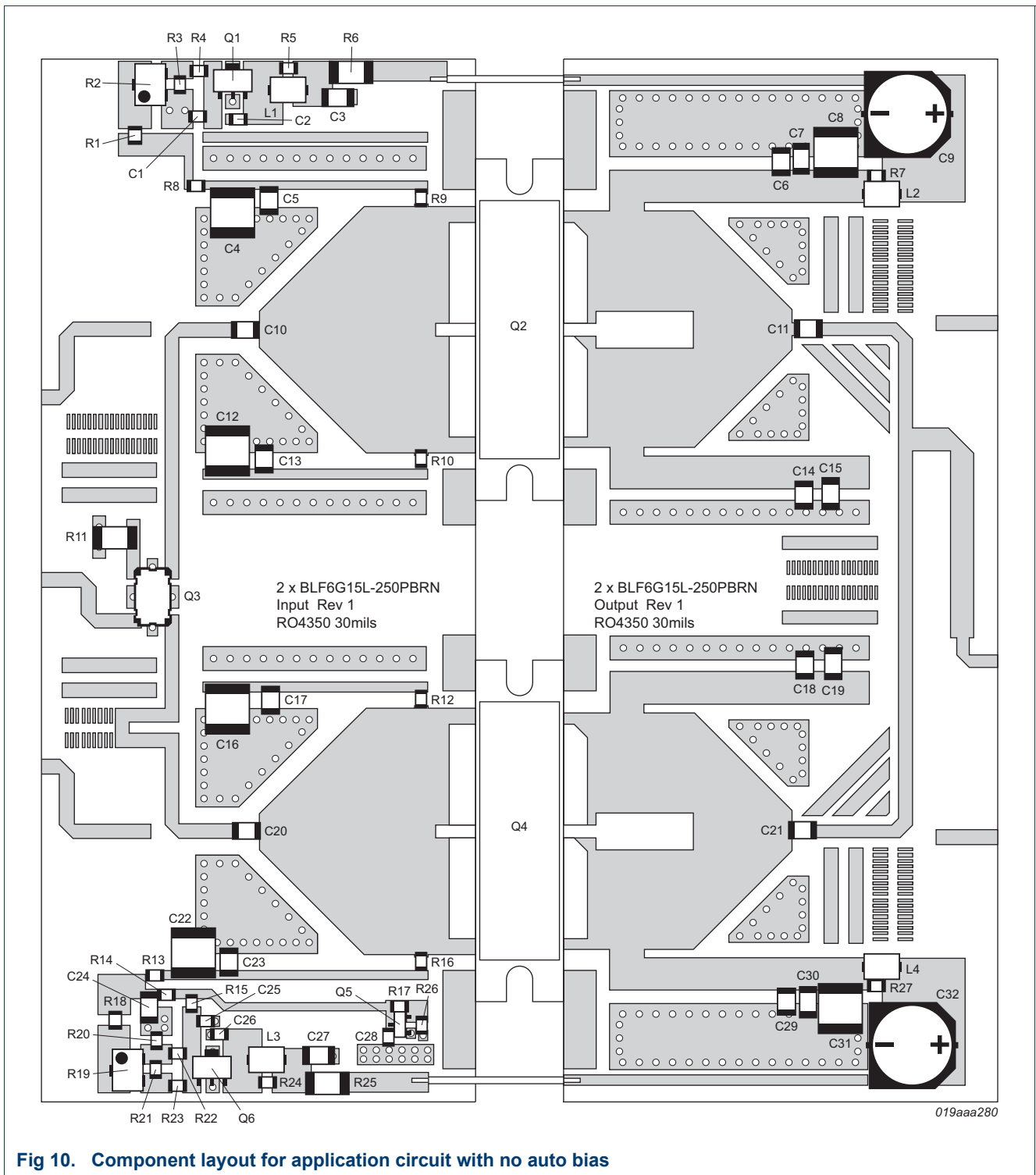


Fig 10. Component layout for application circuit with no auto bias

Table 2. Parts list for application circuit (no auto bias)

Component	Value	Description	Manufacturer
C1, C2, C25, C26	100 nF	capacitor	Murata GRM21BR71H104KA01L
C3, C24, C27, C28	1 μ F	capacitor	Murata GRM31MR71H105KA88L
C4, C8, C12, C16, C22, C31	10 μ F; 50 V	capacitor	Murata GRM32ER71H106KA12L
C5, C6, C10, C11, C13, C14, C17, C18, C20, C21, C23, C29	27 pF	capacitor, ATC 100B	American Technical Ceramics
C7, C15, C19, C30	470 nF; 50 V	ceramic capacitor	
C9, C32	470 μ F; 63 V	electrolytic capacitor	
Q1, Q6	Regulator	JRC 78L08	
Q5	NPN transistor	PMBT2222	NXP Semiconductors
Q3	15 mm \times 13 mm	3 dB hybrid XC1400P-03S	Anaren
Q2, Q4	LDMOS	BLF6G15L-250PBRN	Ampleon
L1, L2, L3, L4	26 mm \times 5 mm	inductor	
R1, R18	2 k Ω , 1%	resistor, 0805	
R2, R19	200 Ω	potentiometer	
R20	75 Ω , 1%	resistor, 0805	
R3, R4, R21, R23	430 Ω , 1%	resistor, 0805	
R15, R22	1.1 k Ω , 1%	resistor, 0805	
R14	11 k Ω , 1%	resistor, 0805	
R13	820 Ω , 1%	resistor, 0805	
R8	5.1 Ω , 1%	resistor, 0805	
R9, R10, R12, R16	10 Ω , 1%	resistor, 0805	
R5, R7, R24, R27	9.1 Ω , 1%	resistor, 0805	
R6, R25	499 Ω , 0.5W, 5%	resistor, 2010	
R17	5.1 k Ω	resistor, 0805	
R26	910 Ω	resistor, 0805	
R11	50 Ω	50 Ω load	

6. Appendix B: PCB layout and bill of materials with auto bias

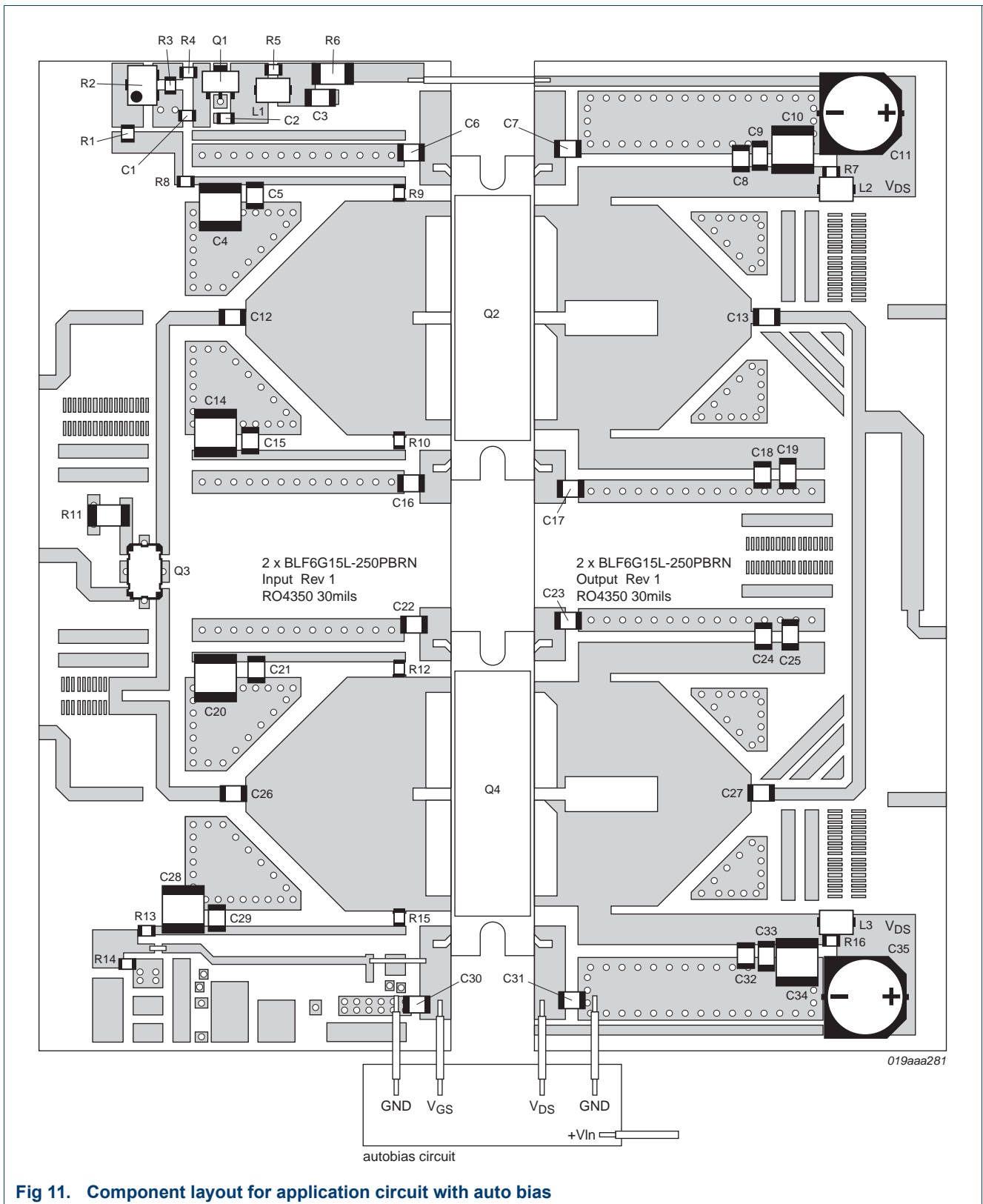
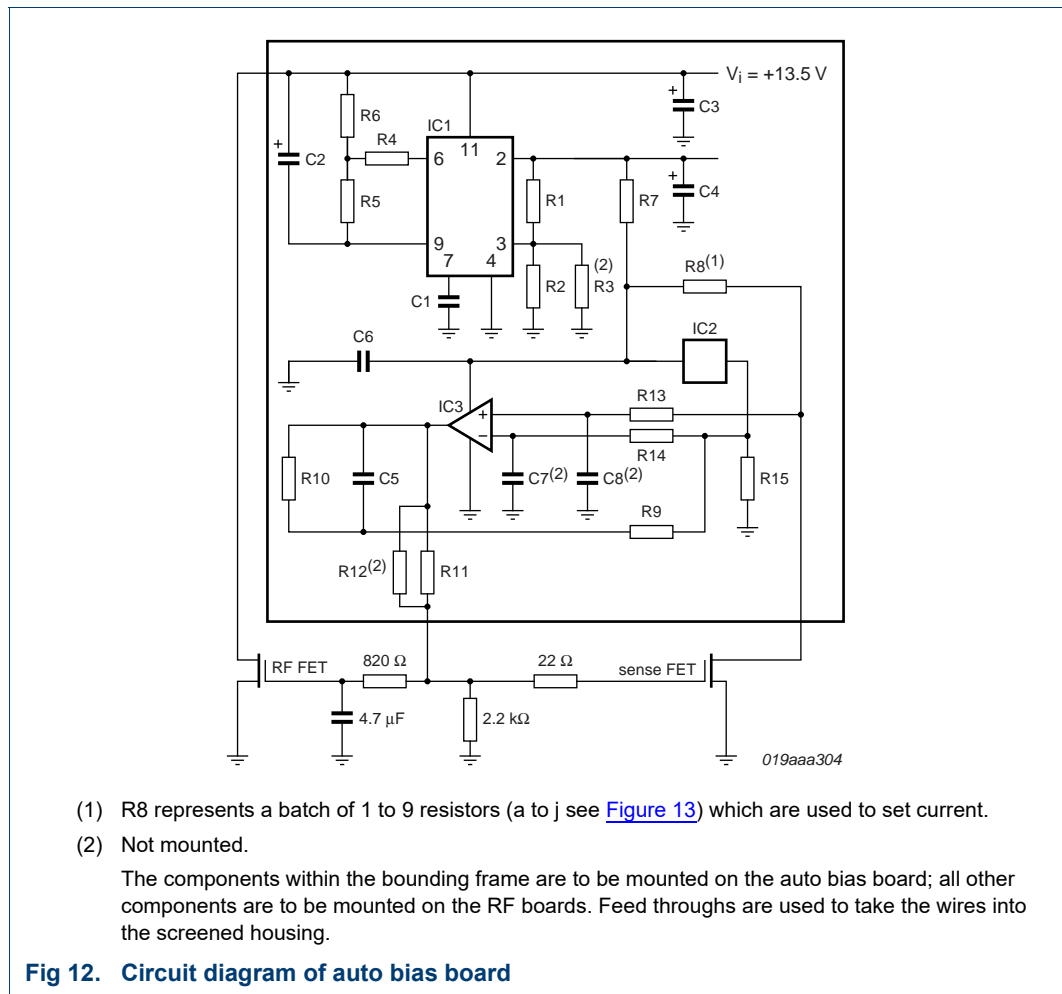


Fig 11. Component layout for application circuit with auto bias

Table 3. Parts list for application circuit (auto bias)

Component	Value	Description	Manufacturer
C1, C2	100 nF	capacitor	Murata GRM21BR71H104KA01L
C3	1 μ F	capacitor	Murata GRM31MR71H105KA88L
C4, C10, C14, C20, C28, C34	10 μ F	capacitor	Murata GRM32ER71H106KA12L
C5, C6, C7, C8, C12, C13, C15, C16, C17, C18, C21, C22, C23, C24, C26, C27, C29, C30, C31, C32	27 pF	capacitor	
C9, C19, C25, C33	470 nF; 50 V	ceramic capacitor	
C11, C35	470 μ F; 63 V	electrolytic capacitor	
Q1	regulator	JRC 78L08	
Q2, Q4	LDMOS	BLF6G15-250PBRN	Ampleon
Q3	15 mm \times 13 mm	3 dB hybrid XC1400P-03S	Anaren
L1, L2, L3	26 mm \times 5 mm	inductor	
R1, R14	2 k Ω , 1%	resistor, 0805	
R2	200 Ω	potentiometer	Bourns
R3, R4	430 Ω , 1%	resistor, 0805	
R5, R7, R16	9.1 Ω	resistor, 0805	
R6	499 Ω , 0.5 W, 5%	resistor, 2010	
R8	5.1 Ω , 1%	resistor, 0805	
R9, R10, R12, R15	10 Ω , 1%	resistor, 0805	
R11	50 Ω	50 Ω load	
R13	820 Ω , 1%	resistor, 0805	

7. Appendix C: Component layout auto bias board



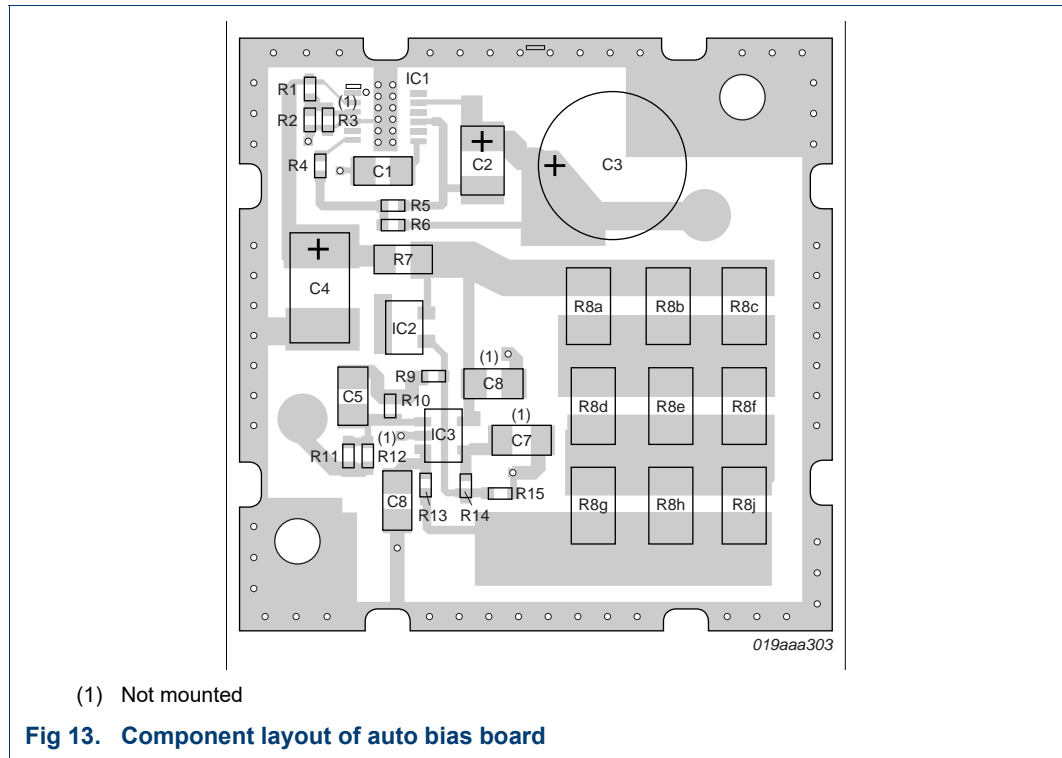


Table 4. Parts list for auto bias board

Component	Value	Description	Manufacturer
C1	1 nF	ceramic capacitor	
C2	2.2 μF	electrolytic capacitor	
C3	100 μF	electrolytic capacitor	
C4	10 μF	electrolytic capacitor	
C5	2.2 nF	ceramic capacitor	
C6	100 nF	ceramic capacitor	
IC1	-	LT3011	Linear Technology
IC2	-	LM4051	National Semiconductor
IC3	-	LM7341	National Semiconductor
R1, R6	1 MΩ	resistor, 0603	
R2, R3 ^[1]	100 kΩ	resistor, 0603	
R4	4.7 kΩ	resistor, 0603	
R5	47 kΩ	resistor, 0603	
R7	4.7 Ω	resistor, 1206	
R8	57 Ω	up to 9 off; resistor, 0603	
R9	2.7 kΩ	resistor, 0603	
R10	56 kΩ	resistor, 0603	
R11, R12 ^[1]	6.8 kΩ	resistor, 0603	
R13, R14, R15	10 kΩ	resistor, 0603	

[1] Not mounted

8. Abbreviations

Table 5. Abbreviations

Acronym	Description
ACPR	Adjacent Channel Power Ratio
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communication
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
UMTS	Universal Mobile Telecommunications System
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

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Date of release: 1 September 2015
 Document identifier: AN10923#2