AN10885

Doherty RF performance analysis using the BLF7G22LS-130

Rev. 3 — 1 September 2015

Application note

AMPLEON

Document information

Info	Content
Keywords	RF power transistors, Doherty architecture, LDMOS, power amplifier, RF performance, Digital PreDistortion (DPD), UMTS, W-CDMA, BLF7G22LS-130
Abstract	This application note describes a state-of-the-art power amplifier design for UMTS base stations using the BLF7G22LS-130 LDMOS transistor

Revision history

Rev	Date	Description
AN10885#3	20150901	Modifications • The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.
AN10885#2	20100225	Application note
AN10885#1	20100106	Initial version

Contact information

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1. Introduction

This application note describes a state-of-the-art power amplifier design for UMTS base stations using the BLF7G22LS-130 LDMOS power transistor. The amplifier design characteristics and the test methods used to determine the RF performance are also described.

The amplifier uses two BLF7G22LS-130 devices in a Doherty architecture on a Rogers 3006 PCB having a thickness of 0.64 mm (0.025"). The design ensures high-efficiency while maintaining a very similar peak power capability of two transistors combined. The input and output sections are internally matched, benefiting the amplifier design with high gain and good gain flatness and phase linearity over a wide frequency band.

The BLF7G22LS-130 is a seventh generation LDMOS device using Ampleon's advanced LDMOS process.

2. Test summary

The amplifier was characterized under the following conditions:

- Network analyzer measurements for power gain (G_p), delay (t_d) and Input Return Loss (IRL) at:
  - output power (P_L) = 47 dBm
  - drain-source voltage (V_{DS}) = 28 V
  - main power amplifier quiescent drain current (I_{Dq}) = 900 mA
  - gate-source voltage of peak amplifier ($V_{GS (peak)}$) = 0.5 V
- CDMA Interim Standard (IS-95) at V_{DS} = 28 V, I_{Dq} = 900 mA and V_{GS} = 0.5 V
- 2-carrier W-CDMA (15 MHz spacing), V_{DS} = 28 V, I_{Dq} = 900 mA and $V_{GS (peak)}$ = 0.5 V
- Peak output power (P3dB) capability using CDMA IS95 signal, ratio of peak power to average power = 9.7 dB at 0.01 % probability, V_{DS} = 28 V, I_{Dq} = 900 mA and $V_{GS (peak)}$ = 0.5 V
- Output power 3 dB compression point using pulsed signal, width = 12 µs, 10 % duty cycle at V_{DS} = 28 V, I_{Dq} = 900 mA and $V_{GS (peak)}$ = 0.5 V
- Digital PreDistortion (DPD) measurements using a DPD system, 2-carrier W-CDMA signal, Peak-to-average ratio (PAR) = 7.5 dB at 0.01 % probability (total signal), V_{DS} = 28 V, I_{Dq} = 900 mA, $V_{GS (peak)}$ = 0.5 V

Table 1. Performance summary

Frequency (GHz)	G_p at 47 dBm (dB)	IRL at 47 dBm (dB)	P3dB pulsed 12 µs pulse width (dBm)	IMD3 (no correction) at 47 dBm (dB)	IMD3 with DPD at 47 dBm (dB)	Drain efficiency (η_D) at 47 dBm (%)
2.11	17.2	−14.0	54.4	−31.3/−30.9	−60.2/−59.6	44.2
2.14	17.3	−15.5	54.4	−33.4/−33.0	−59.8/−58.4	42.9
2.17	17.2	−17.0	54.4	−33.8/−34.7	−59.4/−57.9	42.2

3. RF performance

3.1 Network analyzer measurements

Network analyzer measurements were performed under the following conditions:

- P_L = 47 dBm
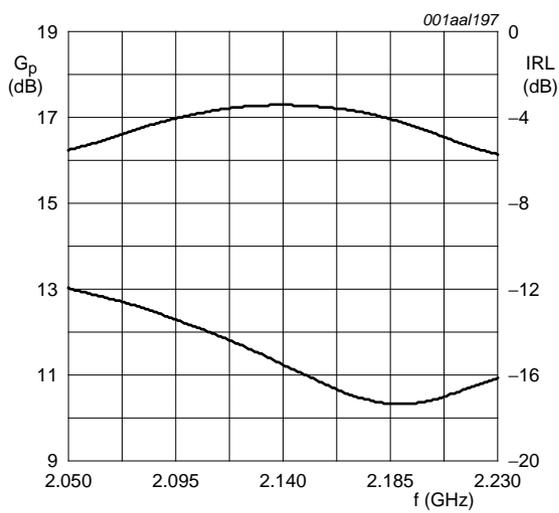- V_{DS} = 28 V
- I_{Dq} = 900 mA
- $V_{GS\,(peak)}$ = 0.5 V

Fig 1. Power gain and input return loss as a function of frequency

Fig 2. Delay as a function of frequency
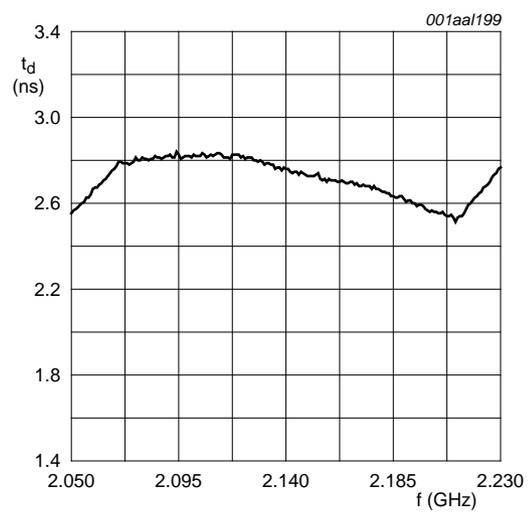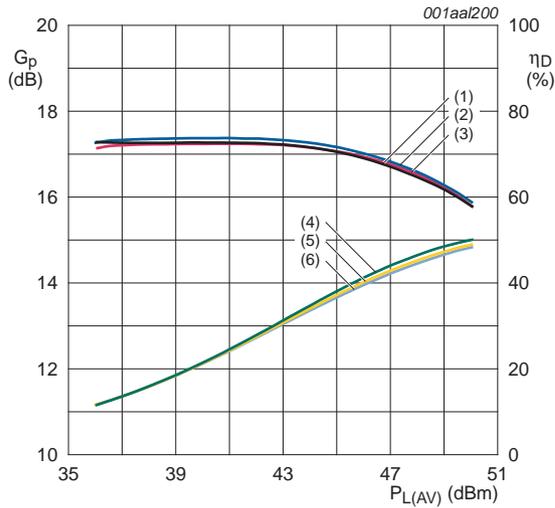
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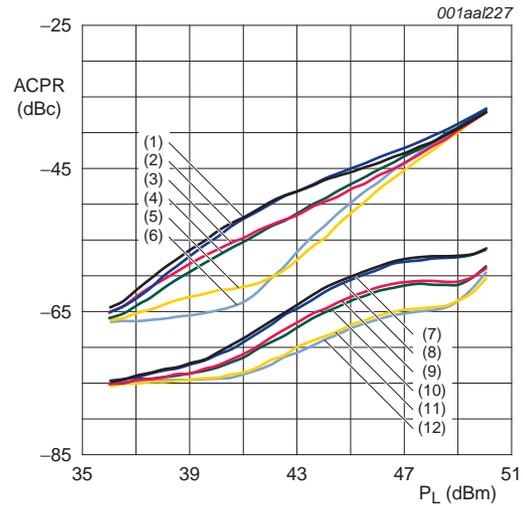
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3.2 IS-95 measurements

The IS-95 measurements were performed under the following conditions:

- Bias: V_{DS} = 28 V

- I_{Dq} = 900 mA

- $V_{GS\,(peak)}$ = 0.5 V

(1) G_p = 2110 MHz.

(2) G_p = 2140 MHz.

(3) G_p = 2170 MHz.

(4) η_D = 2110 MHz.

(5) η_D = 2140 MHz.

(6) η_D = 2170 MHz.

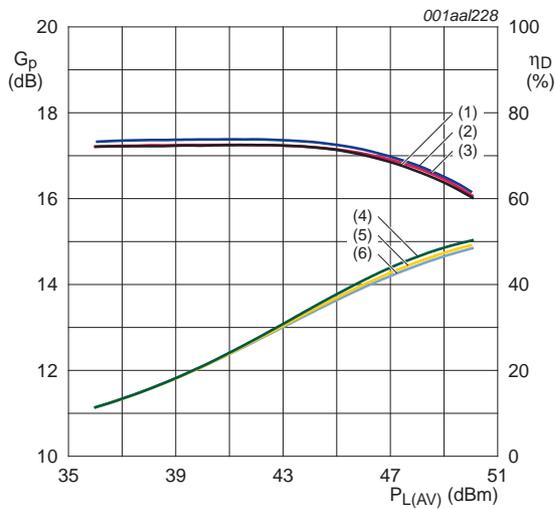**Fig 3.** **Power gain and efficiency as a function of average output power, IS-95**

(1) 2110 MHz − 885 kHz.

(2) 2110 MHz + 885 kHz.

(3) 2140 MHz − 885 kHz.

(4) 2140 MHz + 885 kHz.

(5) 2170 MHz − 885 kHz.

(6) 2170 MHz + 885 kHz.

(7) 2110 MHz − 1.98 MHz.

(8) 2110 MHz + 1.98 MHz.

(9) 2140 MHz − 1.98 MHz.

(10) 2140 MHz + 1.98 MHz.

(11) 2170 MHz − 1.98 MHz.

(12) 2170 MHz + 1.98 MHz.

Fig 4. **Adjacent Channel Power Ratio (ACPR) as a function of output power**

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3.3 2-carrier W-CDMA measurements

These measurements were performed under the following conditions:

- Channel bandwidth = 3.84 MHz, spacing: 15 MHz
- Bias: V_{DS} = 28 V
- I_{Dq} = 900 mA
- $V_{GS (peak)}$ = 0.5 V
- Heatsink temperature (T_h) = 25 °C

(1) G_p = 2110 MHz.
(2) G_p = 2140 MHz.
(3) G_p = 2170 MHz.
(4) η_D = 2110 MHz.
(5) η_D = 2140 MHz.
(6) η_D = 2170 MHz.

Fig 5. Power gain and efficiency as a function of average output power, 2-carrier W-CDMA
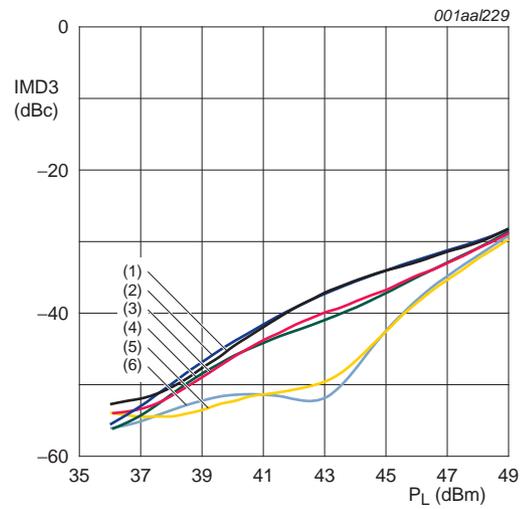
(1) 2110 MHz IMD3 low.
(2) 2110 MHz IMD3 high.
(3) 2140 MHz IMD3 low.
(4) 2140 MHz IMD3 high.
(5) 2170 MHz IMD3 low.
(6) 2170 MHz IMD3 high.

Fig 6. IMD3 as a function of output power, 2-carrier W-CDMA

3.4 Peak output power measurements

Two methods were used to measure peak output power.

- Using a standard IS-95 signal (PAR = 9.7 dB at 0.01 % probability on the CCDF), determining the output power where the PAR reaches 6.7 dB at 0.01 % probability on the CCDF, measured as the 3 dB compression point
- Using the pulsed signal, measuring the 3 dB compression points

The peak power measurements were performed under the following conditions:

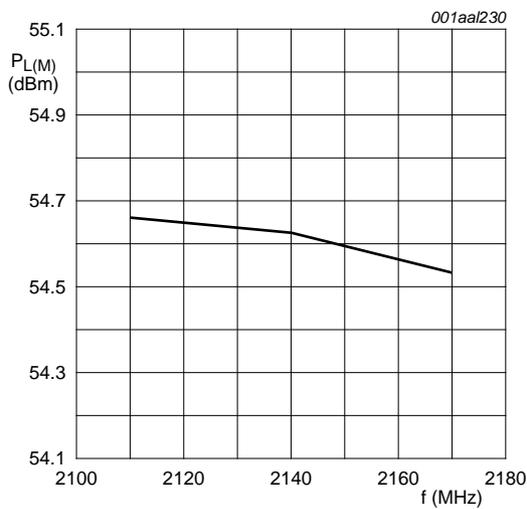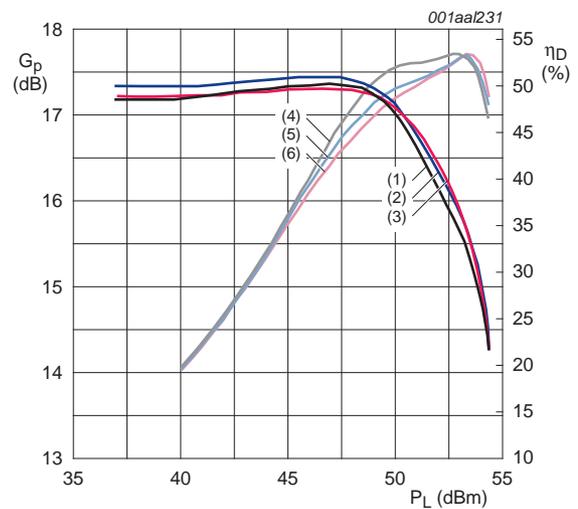- Bias: V_{DS} = 28 V
- I_{Dq} = 900 mA
- $V_{GS\ (peak)}$ = 0.5 V

Fig 7. Peak output power as a function of frequency

(1) f = 2110 MHz.
(2) f = 2140 MHz.
(3) f = 2170 MHz.
(4) f = 2110 MHz.
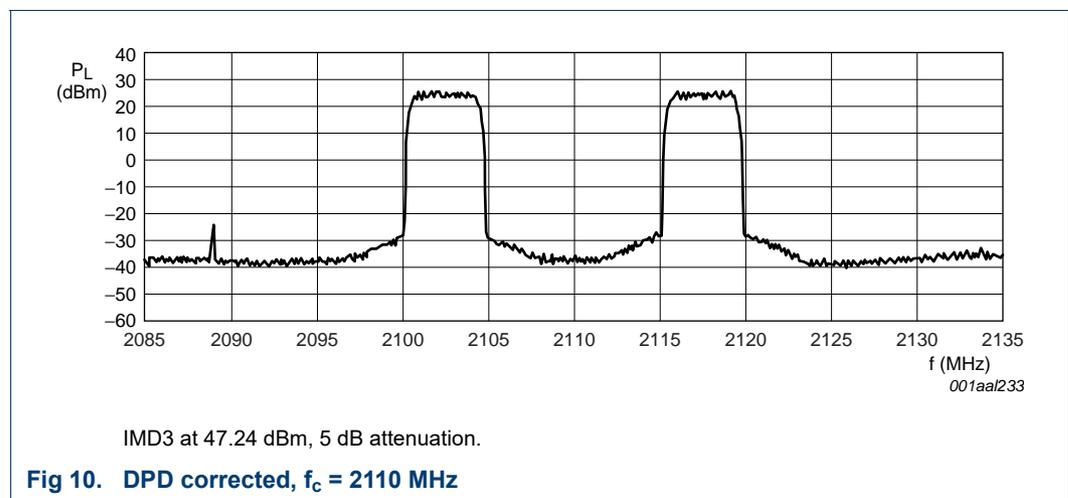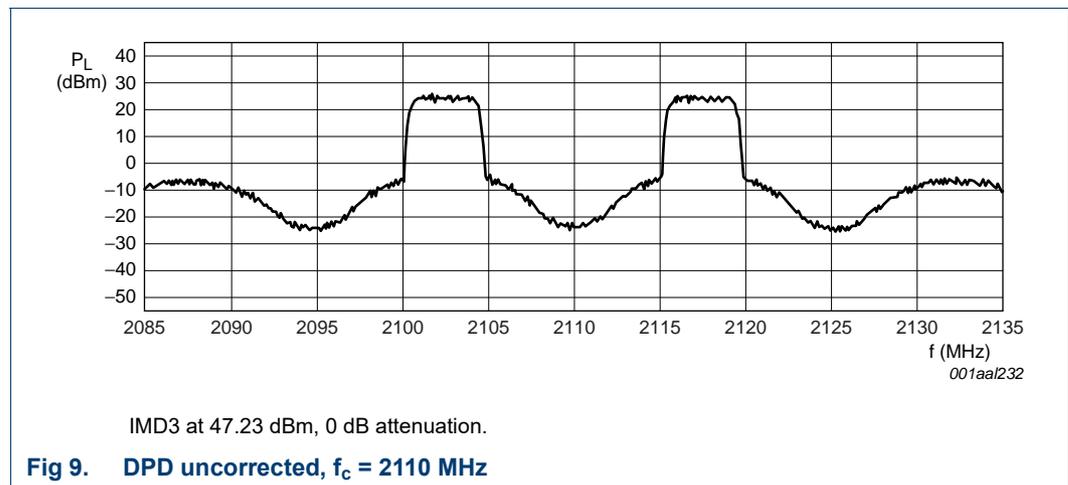(5) f = 2140 MHz.
(6) f = 2170 MHz.

Fig 8. Power gain and efficiency as a function of output power

3.5 DPD measurements

The DPD measurements were performed using an in-house designed DPD system.

The following DPD measurements were performed under the following conditions:

- f_c = 2110 MHz

- DPD system: 2-carrier W-CDMA signal, spacing: 15 MHz

- V_{DS} = 28 V, I_{Dq} = 900 mA, $V_{GS\,(peak)}$ = 0.5 V

- IMD3 at 47.23 dBm, 15 MHz offset (integrated bandwidth = 3.84 MHz) uncorrected (no DPD applied): −31.3 dB and −30.9 dB

- IMD3 at 47.24 dBm, 15 MHz offset (integrated bandwidth = 3.84 MHz) corrected (DPD applied): −60.2 dB and −59.6 dB

- IMD3 correction = 28.9 dB and 28.7 dB

IMD3 at 47.23 dBm, 0 dB attenuation.

Fig 9. DPD uncorrected, f_c = 2110 MHz

IMD3 at 47.24 dBm, 5 dB attenuation.

Fig 10. DPD corrected, f_c = 2110 MHz

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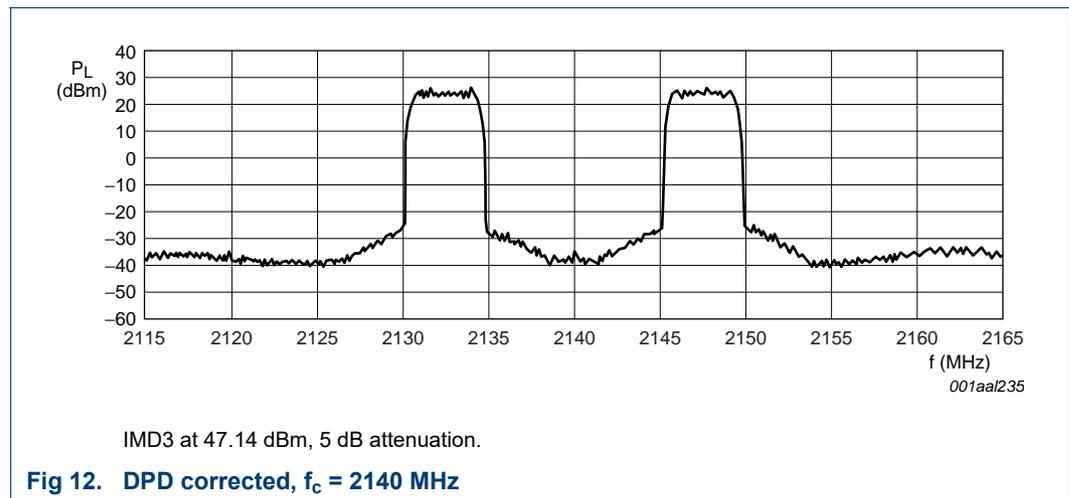
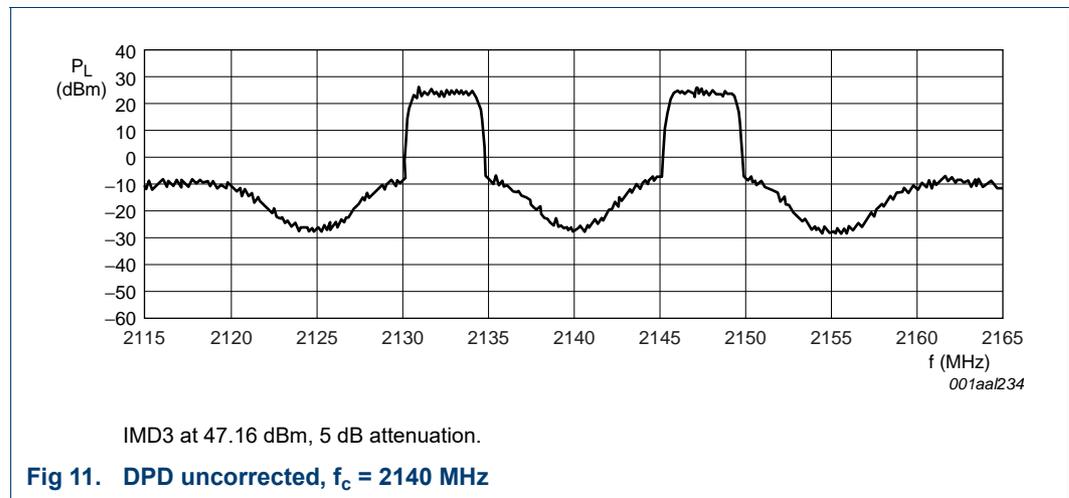**Rev. 3 — 1 September 2015**

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The following DPD measurements were performed under the following conditions:

- f_c = 2140 MHz

- DPD system: 2-carrier W-CDMA signal, spacing: 15 MHz

- V_{DS} = 28 V, I_{Dq} = 900 mA, $V_{GS\,(peak)}$ = 0.5 V

- IMD3 at 47.16 dBm, 15 MHz offset (integrated bandwidth = 3.84 MHz) uncorrected: -33.4 dB and -33.0 dB

- IMD3 at 47.14 dBm, 15 MHz offset (integrated bandwidth = 3.84 MHz) corrected: -59.8 dB and -58.4 dB

- IMD3 correction = 26.4 dB and 25.4 dB

IMD3 at 47.16 dBm, 5 dB attenuation.

Fig 11. DPD uncorrected, f_c = 2140 MHz

IMD3 at 47.14 dBm, 5 dB attenuation.

Fig 12. DPD corrected, f_c = 2140 MHz

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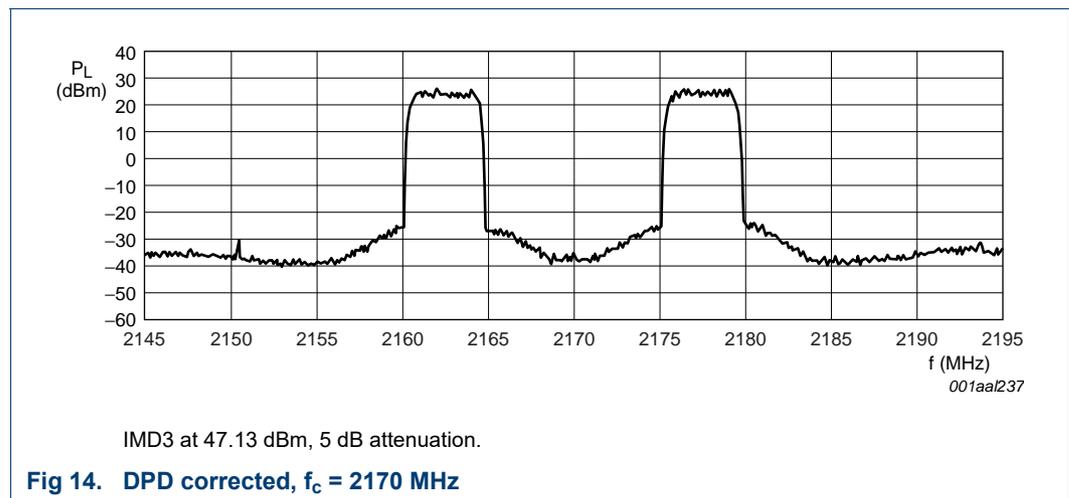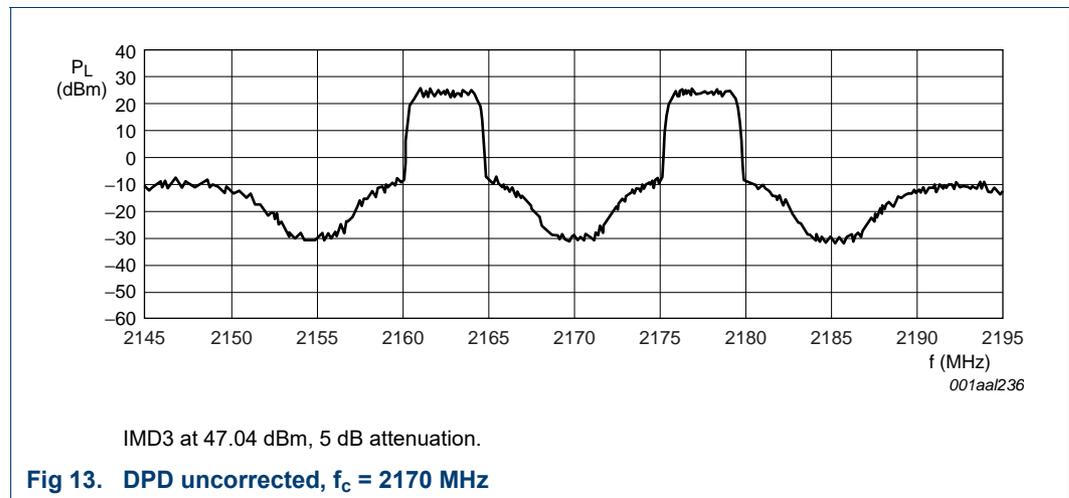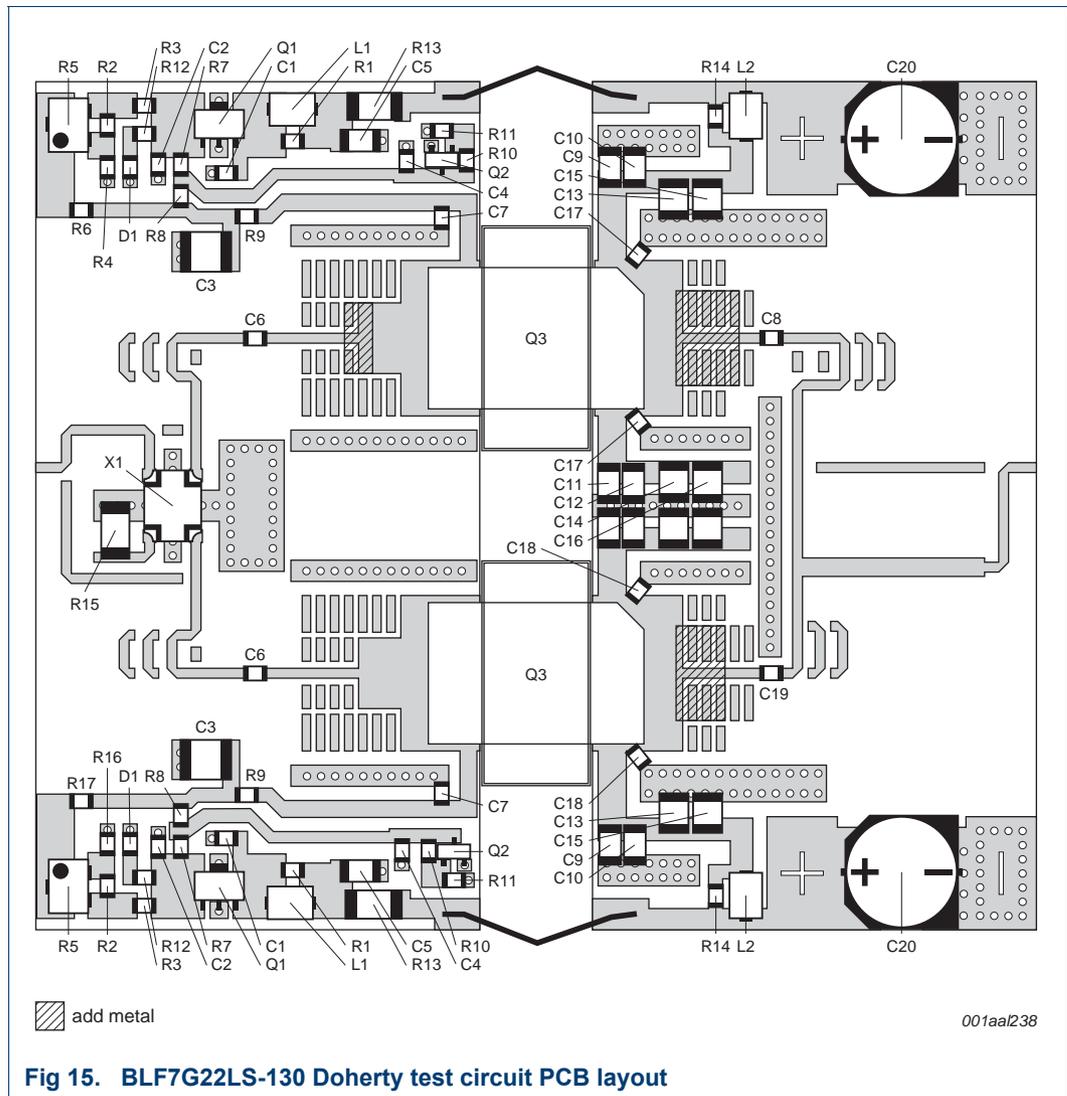**Application note**

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The following DPD measurements were performed under the following conditions:

- f_c = 2170 MHz

- DPD system: 2-carrier W-CDMA signal, spacing:15 MHz

- V_{DS} = 28 V, I_{Dq} = 900 mA, $V_{GS\ (peak)}$ = 0.5 V

- IMD3 at 47.04 dBm, 15 MHz offset (integrated bandwidth = 3.84 MHz) uncorrected: −33.8 dB and −34.7 dB

- IMD3 at 47.13 dBm, 15 MHz offset (integrated bandwidth = 3.84 MHz) corrected: −59.4 dB and −57.9 dB

- IMD3 correction = 25.6 dB and 23.2 dB

IMD3 at 47.04 dBm, 5 dB attenuation.

Fig 13.   DPD uncorrected, f_c = 2170 MHz

IMD3 at 47.13 dBm, 5 dB attenuation.

Fig 14.   DPD corrected, f_c = 2170 MHz

4. BLF7G22LS-130 Doherty test circuit

Fig 15.   BLF7G22LS-130 Doherty test circuit PCB layout

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4.1 BLF7G22LS-130 Doherty test circuit components

Table 2. **BLF7G22LS-130 Doherty test circuit components**

Designator	Description	Part identifier	Manufacturer
Input PCB	Rogers 3006; ε_r = 6.15, ± 0.15; thickness 0.64 mm (0.025"); 35 μm (1 oz.) copper on each side; Ref. 1 on page 13	BLF7G22LS-130 Doherty PA Input-Rev1	Ohio circuits
Output PCB		BLF7G22LS-130 Doherty PA Output-Rev1	Ohio circuits
Q1	78L08 voltage regulator	NJM#78L08UA-ND	NJR
Q2	2N2222 NPN transistor	MMBT2222	Fairchild
Q3	BLF7G22LS-130	BLF7G22LS-130	Ampleon
R1, R14	9.1 Ω	CRCW08059R09FKEA	Vishay Dale
R2, R3, R17	430 Ω	CRCW0805432RFKEA	Vishay Dale
R4	75 Ω	CRCW080575R0FKTA	Vishay Dale
R5	200 Ω, potentiometer	3214-1-201E	Bourns
R6	2 kΩ	CRCW08052K00FKTA	Vishay Dale
R7, R12	1.1 kΩ	CRCW08051K10FKEA	Vishay Dale
R8	11 kΩ	CRCW080511K0FKEA	Vishay Dale
R9	5.1 Ω	CRCW08055R11FKEA	Vishay Dale
R10	5.1 kΩ	CRCW08055K10FKTA	Vishay Dale
R11	910 Ω	CRCW0805909RFKTA	Vishay Dale
R13	499 Ω, 0.5 W	CRCW2010499RFKEF	Vishay Dale
R15	SMT 2010 50 Ω R_L	-	EMC
R16	0 Ω	-	Vishay Dale
X1	3 dB, hybrid coupler, 30 W	1J503S	Anaren
L1, L2	Ferroxcube bead	2743019447	Fair Rite
C1, C2, C4	100 nF ceramic 0805	S0805W104K1HRN-P4	MultiComp
C3	4.7 μF	C4532X7R1H475M	TDK
C5	1 μF	C3216X7R1H105K	TDK
C6, C7, C19	15 pF	600F	American Technical Ceramics
C8	12 pF	600F	American Technical Ceramics
C13, C14	15 pF	ATC100B150JT500X	American Technical Ceramics
C9, C10, C11, C12	1 μF	GRM31CR72A105KA01L	MuRata
C15, C16	10 μF	GRM32DF51H106ZA01L	MuRata
C20	220 μF, 50 V electrolytic SMT	PCE3474CT-ND	Panasonic
C17	1.5 pF	600F	American Technical Ceramics
C18	1.8 pF	600F	American Technical Ceramics

5. Abbreviations

Table 3.   Abbreviations

Acronym	Description
ACPR	Adjacent Channel Power Ratio
CCDF	Complementary Cumulative Distribution Function
DPD	Digital PreDistortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average power Ratio
SMT	Surface-Mount Technology
UMTS	Universal Mobile Telecommunications System
W-CDMA	Wideband Code Division Multiple Access

6. References

[1]   **Data sheet 1.3000; RO3000 Series High Frequency Circuit Materials** – Advanced Circuit Materials Division; Rogers Corporation.

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