AMPLEON

European Microwave Week 2019

Student Design Competition – Thrust 2

The Title of Competition: Wideband Biasing Network Design for High Power Amplifiers

Submission Deadline: September 15, 2019

Sponsor: Ampleon Netherlands B.V.

Primary contact name: Dr. Lazaro Marco-Platon (lazaro.marco@ampleon.com)

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Abstract

This competition will introduce students to the RF high power amplifier (HPA) biasing for wideband applications. Biasing networks plays a key role in video bandwidth (VBW) and RF performance of HPAs.

A design competition titled "Wideband Biasing Network Design for High Power Amplifiers" will take place at the 2019 European Microwave Week in Paris. This competition is open to all students. The main target of the contest is design and realization of a biasing network, considering low insertion loss at the operation bandwidth and low impedance at the low frequency region. The competitors will design and fabricate a biasing network, having a resonance-free low impedance response in the low frequency region. Although students are free to use any topology and material, they need to meet a given set of specifications.

The winner will be the network that demonstrates the widest operation bandwidth having the lowest input impedance in the low frequency region. If there is a tie, wider "accepted operation bandwidth" will be the winner.

A representative of the design team must be present at the competition day. Measurements will be open to all EuMW participants.

Questions can be sent to Dr. Lazaro Marco-Platon and Ali I. Isik.

Last update: *28 May 2019*

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Awards

1st : 1000 €

2nd : 500 €

Promising designs will also be awarded (250 €).

Design Specifications and Rules

1) *The circuit should meet these specifications*
   a. *Center frequency: 2.6 GHz*
   b. *Low insertion loss at operation the band (< 0.3 dB)*
   c. *Low impedance at low frequency region (< 5 Ω)*
   d. *Low DC resistance at the biasing line (< 0.5 Ω)*
   e. *SMA female connector at input and output*
   f. *Length of the circuit must be 50 mm, check Figure 2 for details*
2) *Each team can participate with a maximum of two circuits. If a team consists of five or more students, three circuits are allowed. Each team can have only one reward, even if all designs have the highest scores. Only one team is allowed from each laboratory/workgroup/advisor.*
3) *The students will prepare the circuit(s) for the measurements. The implemented circuits will be reliable for mechanical issues such as cable connection. The organization committee does not accept any responsibility in case of physical damages during the competition.*
4) *All measurement tools will be provided by the organizer such as cables, VNA, etc. A 50 Ω VNA will be used for the measurements.*
5) *The implemented circuit should be suitable for visual inspection. No sealed casing is allowed.*
6) *Active components, embedded batteries, and supercapacitors are not allowed.*
7) *The circuit board can have a maximum of two layers (top layer for signal lines, bottom layer for ground). Students are free to choose the material and thickness of the circuit board.*
8) *No changes are allowed during the measurements.*
9) *The circuit should look like a PA biasing network. Unreasonable designs will be disqualified. A DC blocking capacitor must be included before the output connector.*
10) *There will be three measurements to evaluate the designs:*
   a. *DC resistance: From DC biasing point to input connector, total resistance should be lower than 0.5 Ω. A multimeter will be used for DC resistance measurement.*
   b. *Accepted bandwidth: The band of having less than 0.3 dB insertion loss will be accepted as operation bandwidth. Symmetry will also be considered; please check details.*
   c. *Decoupling bandwidth: The band having less than 5 Ω impedance at the low frequency region seen from the input section*
   d. *The widest decoupling BW will be the winner of the competition. The accepted operation BW should be at least 2.5 times wider than decoupling BW.*
11) *Before the competition day, a detailed report including measured data and design files (such as ADS or AWR workspace) should be submitted to the organizing committee.*

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How to Participate

1. *Request the entry form (by e-mail)*
2. *Submit the entry form before September 15, 2019 (a confirmation letter will be sent)*
3. *Students are encouraged to ask questions and for recommendations*
4. *Submit a brief report including simulations, layout, and measurements before the competition.*
   (The selected projects will receive an acceptance letter to attend the competition.)

Power Amplifier Biasing Networks

A typical PA consists of an active device and at least four passive sub-circuits: input matching, gate biasing, output matching, and drain biasing. Figure 1 depicts such a structure.

A conventional biasing structure of a PA includes a resistor at the gate and an inductor at the drain. These components are RF shorted out at the DC supply point with a couple of RF bypass capacitors. Values of the DC blocking capacitors are often selected at pF level due to their low effective serial resistance (ESR) at the fundamental frequency and high self-resonance frequency (SRF).
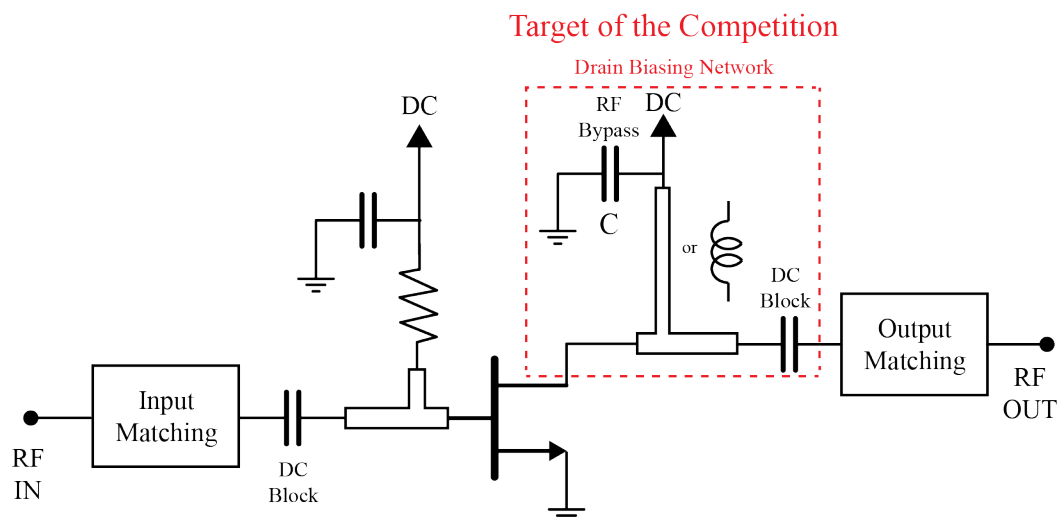

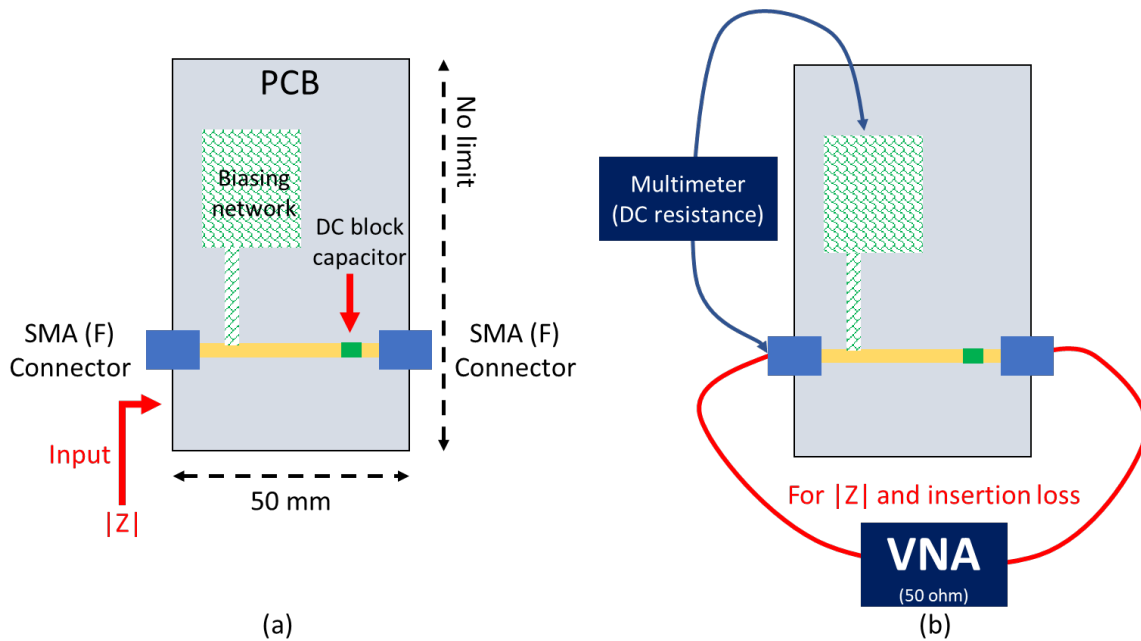**Figure 1.** *Conventional biasing structure of a power amplifier.*

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Figure 2. *Details of the PCB dimensions and measurement direction of |Z| (a), measurement points for VNA and multimeter (b).*

Resources for Biasing Network Design

[1] Ampleon web page, application documents: www.ampleon.com

[2] O. Ceylan, L. Marco-Platon, and S. Pires, "Refine Biasing Networks for High PA Low Frequency Stability," Microwaves RF, vol. 57, no. 4, pp. 52–56, 2018.

[3] A. Khanifar, N. Maslennikov and B. Vassilakis, "Bias circuit topologies for minimization of RF amplifier memory effects," 33rd European Microwave Conference Proceedings, Munich, Germany, 2003, pp. 1349-1352 Vol.3. doi: 10.1109/EUMC.2003.177737

[4] A. A. Aziz, F. Danaher, and A. Hashim, "A Robust Chip Capacitor for Video Band Width in RF Power Amplifiers," in 16th Electronics Packaging Technology Conference (EPTC), 2014, pp. 760–761.
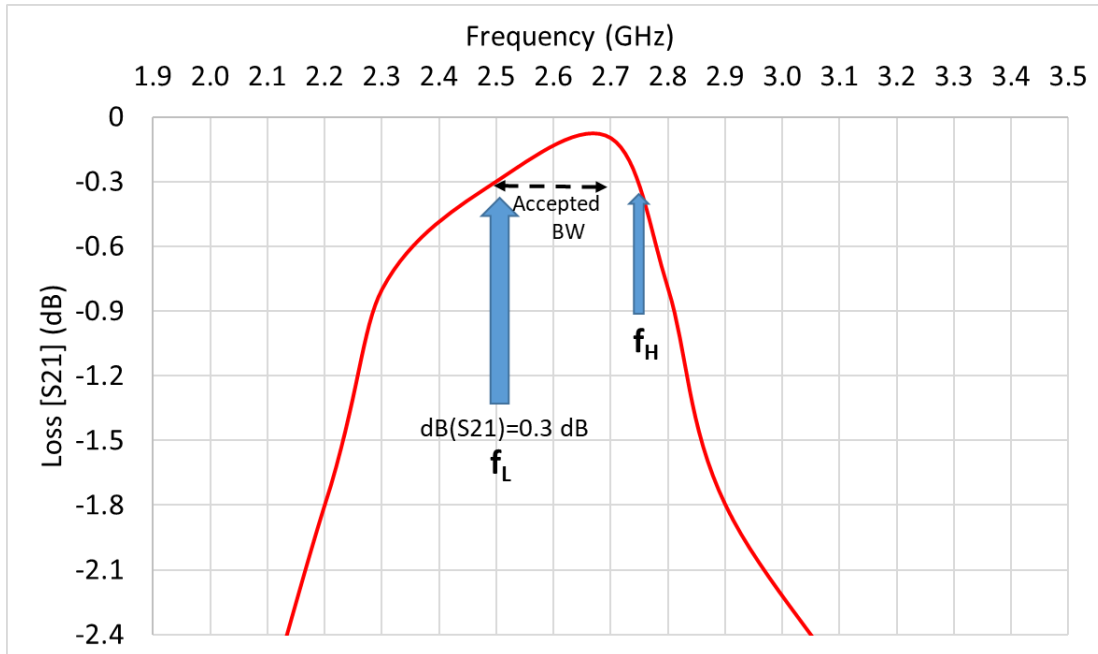
Evaluation Examples
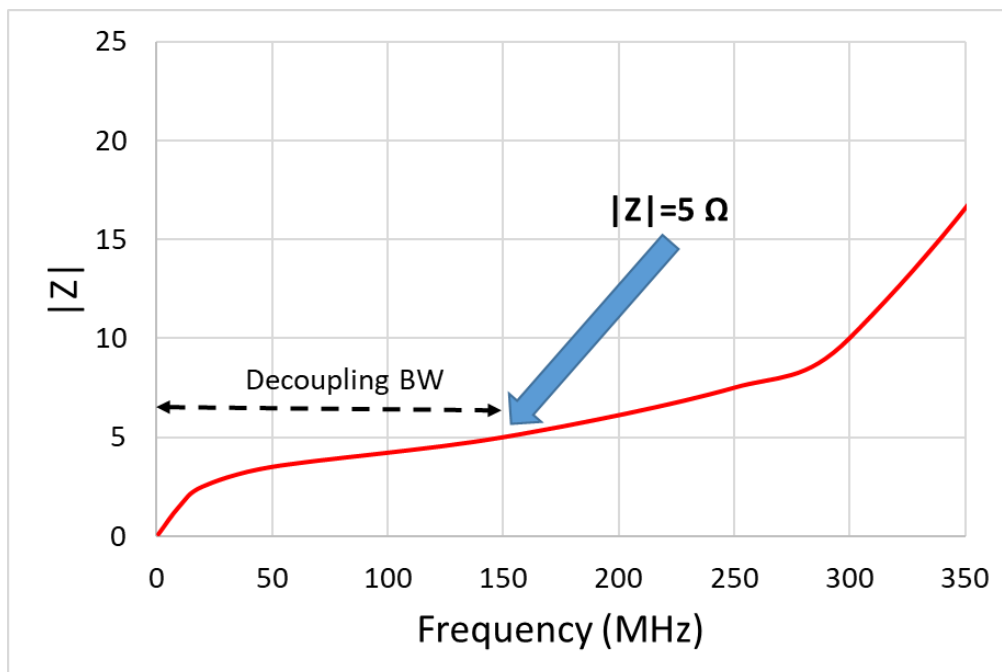
Team A

Figure 3. *Accepted BW of Team A*

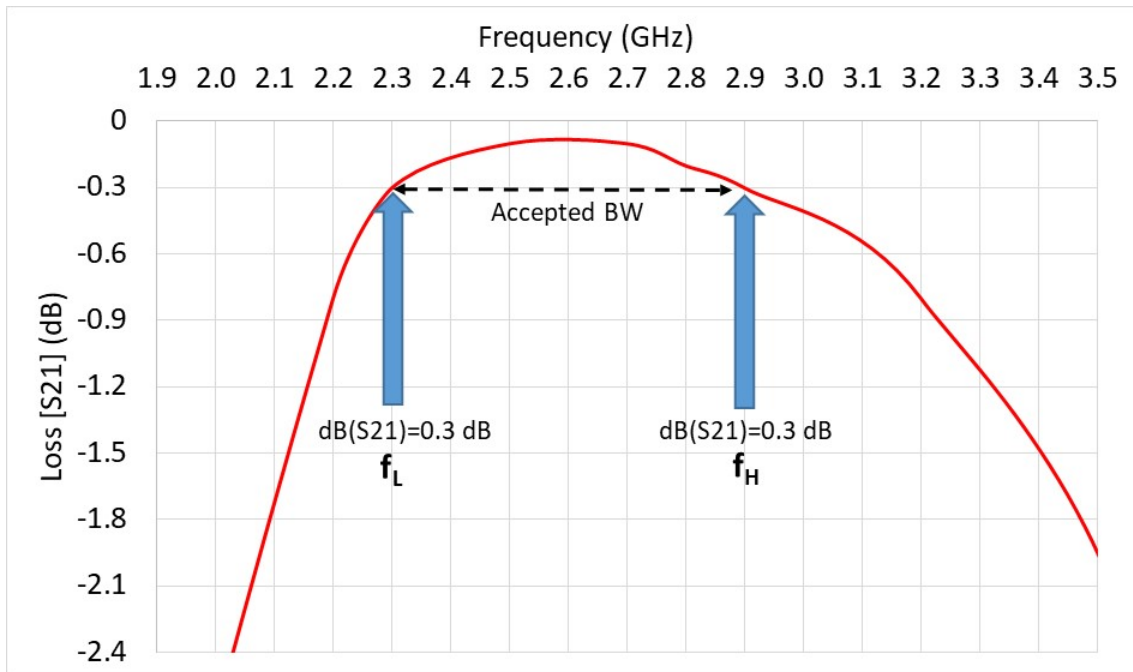**Figure 4.** *Decoupling BW of Team A*

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Figure 5. Accepted BW of Team B
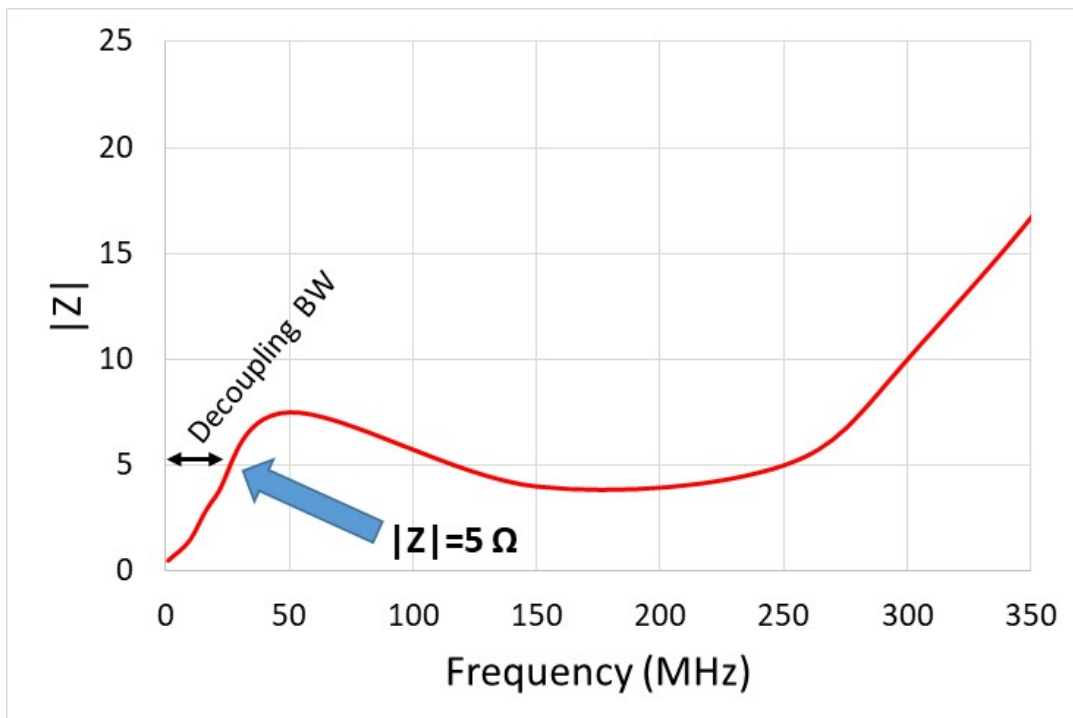
Figure 6. Decoupling BW of Team B

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Team C

Figure 7. Accepted BW of Team C
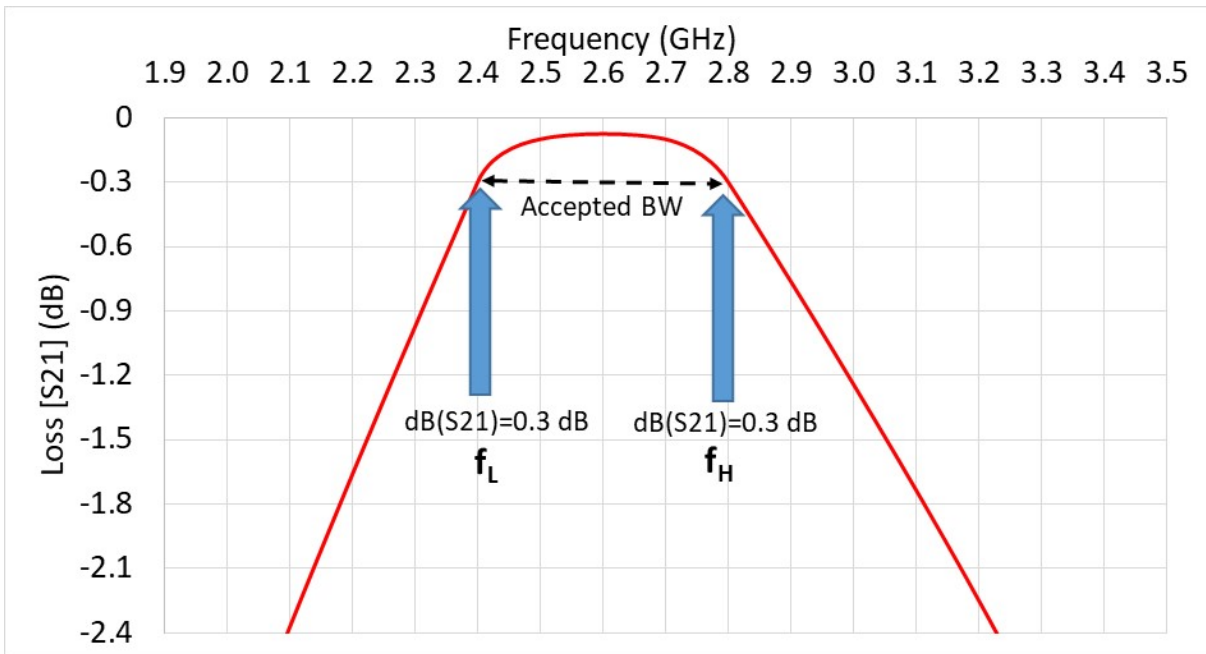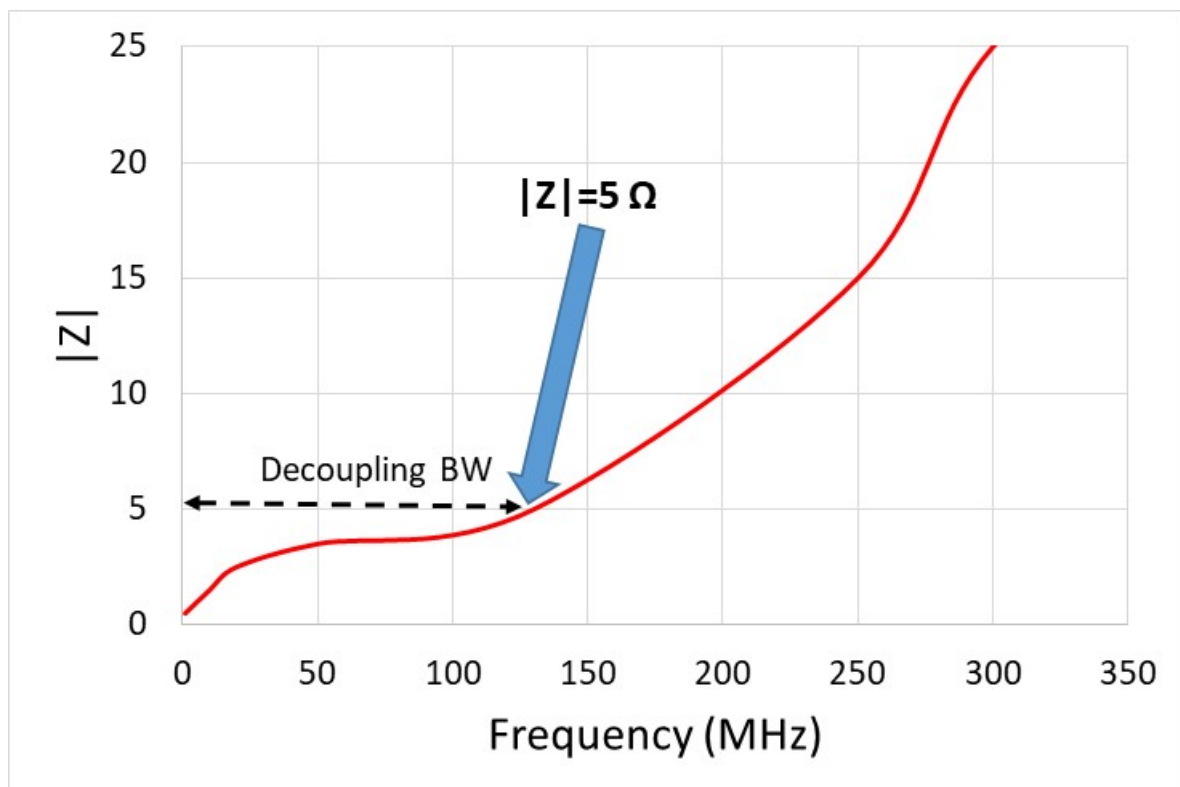

Figure 8. Decoupling BW of Team C

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Score Board

All teams meet DC resistance condition (< 0.5 Ω).

Team A -> Operation BW < 2.5 x Decoupling BW, FAIL

Team B -> Operation BW > 2.5 x Decoupling BW, PASS

Team C -> Operation BW > 2.5 x Decoupling BW, PASS

	Operation BW				
	Low side f_L	High side f_H	Accepted Operation BW	Decoupling BW	Result
Team A	2.50 GHz	2.75 GHz	200 MHz	150 MHz	Disqualified
Team B	2.30 GHz	2.90 GHz	600 MHz	30 MHz	2nd
Team C	2.40 GHz	2.80 GHz	400 MHz	130 MHz	1st

How to calculate symmetric and accepted operation BW:

$$Accepted\ BW\ [MHz] = \begin{cases} 2 \times (2600 - f_L) & if & (2600 - f_L) < (f_H - 2600) \\ 2 \times (f_H - 2600) & if & (2600 - f_L) > (f_H - 2600) \\ f_H - f_L & if & (2600 - f_L) = (f_H - 2600) \end{cases}$$

Organized by Dr. Osman CEYLAN